ARX-2427, 2447 & 2457 UNIVERSAL BUS INTERFACE UNITS TO MIL-STD-1553B

AEROFLEX
An ARX Company

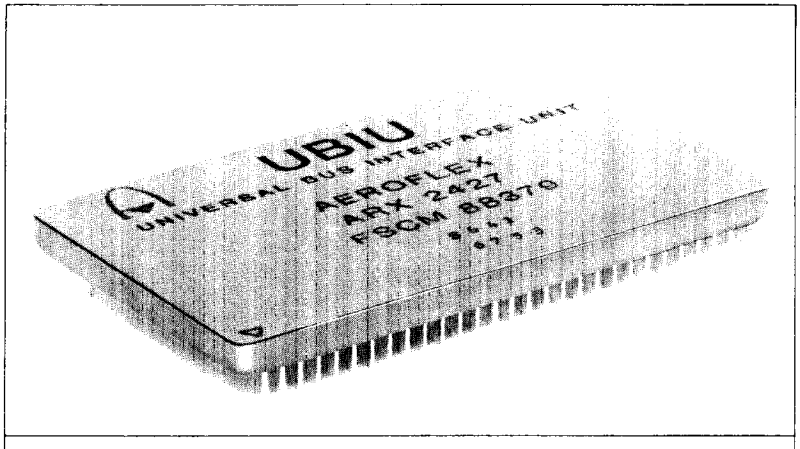
Features

- **Dual redundant remote terminal (RT), Bus Controller (BC) and Bus Monitor (BM) in one unit**
- **Low Power CMOS chip set**
- **Extensive error checking**
- **Continuous self-test**
- **Wrap around data verification while transmitting**
- **Built-in test word**
- **8 or 16 bit Subsystem Interface**
- **Failsafe timeout included**
- **Handles all data transfer formats including broadcast**
- **Handles all mode codes for dual redundant operation.**
- **Status bits externally available**
- **Dual Port Ram subsystem interface**
- **MIL-STD-883 Screened**

Introduction

The UBIU is a single package interface which eliminates the problems associated with 1553 interface selection. This unit will satisfy all bus operational requirements performing the tasks of a remote terminal, a bus controller and a bus monitor. These modes are easily selected using mode select lines in hardware. The UBIU incorporates a powerful on-board Dual Port Ram as the subsystem interface.

The hybrid assembly contains dual transceivers, a Dual Encoder/Decoder, an RTU/BCU/BMU state controller with peripheral logic and registers (called a "Message Processor") and a General Purpose Input/Output Interface (GPIO). The combination handles all of the 1553B protocol and subsystem interfacing. The only parts external to the hybrid are the bus coupling transformers, isolation resistors and an optional PROM if illegal commands and/or mode codes must be detected. Any standard command and/ or mode command may be illegalized. Commands may be illegalized as a function of subaddress, word count, t/r bit or any combination of these characteristics.



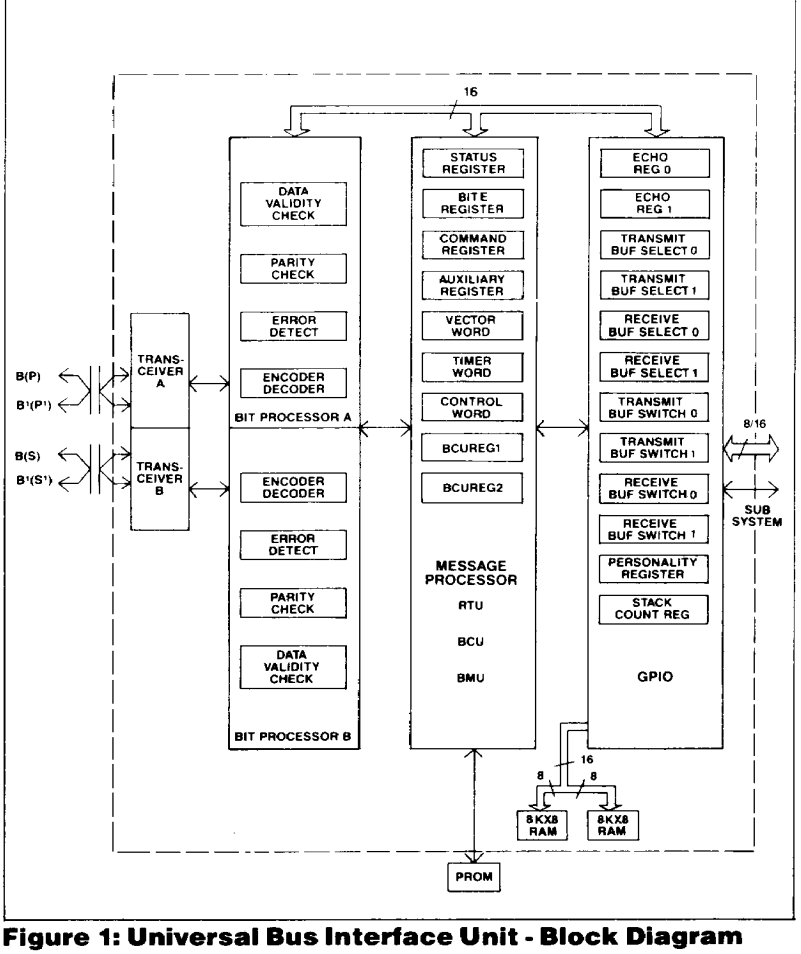


Figure 1: Universal Bus Interface Unit - Block Diagram

Specifications

PARAMETER	ARX 2457 (+5 VOLTS)	ARX 2427 (+5, +15, −15)	ARX 2447 (+5, +12, −12)
Receiver differential input voltage at device terminals	8 V p-p	40 V p-p	28 V p-p
Receiver threshold level at point cc, figure 5	0.42 Vpp MIN, 0.84 Vpp MAX	0.42 Vpp MIN, 0.84 Vpp MAX	0.42 Vpp MIN, 0.84 Vpp MAX
Transmitter output Amplitude at point cc, figure 5	18 Vpp MIN, 27 Vpp MAX	18 Vpp MIN, 27 Vpp MAX	18 Vpp MIN, 27 Vpp MAX
Transmitter output rise and fall time (10% to 90%)	100 ns MIN, 300 ns MAX	100 ns MIN, 300 ns MAX	100 ns MIN, 300 ns MAX
Transmitter output dynamic offset (Tailoff) at point cc, figure 5	±250 mV	±250 mV	±250 mV
Transmitter output noise at point cc, figure 5	10 mVpp MAX	10 mVpp MAX	10 mVpp MAX

POWER SUPPLY REQUIREMENTS	ARX 2457 (+5 VOLTS)	ARX 2427 (+5, +15, −15)	ARX 2447 (+5, +12, −12)
+5 VOLTS STANDBY	120mA MAX	70mA MAX	70mA MAX
+15 VOLTS STANDBY (V_{CC})		64mA MAX	
−15 VOLTS STANDBY (V_{EE})		52mA MAX	
+12 VOLTS STANDBY (V_{CC})			64mA MAX
−12 VOLTS STANDBY (V_{EE})			52mA MAX
+5 VOLTS @ 50% duty cycle	455mA MAX	70mA MAX	70mA MAX
+15 VOLTS @ 50% duty cycle (V_{CC})		172mA MAX	
−15 VOLTS @ 50% duty cycle (V_{EE})		52mA MAX	
+12 VOLTS @ 50% duty cycle (V_{CC})			212mA MAX
−12 VOLTS @ 50% duty cycle (V_{EE})			52mA MAX

Power Supply Tolerance (All devices) +5V ±10% ±15V ±5% ±12V ±5%

Logic Characteristics

TEST	SYMBOL	CONDITION	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	V_{OH1}	I_{OH} = −1.3 mA Pins 4, 12, 20, 43, 44, 45, 46, 50, 51, 52, 53, 59, 60, 67, 97, 98, 99, 100, 101, 104, 105, 106, 107, 108	4		Volts
High Level Output Voltage	V_{OH2}	I_{OH} = −4.0 mA Pins 29, 30, 31, 32, 33, 34, 35, 36, 37, 40, 84, 85, 86, 87, 88, 89, 90, 91, 94	2.4		Volts
Low Level Output Voltage	V_{OL1}	I_{OL} = 1.75 mA Pins 4, 12, 20, 43, 44, 45, 46, 50, 51, 52, 53, 59, 60, 67, 97, 98, 99, 100, 101, 104, 105, 106, 107, 108		0.4	Volts
Low Level Output Voltage	V_{OL2}	I_{OL} = 5.0 mA Pins 29, 30, 31, 32, 33 34, 35, 36, 37, 40, 84, 85, 86, 87, 88, 89, 90, 91, 94		0.4	Volts
Tristate (HIZ) Output Leakage Current	I_{OZ}	0 Volts < V_{IN} < 5.5 V Pins 38, 51, 52, 53, 106, 107	−20	+20	µA
Tristate (HIZ) Input Leakage Current w/Pull Up	I_{IZ}	V_{IN} = 0 Volts Pins 29, 30, 31, 32, 33, 34, 35, 36, 84, 85, 86, 87, 88, 89, 90, 91		360	µA
High Level Input Current (No Pull Ups)	I_{IH1}	V_{IN} = Vdd 5, 6, 7, 8, 9, 10, 11, 47, 48, 49, 61, 62, 63, 64, 65, 66, 83, 102, 103		10	µA
High Level Input Current (Pull Ups)	I_{IH2}	V_{IN} = Vdd Pins 14, 15, 17, 18, 19, 21, 22, 23, 24, 25, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36, 41, 69, 70, 71, 72, 74, 75, 77, 78, 79, 80, 81, 82, 84, 85, 86, 87, 88, 89, 90, 91, 92, 95, 96		10	µA
High Level Input Current (Pull Down)	I_{IH3}	V_{IN} = 2.5 V Pins 13, 16, 38, 39, 73, 76, 93		100	µA
Low Level Input Current (No Pull Ups)	I_{IL1}	V_{IN} = 0.4 V Pins 5, 6, 7, 8, 9, 10, 11, 47, 48, 49, 61, 62, 63, 64, 65, 66, 83, 102, 103		−10	µA
Low Level Input Current (Pull Ups)	I_{IL2}	V_{IN} = 0.4 V Pins 14, 15, 17, 18, 19, 21, 22, 23, 24, 25, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36, 41, 69, 70, 71, 72, 74, 75, 77, 78, 79, 80, 81, 82, 84, 85, 86, 87, 88, 89, 90, 91, 92, 95, 96		−340	µA
Low Level Input Current (Pull Down)	I_{IL3}	V_{IN} = 0.4 V Pins 13, 16, 38, 39, 73, 76, 93		−1.02	mA

TEST	SYMBOL	CONDITION	LIMITS MIN	LIMITS MAX	UNITS
High Level Input Voltage	V_{IH1}	Pins 5, 6, 7, 8, 9, 10, 11, 14, 15, 17, 47, 48, 49, 61, 62, 63, 64, 65, 66, 69, 70, 71, 72, 83, 102, 103	3.5		Volts
High Level Input Voltage	V_{IH2}	Pins 18, 19, 21, 22 23, 24, 25, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36, 41, 74, 75, 77, 78, 79, 80, 81, 82, 84, 85, 86, 87, 88, 89, 90, 91, 92, 95, 96	2.0		Volts
Low Level Input Voltage	V_{IL1}	Pins 5, 6, 7, 8, 9, 10, 11, 14, 15, 17, 47, 48, 49, 61, 62, 63, 64, 65, 66, 69, 70, 71, 72, 83, 102, 103		1.2	Volts
Low Level Input Voltage	V_{IL2}	Pins 18, 19, 21, 22, 23, 24, 25, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36, 41, 74, 75, 77, 78, 79, 80, 81, 82, 84, 85, 86, 87, 88, 89, 90, 91, 92, 95, 96		0.7	Volts

Physical

Temperature

Operating (Case)	−55 deg. C to 125 deg. C
Storage (Ambient)	−55 deg. C to 150 deg. C
Weight	2.0 oz. (56.7 gm.) typ.

Thermal

Thermal Resistance, junction to case, θjc for hottest die	47.2 deg. C per watt
Temperature rise hottest die	22.5 deg. C @ 100% duty cycle

Register Address Table

Address	R/W	Register	Loc
183C	R/W	R – CMD STACK CNT / W – BC TXMT Strobe	GPIO
183A	R/W	R-DATA BLOCK CNT / W – Clear STACK Counters	GPIO
1838	R/W	R – MANUAL BUFF / W – AUTO BUFF	GPIO
1836	R	Clear interrupt (Level Mode)	GPIO
1834	R/W	PERSONALITY	GPIO
1832	R/W	ECHO HI	GPIO
1830	R/W	ECHO LO	GPIO
182E	R	TXMT SELECT HI	GPIO
182C	R	TXMT SELECT LO	GPIO
182A	R	REC SELECT HI	GPIO
1828	R	REC SELECT LO	GPIO
1826	R/W	TXMT SWITCH HI	GPIO
1824	R/W	TXMT SWITCH LO	GPIO
1822	R/W	REC SWITCH HI	GPIO
1820	R/W	REC SWITCH LO	GPIO
1814	R	Control World	MP
1812	R	Time tag	MP
1810	R/W	BC CMD WRD REG 2	MP
180E	R	COMMAND WORD	MP
180C	R	BITE WRD	MP
180A	R	AUX. REG	MP
1808	R/W	VECTOR WORD	MP
1804	R/W	BC CMD WRD REG 1	MP
1802	R	STATUS WORD	MP

Internal Registers

Registers have been included in the device to enable the subsystem to control the various operations. They are accessible via a memory mapped addressing scheme.

A. MESSAGE PROCESSOR

Status Register (READ only)

BIT 0	Terminal Flag
BIT 1	Dynamic Bus Control Acceptance
BIT 2	Subsystem Flag
BIT 3	Busy
BIT 4	Broadcast Received
BIT 5:7	RSV (0:2)
BIT 8	Service Request
BIT 9	Instrumentation Bit
BIT 10	Message Error
BIT 11:15	Remote Terminal Address (0:4)

Built-in test (BITE) Register (READ ONLY)

BIT 0	Transmitter Inhibit Primary
BIT 1	Transmitter Inhibit Secondary
BIT 2	Broadcast Transmit Error (Bus Controller mode)
BIT 3	Failsafe 0
BIT 4	Failsafe 1
BIT 5	Handshake Fail
BIT 6	Looptest Fail
BIT 7	Illegal Command Received
BIT 8	Illegal Word Count
BIT 9	Illegal Subaddress
BIT 10	Zero
BIT 11	T/R Bit Wrong
BIT 12	Low Word Error
BIT 13	High Word Error
BIT 14	Sync Error
BIT 15	Datamatch Error

Command Register (READ only)

This register holds the Command Word received while operating in the Remote Terminal mode, or it holds the Status Word received from the transmitting RT during Bus Controller mode of operation.

Auxiliary Register (READ only)

This register is used in the Bus Controller mode to hold the Status Word received from the receiving RT during an RT to RT transfer.

Vector Word (READ/WRITE)

The contents of this register are transmitted when a Transmit Vector Word mode command is received during Remote Terminal mode of operation. This register can be accessed by the subsystem for a READ or a WRITE.

Time Tag (READ only)

This register is effectively a sixteen bit time tag counter which will be incremented every 20 microseconds. The counter is cleared during power up initialization or after receiving a reset mode command or an external reset.

Control Word (READ only)

BIT 0:4	Word Count (0:4)
BIT 5:9	Subaddress (0:4)
BIT 10	T/R Bit
BIT 11	Latched Broadcast
BIT 12	Latched Mode Code
BIT 13:15	Zero

BCU Register 1 (READ/WRITE)

This register is used by the subsystem in the Bus Controller mode to load receive command word, transmit command word or a receive command word of a RT to RT transfer.

BCU Register 2 (READ/WRITE)

This register is used by the subsystem in the Bus Controller mode to load the transmit command word of an RT to RT transfer.

B. GPIO

Echo Register 0 and Echo Register 1 (READ/WRITE)

These two sixteen bit registers are used to provide rapid echo back responses. The 32 bits in these two registers correspond to the 32 subaddresses. If any one bit is set to a "1" then after receiving a valid transmit command with the corresponding subaddress the data is transmitted from the receive area instead of the transmit area. Therefore, if there is a receive command followed by a transmit command with the same subaddress and the corresponding bit in the Echo Register is set, then the data received with receive command would be transmitted back in response to the transmit command. This enables a bus controller to verify the proper functioning of a remote terminal.

Transmit Buffer Select 0 and Transmit Buffer Select 1 (READ only)

These two 16 bit registers are used to determine the current buffer area for each transmit subaddress. A bit set to "0" will indicate that buffer A is the current buffer and "1" will indicate buffer B as current. The subsystem only has access to the non-current area.

Receive Buffer Select 0 and Receive Buffer Select 1 (READ only)

These two 16 bit registers are used to determine the current buffer area for each receive subaddress. A bit set to "0" will indicate buffer A is the current buffer and "1" will indicate buffer B as current. The subsystem only has access to the non-current area.

Transmit Buffer Switch 0 and Transmit Buffer Switch 1 (READ/WRITE)

These two 16 bit registers have a 1 to 1 correspondence with Transmit Buffer Select 0 and Transmit Buffer Select 1. The subsystem writes to these registers the information to re-assign the buffers for Transmit Area. The contents of these registers are transferred to the corresponding transmit Buffer Select 0 and Transmit Buffer Select 1 when the Message Processor is idle. This register is used in Standard Mode.

Clear Interrupt Register (READ only)

This is used to reset the Data Interrupt output to a high in the level mode.

Auto Buffer Select Register (WRITE)

Manual Buffer Select Register (READ)

Data Block Count Register (READ)

This register contains the Stack Mode block count.

Clear Stack Register (WRITE)

Writing to this register clears the data block count and stack block count registers

Command Stack Count Register (READ)

This register contains the Stack Mode command block count.

Receive Buffer Switch 0 and Receive Buffer Switch 1 (READ/WRITE)

These two 16 bit registers have a 1 to 1 correspondence with Receive Buffer Select 0 and Receive Buffer Select 1. In Manual Mode the Subsystem can write all zeros or all ones by setting D0 and D8 to a zero or a one. The contents of these registers are then transferred to the corresponding Receive Buffer Select 0 and Receive Buffer Select 1 when the Message Processor is idle, and the device is in Auto Mode. At the completion of a receive command the bit corresponding to subaddress of that command is toggled, unless the ECHO bit is set for that subaddress.

Personality Register (READ/WRITE)

BIT 0	$\overline{BM}$
BIT 1	$\overline{RT}$
BIT 2	$\overline{BC}$
BIT 3	$\overline{STACK}$/Std Mem Config.
BIT 4	Failsafe Pri.
BIT 5	Failsafe Sec.
BIT 6	Parity Add.
BIT 7	$\overline{AUTO}$/Manual Buffer Switch
BIT 8	Interrupt Type (Pulse or Level)
BIT 9	Inhibit Command Counter
BIT 10	Inhibit Transmit Counter
BIT 11	Inhibit Receive Counter
BIT 12	Internal BC Transmit Strobe
BIT 13:15	Zero

Remote Terminal Mode

In the Remote Terminal mode of operation the device responds to the receive, transmit, RT to RT transfer and all the mode commands with the exception of selective shutdown and override selective shutdown. The data for these operations is stored in the on-board Ram controlled by the GPIO section.

Extensive error checking is performed on both the received and transmitted data. If an error is detected during a receive operation the ERRLINE is pulsed low, thereby inhibiting any data transfer to the subsystem. On the other hand, if data is received without errors by the terminal the subsystem is informed that good data has appeared. The Data Interrupt (DI) output becomes active after reception of good data. Some of the error conditions monitored include:

- High and low word counts
- High and low bit counts
- Gap errors

- Manchester, sync and parity errors
- Data and word validity
- Handshake errors
- Timeout errors
- Improper transmissions
- Continuous loopback test errors

All the errors are recorded in the STATUS and BITE registers. The COMMAND, STATUS and BITE registers are updated on a message by message basis unless a Transmit Status Word or a Transmit Last Command or Transmit Bit Word command is being processed.

Since the device does a continuous loopback test when transmitting, actually receiving its own transmission, the same checks and data validation performed on received messages are performed on transmit messages.

Data is transferred to and from the subsystem by the GPIO section. It is configured as a Dual Port Ram. The double sided double buffered design eliminates contention problems. The data I/O can be set to interface in an 8 or 16 bit configuration, via BW and A0 input pins.

Data is mapped into the Ram blocks using the subaddress and the T/R bit fields of the command word in the standard memory configuration. In the stack configuration the data is stored in the same sequence as received. An alternate method of Ram mapping is to decode the subaddress into a new vector pointer using an external PROM. The PROM output is then used in place of the subaddress to map data into the Ram.

The data is always received or transmitted from the active side. The sides are switched automatically after receiving good data if in AUTO BUF Mode. The subsystem has access to the non-active side.

	SUB.ADR.		RT MODE
STD. CONFIG.	31	xmt	32 wrds
		rcv	32 wrds
	0	xmt	32 wrds
		rcv	32 wrds
STACK CONFIG.	BLOCK		
		Command Word Stack*	256 wrds
	31	xmt	32 wrds
	30	xmt	32 wrds
	0	xmt	32 wrds
	31	rcv	32 wrds
	30	rcv	32 wrds
	1	rcv	32 wrds
	0	rcv	32 wrds

* Command Word Stack stores command word, actual word count and status word consecutively, for each command.

Bus Controller Mode

In the BCU mode the device controls all the message and data transfers on the bus. The subsystem uses BCUCMDRG1 and BCUCMDRG2 for command word transmission. The COMMAND and AUXILIARY registers are used to hold the received Status words.

After command word transmission the responses are checked. All the error checking performed in the RTU mode is also done in the BCU mode, with the following additions:

- Status response times are checked
- Response terminal address is checked
- All data words, whether transmitted or received, are checked
- All commands are checked
- RT to RT responses are checked

For a transmit command the received data is validated, then loaded into the Ram receive area, if no errors are detected.

For a receive command the data is transmitted from the transmit area of the Ram.

A Broadcast Transmit Error bit is set in the Bit Word if a transmit command with address of all ones is initiated by the Bus Controller.

Bus control cycle is initiated by either applying a 3 microsecond pulse to the BCUXMT input line or writing into address 183C.

Bus Monitor Mode

This mode of operation configures the device as a passive Bus Monitor. In this condition the device receives and stores all the message traffic on the bus. Command words, data words and status words are stored on a message by message basis. A time tag word is stored in the Ram after receipt of the data words in the message. For a transmit command this would be at the end of the message, while for a receive command it would be between the last data word and the status response.

	Rt. Add.		BM MODE
STD. CONFIG.	31	xmt/rcv	64 wrds
	30	xmt/rcv	64 wrds
	1	xmt/rcv	64 wrds
	0	xmt/rcv	64 wrds
STACK CONFIG.	BLOCK		
	63	xmt/rcv	64 wrds
	46	xmt/rcv	64 wrds
	1	xmt/rcv	64 wrds
	0	xmt/rcv	64 wrds

Actual word count is stored at the highest address in each data block for both configurations.

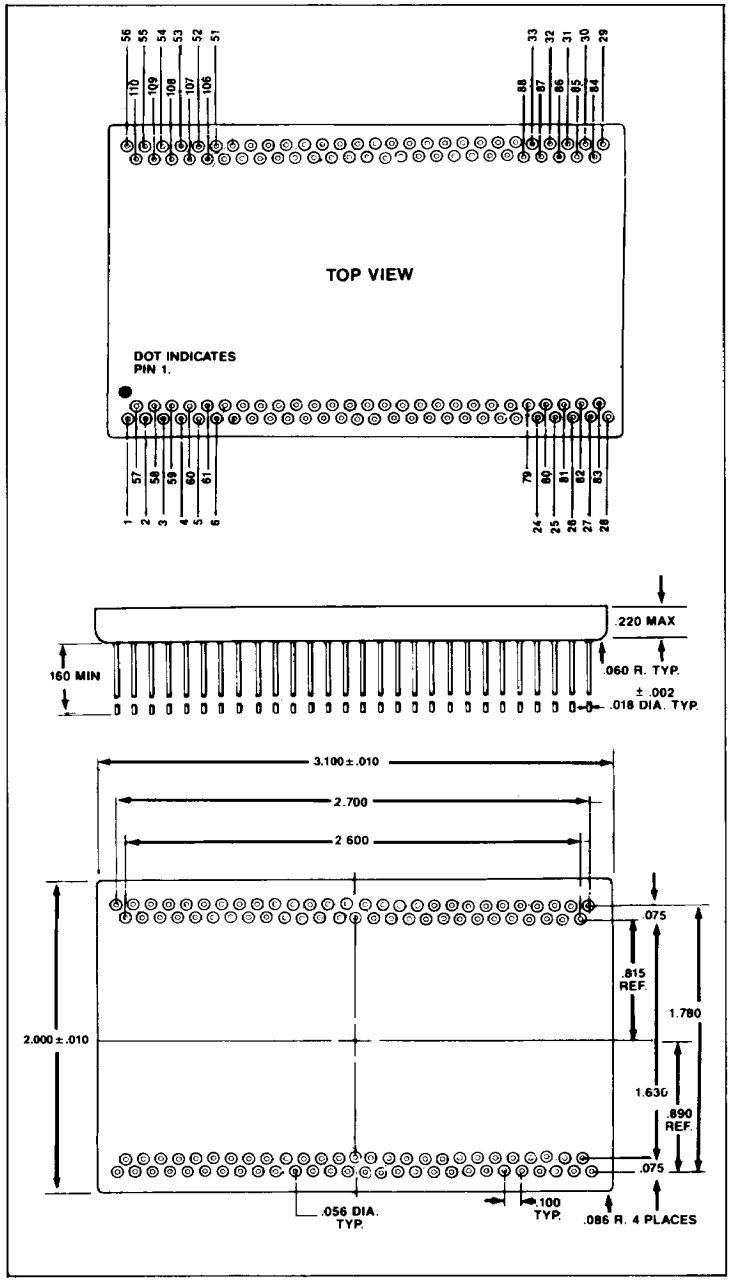
If an error is detected or a response timeout occurs, the time tag word is inserted after the last valid word.

If the terminal has been assigned an address the device can be made to respond to a command bearing that monitor's address as an RT.

The RT/$\overline{BC}$ and $\overline{BM}$ lines select the configuration of the device per the table below.

RT/$\overline{BC}$	$\overline{BM}$	Configuration
0	0	BMU without address resp.
1	0	BMU with address resp.
0	1	BCU
1	1	RTU

Figure 2: Mechanical Outline 110 Pins



The message received is stored at the location corresponding to the remote terminal address received in the standard memory configuration. After receiving the message the sides are switched. The received message is then available to the subsystem. In the stack configuration the data is stored in the same sequence as received.

Figure 3: Pin Connection Table

PIN	LINE(S)	I/O	DESCRIPTION
1	P $\overline{DATA}$	I/O	PRIMARY SERIAL BUS INPUT/OUTPUT
2	V_{EEP}	I	PRI. BUS NEGATIVE SUPPLY VOLTAGE
3	V_{CCP}	I	PRI. BUS POSITIVE SUPPLY VOLTAGE
4	MEO	O	MESSAGE ERROR OUTPUT
5	CWC/$\overline{MDCDOVRD}$	I	STORES RECEIVED MODE CODE DATA WORD IN LOCATION 00001 OR THAT OF MODE CODE NUMBER
6	BCUCHNS/$\overline{P}$	I	PRI. OR SEC. BUS SELECT IN BCU MODE
7	INSBIT	I	INSTRUMENTATION STATUS WORD BIT
8	RSV 2	I	RESERVED STATUS WORD BIT 2
9	RSV 0	I	RESERVED STATUS WORD BIT 0
10	$\overline{SUBSYSFAIL}$	I	TELLS UBIU OF SUBSYSTEM FAILURE
11	$\overline{BCUXMT}$	I	STARTS MESSAGE CYCLE IN BCU MODE
12	$\overline{STADERR}$	O	IMPROPER ADDRESS IN RETURNED STATUS WORD IN BCU MODE
13	RTADR P	I	RTU ADDRESS PARITY BIT
14	RTADR 3	I	RTU ADDRESS BIT 3
15	RTADR 1	I	RTU ADDRESS BIT 1
16	CLK	I	12 MHz CLOCK
17	$\overline{UBIURSTIN}$	I	UBIU RESET (RESETS DEVICE TO POWER UP)
18	$\overline{BRDINH}$	I	INHIBITS PRI & SEC BROADCAST RECOGNITION
19	$\overline{FAILSFTST}$	I	ENABLES PRI & SEC FAILSAFE CIRCUITS FOR TEST PURPOSES
20	$\overline{INCMD}$	O	GOES LOW WHILE UBIU IS PROCESSING ANY MESSAGE
21	A 1	I	BUS ADDRESS BIT 1
22	A 3	I	BUS ADDRESS BIT 3
23	A 5	I	BUS ADDRESS BIT 5
24	A 7	I	BUS ADDRESS BIT 7
25	A 9	I	BUS ADDRESS BIT 9
26	A 11	I	BUS ADDRESS BIT 11
27	BW 8/$\overline{16}$	I	BUS WIDTH (8 OR 16 BITS)
28	CASE GND	I	CASE GROUND
29	D 15	I/O	DATA BUS BIT 15
30	D 13	I/O	DATA BUS BIT 13
31	D 11	I/O	DATA BUS BIT 11
32	D 9	I/O	DATA BUS BIT 9
33	D 7	I/O	DATA BUS BIT 7
34	D 5	I/O	DATA BUS BIT 5
35	D 3	I/O	DATA BUS BIT 3
36	D 1	I/O	DATA BUS BIT 1
37	RTE	O	A HIGH PULSE INDICATES RECEPTION OF A VALID COMMAND (OR STATUS) WORD CONTAINING THE TERMINAL'S ADDRESS
38	$\overline{STACK\ MODE}$	I	SELECTS STD/STACK MEM. CONFIG.
39	$\overline{BUSMONITOR}$	I	CONFIGURATION MODE SELECT
40	$\overline{ACKNOWLEDGE}$	O	SUCCESSFUL SUBSYSTEM READ OR WRITE
41	$\overline{READ}$	I	READ DATA STROBE
42	GND	I	DIGITAL GROUND
43	WRDCNT 4	O	WORD COUNT CMD WORD BIT 4
44	WRDCNT 2	O	WORD COUNT CMD WORD BIT 2
45	WRDCNT 0	O	WORD COUNT CMD WORD BIT 0
46	$\overline{BCUSTATRCV}$	O	STATUS WORD HAS BEEN RECEIVED
47	$\overline{MEI}$	I	MESSAGE ERROR DETECTED FROM PROM
48	$\overline{T/RWRONG}$	I	T/R ERROR DETECTED FROM PROM
49	$\overline{ILLWRDCNT}$	I	WORD COUNT ERROR DETECTED FROM PROM
50	$\overline{UBIURSTOUT}$	O	PULSES LOW IF A RESET RTU MODE CODE IS RECEIVED IN THE RTU MODE OR POWER ON RESET

PIN	LINE(S)	I/O	DESCRIPTION
51	SA/ADR 4	O	BIT 4 OF SUBADDRESS FIELD OF COMMAND WORD IN RTU MODE BIT 4 OF ADDRESS FIELD OF COMMAND WORD IN BMU MODE
52	SA/ADR 2	O	BIT 2 OF SUBADDRESS
53	SA/ADR 0	O	BIT 0 OF SUBADDRESS
54	$V_{CC}S$	I	SEC. BUS POSITIVE SUPPLY VOLTAGE
55	$V_{EE}S$	I	SEC. BUS NEGATIVE SUPPLY VOLTAGE
56	S $\overline{DATA}$	I/O	SECONDARY SERIAL BUS INPUT/OUTPUT
57	P DATA	I/O	PRIMARY SERIAL BUS INPUT/OUTPUT
58	P ANA GND	I	PRIMARY ANALOG GROUND
59	$\overline{INI}$	O	PULSES LOW WHEN A NEW COMMAND STARTS
60	TF	O	TERMINAL FLAG OUTPUT
61	$\overline{SAENA}$	I	TRI-STATES SA (0-4) WHEN A PROM IS USED TO DECODE SUBADDRESSES
62	$\overline{DBCACK}$	I	DYNAMIC BUS ACCEPTANCE
63	SERREQ	I	SERVICE REQUEST STATUS BIT
64	RSV 1	I	RESERVED STATUS WORD BIT 1
65	$\overline{SUBSYSTEMBUSY}$	I	TELLS UBIU SYBSYSTEM IS BUSY
66	$\overline{BCUSYNCTYP}$	I	SET SECOND COMMAND WORD SYNC FOR RT-RT TRANSFER IN BCU MODE
67	$\overline{SYNC/BCUCLSTST}$	O	PULSES LOW IF A SYNC MODE CODE IS RECEIVED IN THE RTU MODE; INDICATES CLEAR STATUS RECEIVED IN BCU MODE
68	+5V	I	+5V LOGIC SUPPLY VOLTAGE
69	RTADR 4	I	RTU ADDRESS BIT 4
70	RTADR 2	I	RTU ADDRESS BIT 2
71	RTADR 0	I	RTU ADDRESS BIT 0
72	$\overline{POC}$	I	POWER ON CLEAR
73	PARERR	I	PARITY ERROR INPUT TO ENCODER
74	$\overline{BITERR}$	I	PUTS DATA ERROR INTO LOOPBACK
75	$\overline{FLSFINH}$	I	DISABLES PRI & SEC FAILSAFE TIMEOUT
76	A 0	I	BUS ADDRESS BIT 0, LOW BYTE ENABLE
77	A 2	I	BUS ADDRESS BIT 2
78	A 4	I	BUS ADDRESS BIT 4
79	A 6	I	BUS ADDRESS BIT 6
80	A 8	I	BUS ADDRESS BIT 8
81	A 10	I	BUS ADDRESS BIT 10
82	A 12	I	BUS ADDRESS BIT 12
83	RAM EXT.	I	SELECTS UPPER AND LOWER 4K×16 AREAS

PIN	LINE(S)	I/O	DESCRIPTION
84	D 14	I/O	DATA BUS BIT 14
85	D 12	I/O	DATA BUS BIT 12
86	D 10	I/O	DATA BUS BIT 10
87	D 8	I/O	DATA BUS BIT 8
88	D 6	I/O	DATA BUS BIT 6
89	D 4	I/O	DATA BUS BIT 4
90	D 2	I/O	DATA BUS BIT 2
91	D 0	I/O	DATA BUS BIT 0
92	HIRAM	I	SELECT BLOCKS 48 TO 63 IN BM STACK MODE
93	RT/$\overline{BC}$	I	CONFIGURATION MODE SELECT
94	$\overline{DI}$	O	GOES LOW WITH EACH $\overline{GBT}$ AND IS CLEARED BY SUBSYSTEM READ IN THE LEVEL MODE. PULSES HIGH FOR EACH $\overline{GBT}$ IN PULSE MODE.
95	$\overline{WRITE}$	I	WRITE DATA STROBE
96	$\overline{CHIPSEL}$	I	ENABLES DATA I/O
97	$\overline{PRMENA}$	O	ENABLES ERROR AND/OR SUBADDRESS DECODING PROM(S)
98	WRDCNT 3	O	WORD COUNT CMD WORD BIT 3
99	WRDCNT 1	O	WORD COUNT CMD WORD BIT 1
100	$\overline{LTBRDCST}$	O	UBIU PROCESSING A BROADCAST COMMAND
101	$\overline{DBCSND}$	O	PULSES LOW IF A DYNAMIC BUS CONTROL MODE CODE IS RECEIVED IN RTU MODE
102	$\overline{ILLCMD}$	I	ILLEGAL COMMAND DETECTED FROM PROM
103	$\overline{ILLSUBADR}$	I	SUBADDRESS ERROR DETECTED FROM PROM
104	$\overline{GBT}$	O	GOOD BLOCK TRANSFERRED
105	$\overline{ERRLINE}$	O	PULSES LOW WHEN ANY TYPE OF ERROR IS DETECTED IN ANY OPERATING MODE
106	SA/ADR 3	O	BIT 3 OF SUBADDRESS FIELD OF COMMAND WORD IN RTU MODE BIT 3 OF ADDRESS FIELD OF COMMAND WORD IN BMU MODE
107	SA/ADR 1	O	BIT 1 OF SUBADDRESS
108	T/R	O	T/R BIT OF COMMAND WORD
109	S ANA GND	I	SECONDARY ANALOG GROUND
110	S DATA	I/O	SECONDARY SERIAL BUS INPUT/OUTPUT

LOGIC WAVEFORMS

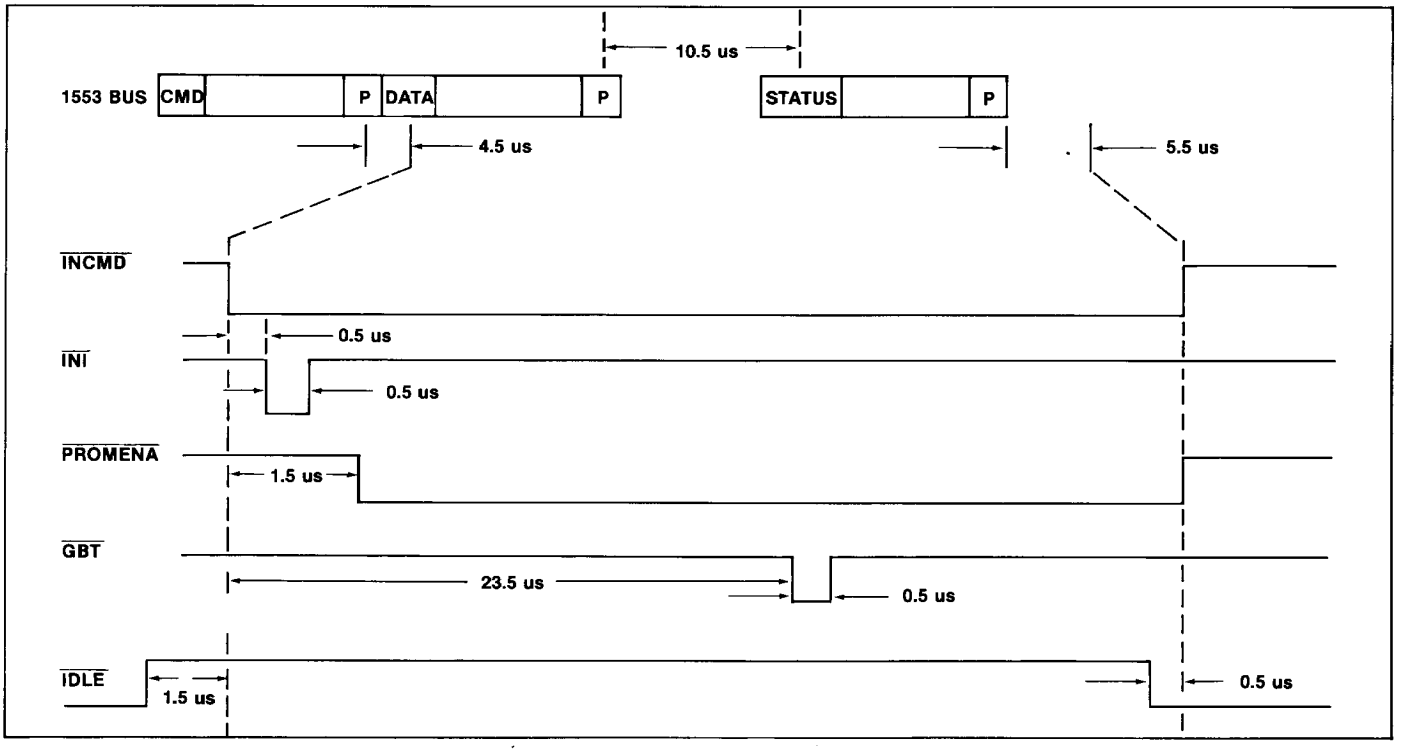


Figure 4a: Receive Timing Diagram—Remote Terminal Mode

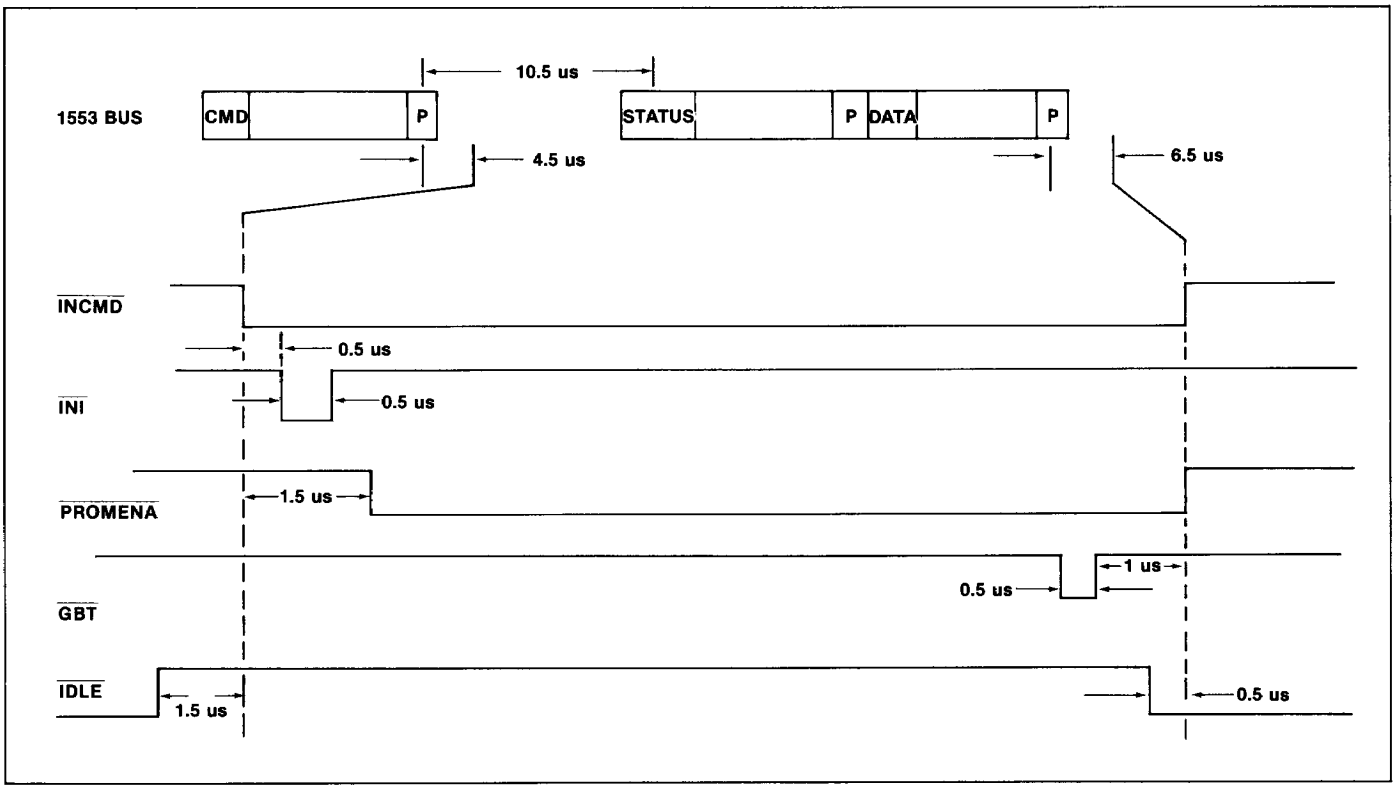


Figure 4b: Transmit Timing Diagram—Remote Terminal Mode

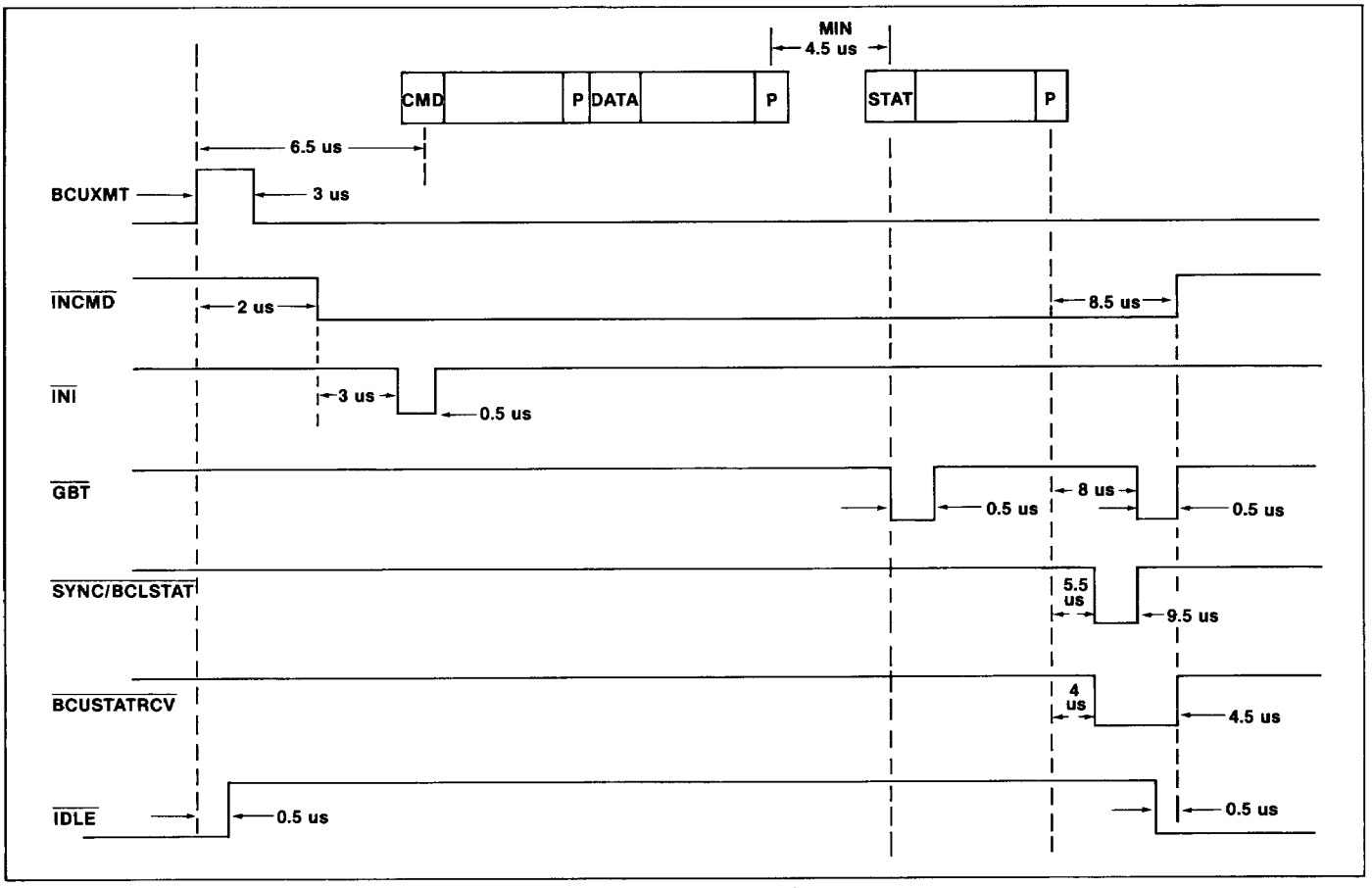


 Figure 4c: Receive Command—Bus Controller Mode

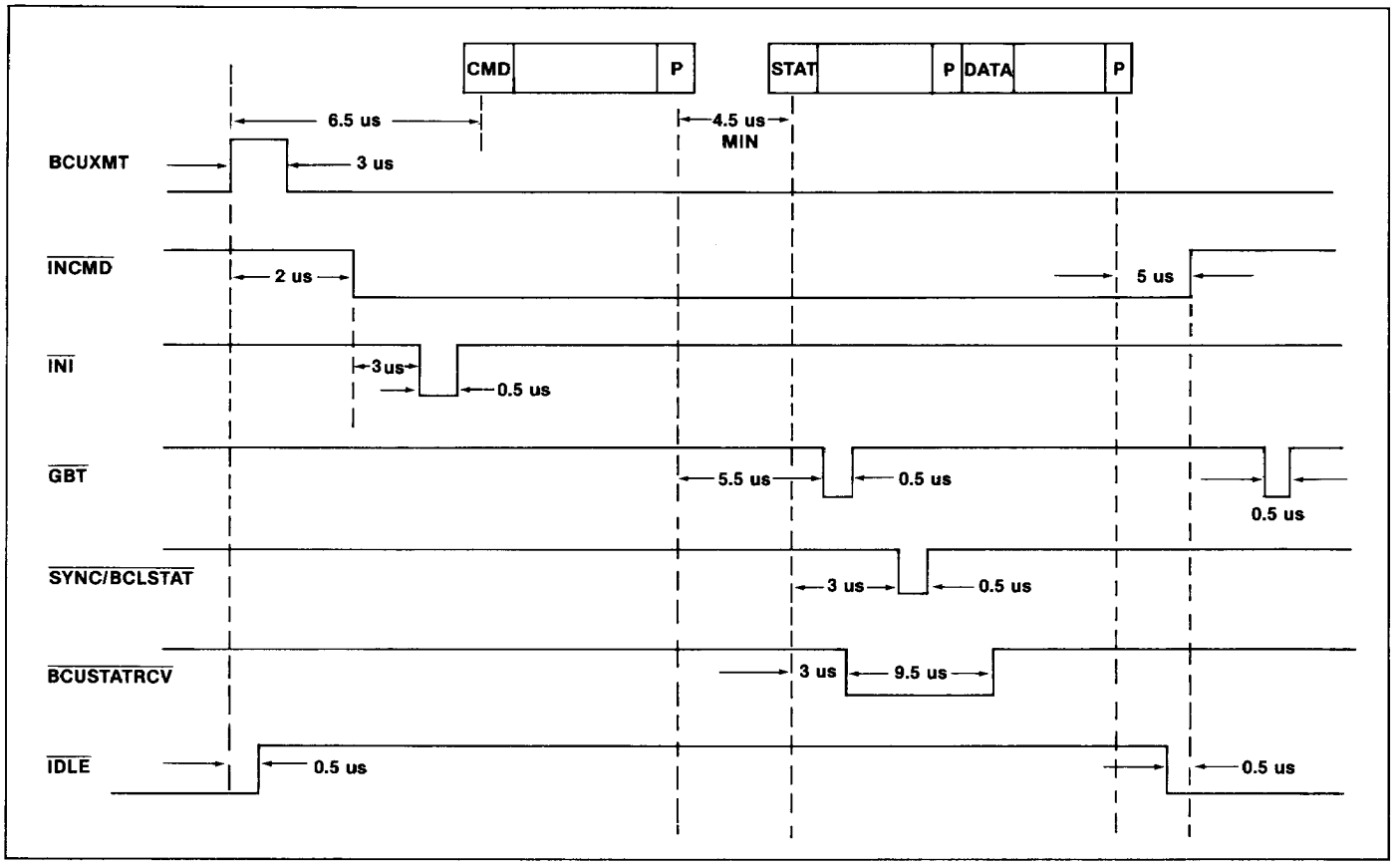


Figure 4d: Transmit Command—Bus Controller Mode

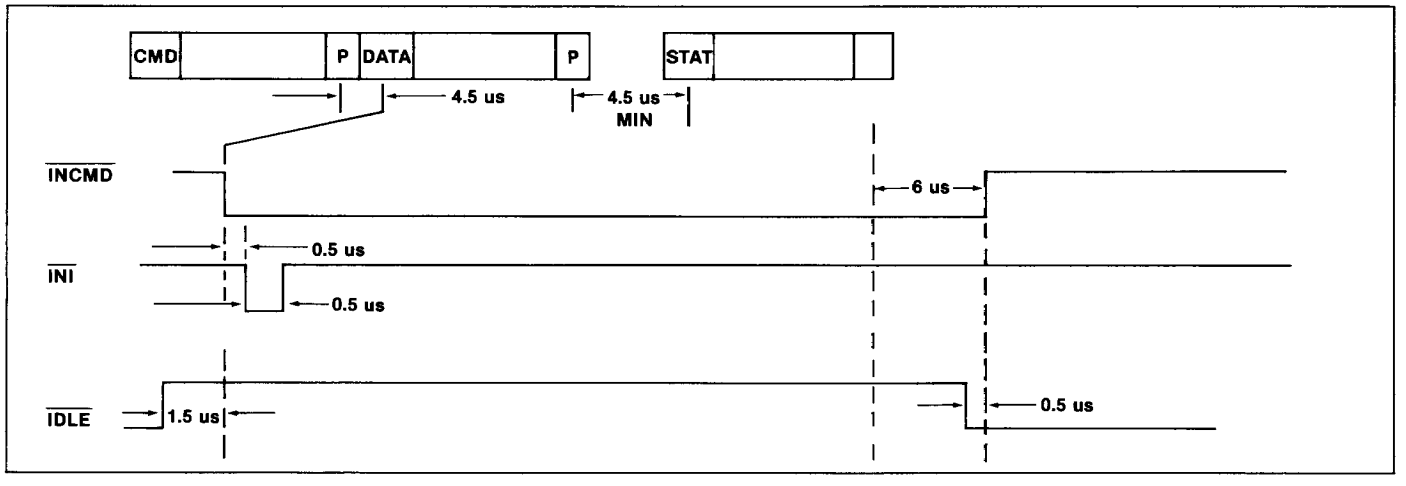


Figure 4e: Bus Monitor—Receive Message

LOGIC WAVEFORMS

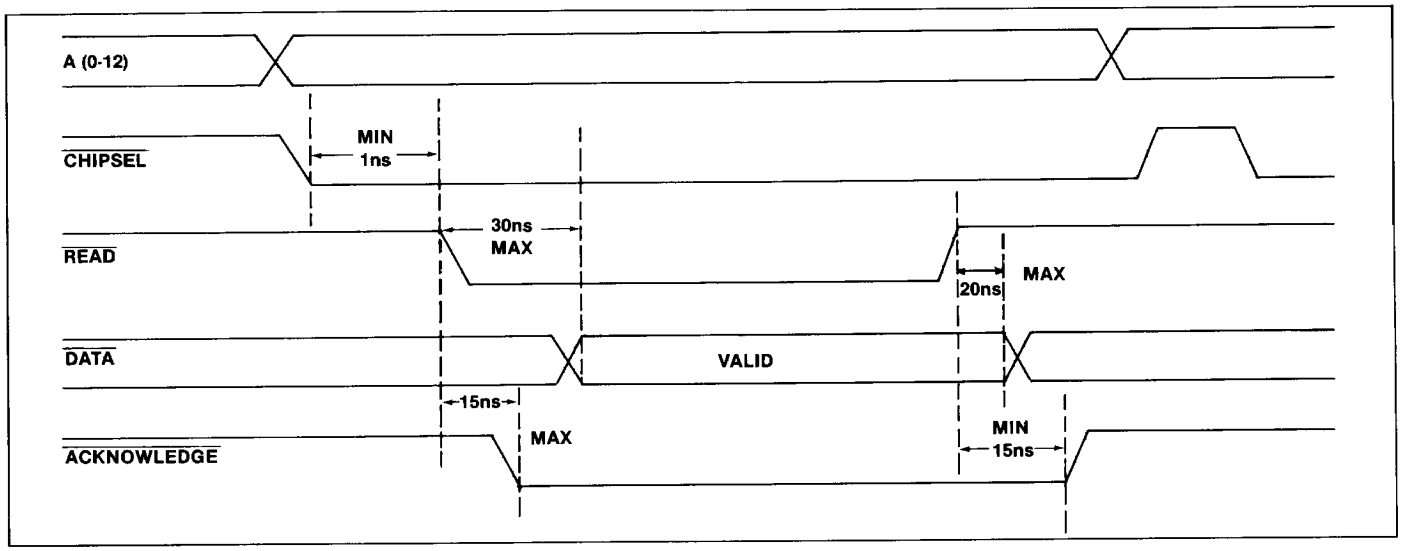


Figure 4f: Read Memory

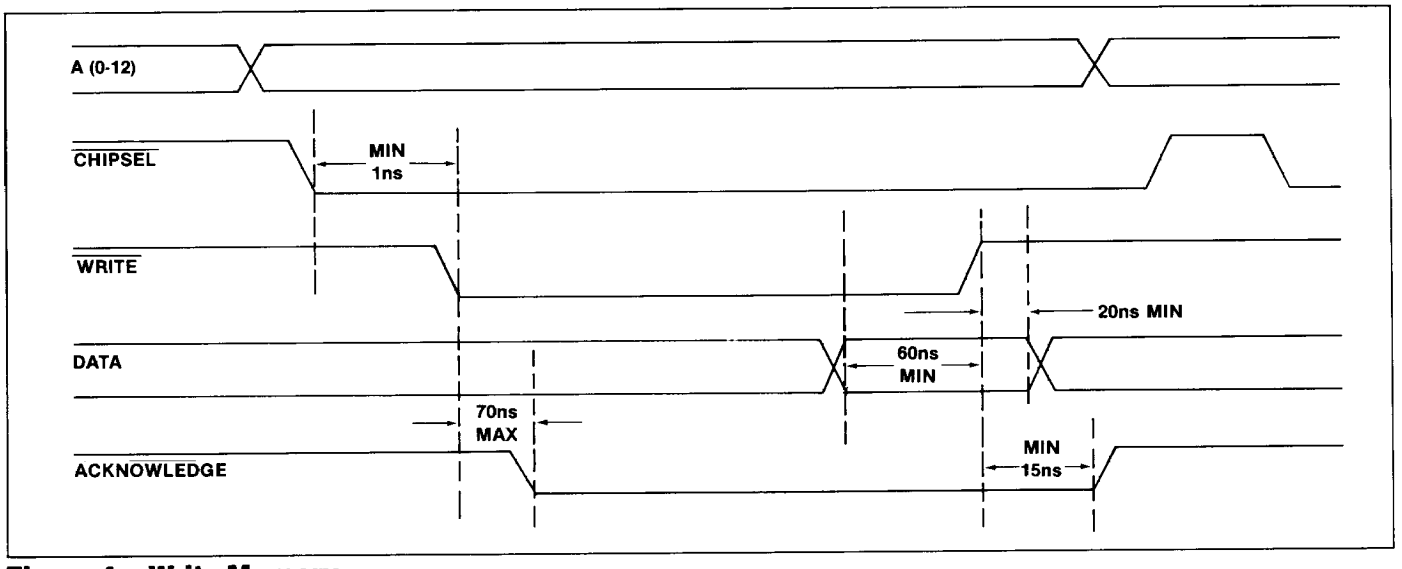


Figure 4g: Write Memory

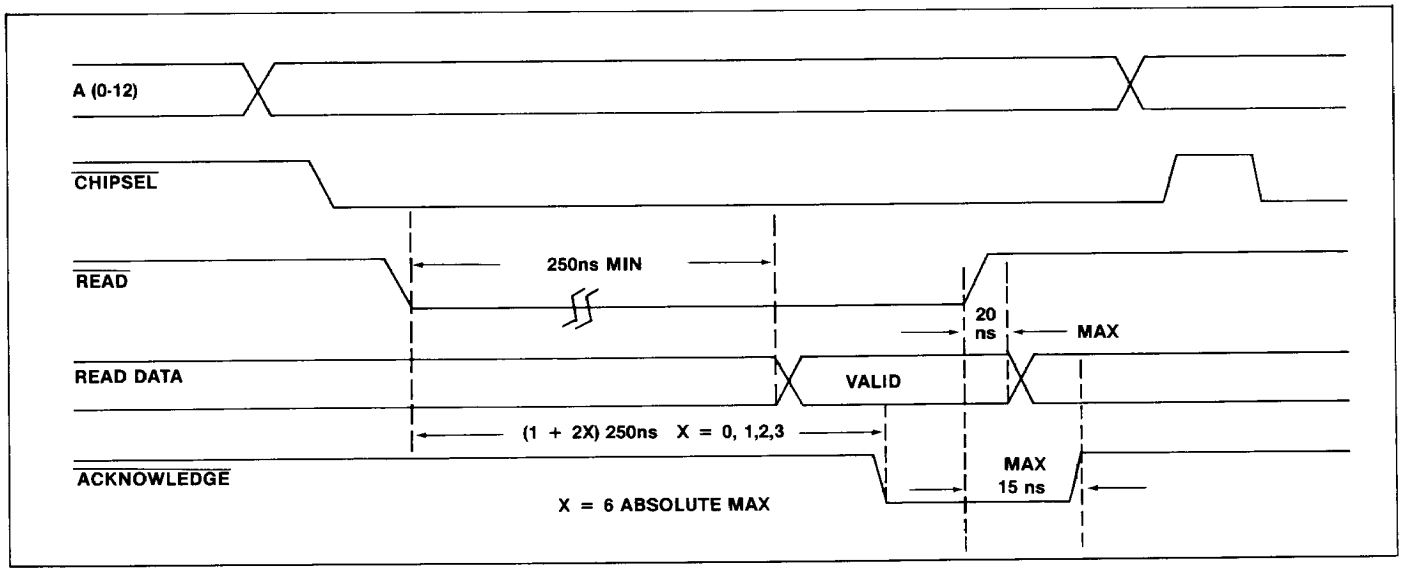


Figure 4h: MP Register Read

LOGIC WAVEFORMS

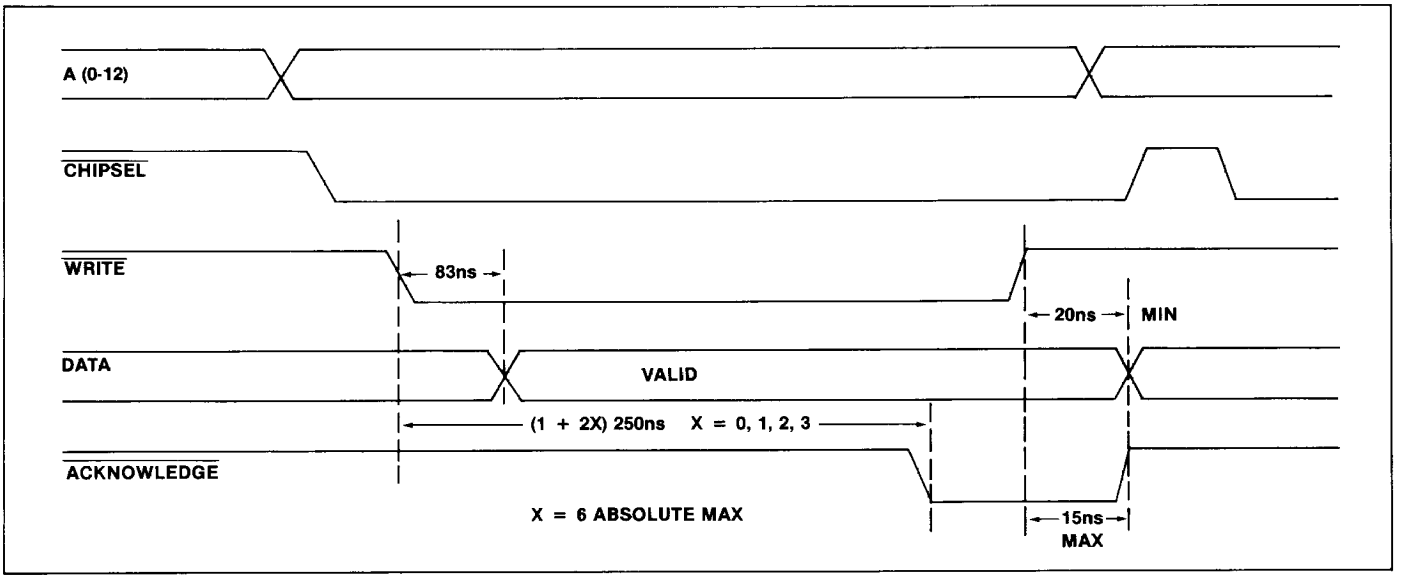


Figure 4i: MP Register Write

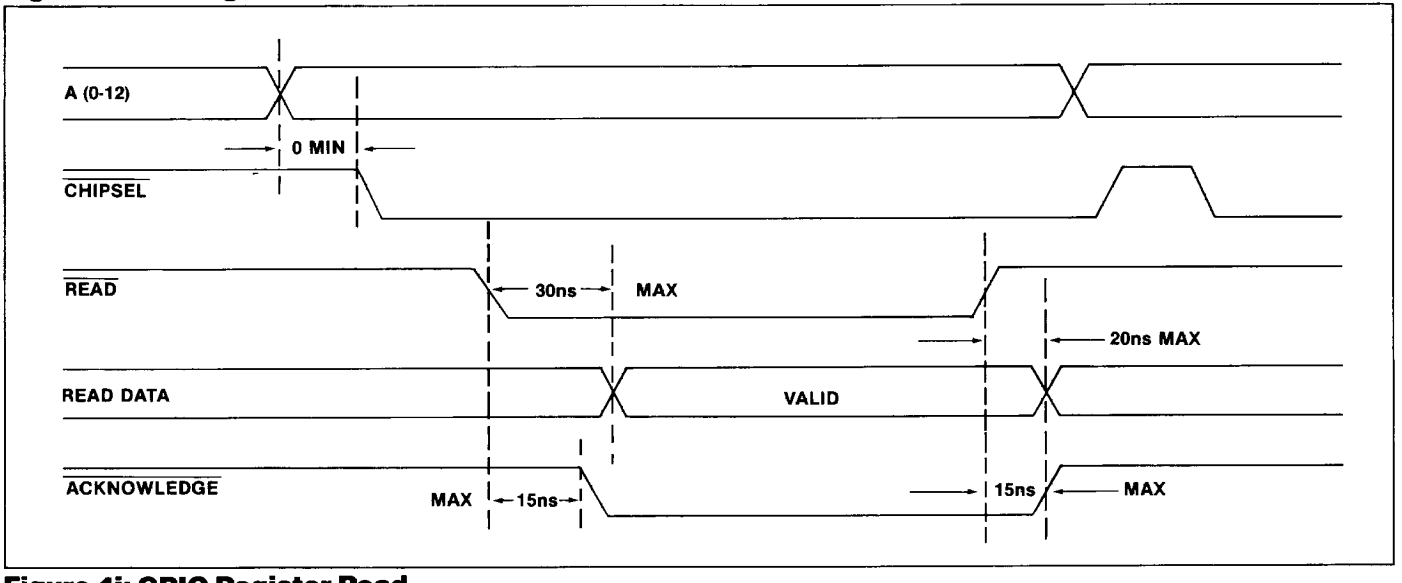


Figure 4j: GPIO Register Read

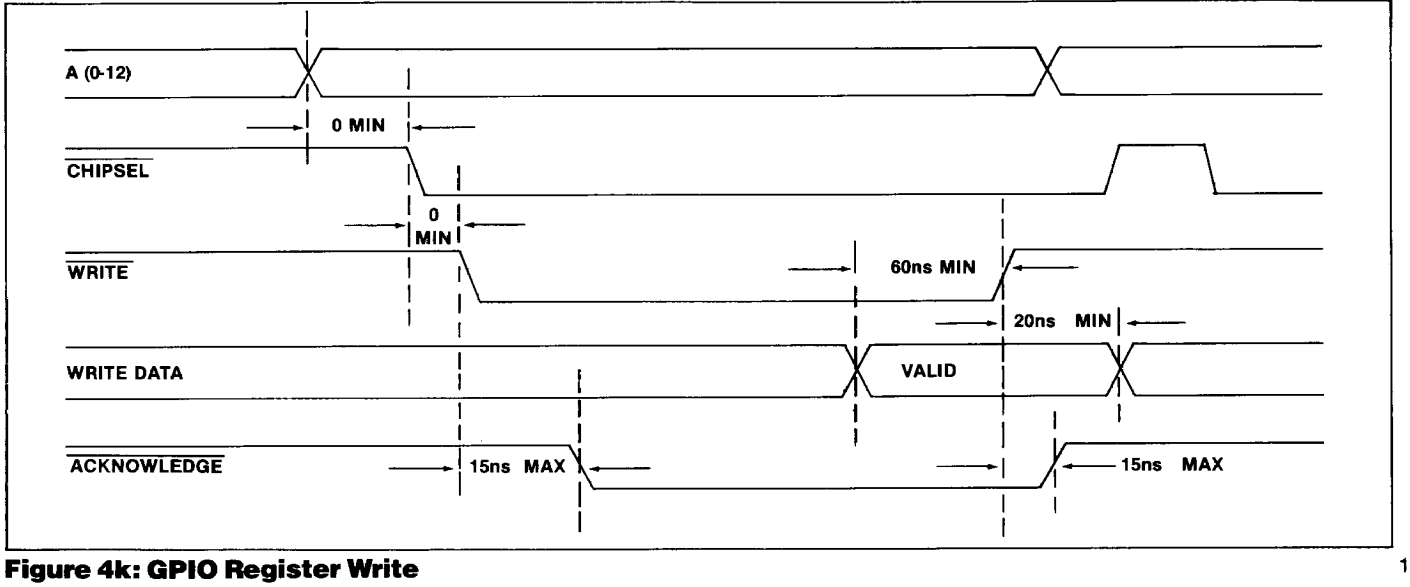


Figure 4k: GPIO Register Write

Terminal Address Lines

Addressing the five bit Terminal Address lines is done by hard wiring. Logic "0" lines must be tied to ground and logic "1" lines tied to +5V. Where logic lines cannot be tied to +5V pull-up resistors should be used (recommended value is 1 to 5 kohms). There is an Address Parity bit which must be used to establish odd parity.

DEVICE	N1:N2	N1:N3
ARX 2457	1:2.12	1:1.5
ARX 2447	1:1	1:.707
ARX 2427	1.4:1	2:1

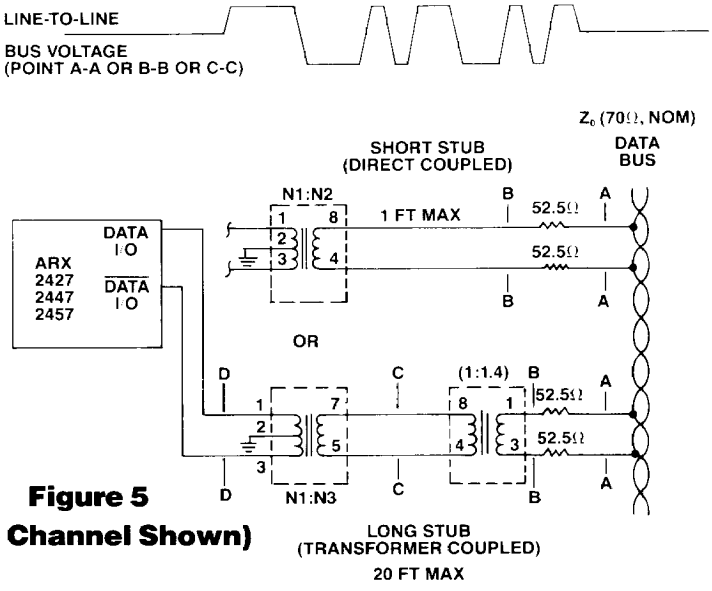


Figure 5
(One Channel Shown)

Ordering Information

ARX 2427	+5 V & ±15 V
ARX 2447	+5 V & ±12 V
ARX 2457	+5 V ONLY

Specifications subject to change without notice.

Memory Map Table

Address	RT Mode		BC Mode	BM Mode	
	STD	STACK		STD	STACK
17FE-17C0					Block 63
17BE-1780					
10FE-1000		Command Word Stack			
0FFE-0FC0	Sub 31 Tx	Block31-Tx		RT Add 31	Block 31
0FBE-0F80	Sub 31 Rec	Block30-Tx			
0F7E-0F40	Sub 30 Tx	Block29-Tx		RT Add 30	Block 30
0F3E-0F00	Sub 30 Rec	Block28-Tx			
087E-0840	Sub 16 Tx	Block 1-Tx		RT Add 16	Block 16
083E-0800	Sub 16 Rec	Block 0-Tx	RT/RT CMDS		
07FE-07C0	Sub 15 Tx	Block31-Rec		RT Add 15	Block 15
07BE-0780	Sub 15 Rec	Block30-Rec			
017E-0140	Sub 2 Tx	Block 5-Rec		RT Add 2	Block 2
013E-0100	Sub 2 Rec	Block 4-Rec			
00FE-00C0	Sub 1 Tx	Block 3-Rec		RT Add 1	Block 1
00BE-0080	Sub 1 Rec	Block 2-Rec			
007E-0040	Sub 0 Tx	Block 1-Rec	BC/RT CMDS	RT Add 0	Block 0
003E-0000	Sub 0 Rec	Block 0-Rec	RT/BC CMDS		

For Toll-Free inquiries call 1-800-THE-1553

AEROFLEX
An ARX Company

Aeroflex Laboratories Inc.
Microelectronics Division
35 South Service Road
Plainview, NY 11803
Tel. (516) 694-6700
TWX: 510-224-6417
FAX: (516) 694-6771

024517 ✓