

# Clock Mode Selection for MSC8126 Mask Set K98M

By Donald Simon and Wes Ray

This application note describes the MSC8126 clock modes for mask set K98M. It also describes a Microsoft® Excel application that assists users in determining the internal/external system clock frequencies generated by the input clock and a 5-bit MODCK value. Mask set K98M supports 27 valid clock modes, as tested using the 0K98M and 1K98M mask sets. The Excel application helps you to reduce design time significantly in two ways:

- Quickly determine whether an input clock frequency and clock mode combination violate frequency limitations.
- Evaluate a wide range of input clock frequencies to determine which combinations meet system requirements.

## CONTENTS

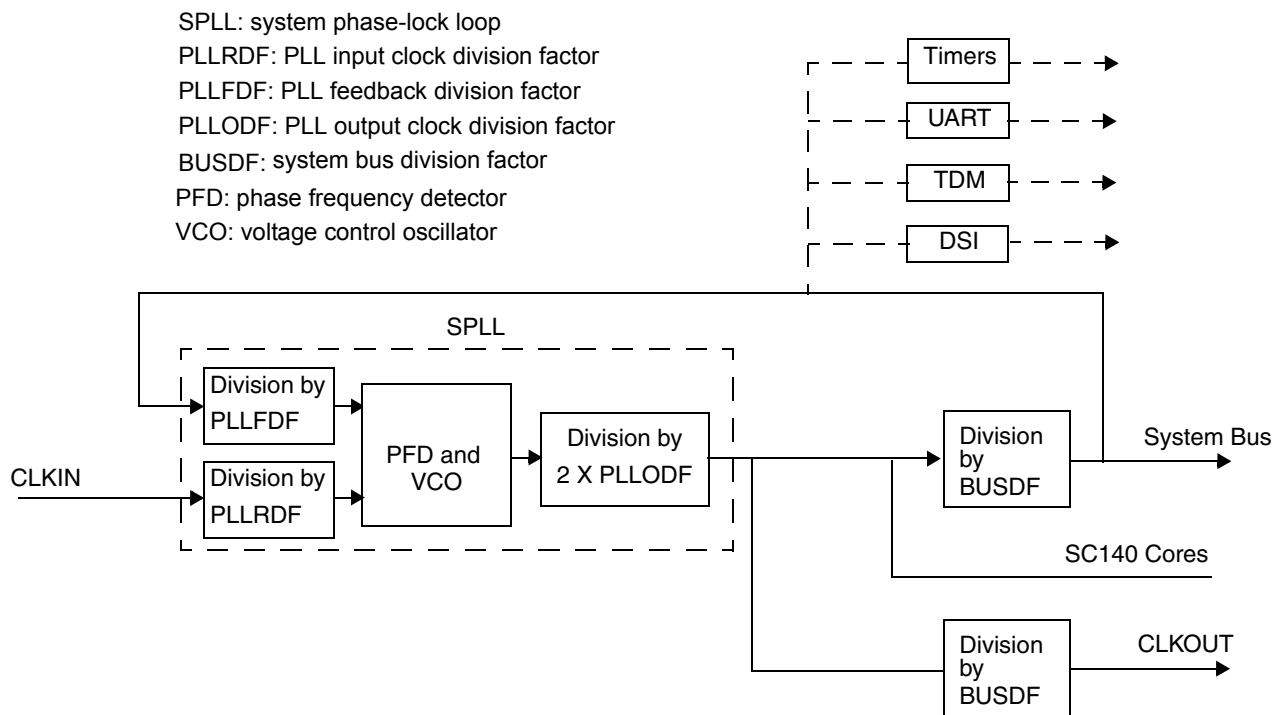
<b>1</b>	Mask Set .....	2
<b>2</b>	Clock Configuration .....	2
<b>3</b>	Clock Modes .....	3
<b>4</b>	Excel Application .....	4
<b>4.1</b>	Mask Set K98M Clock Mode Chart Worksheet .....	5
<b>4.2</b>	Mask Set K98M Clocking Scheme Worksheet .....	6
<b>5</b>	Excel Worksheet Quick Guide .....	7
<b>6</b>	Errata .....	7
<b>7</b>	Mask Set K98M Configuration Modes .....	7
<b>8</b>	References .....	8

# 1 Mask Set

Each MSC8126 device is labeled with a mask set number (for example mask set 1K98M).

## 2 Clock Configuration

**Figure 1** shows the functional clock block diagram for mask set K98M. The clock contains an internal system phase-lock loop (SPLL), bus division factor (BUSDF), clocks for the timers, universal asynchronous receiver/transmitter (UART), time-division multiplexer (TDM), and direct slave interface (DSI). The SPLL contains a phase-lock loop feedback division factor (PLLDF), a PLL input clock division factor (PLLRF), a phase frequency detector (PFD) and voltage control oscillator (VCO), and a PLL output clock division factor (PLLODF). All components in **Figure 1** are clock dividers except for the PFD and VCO.



**Figure 1.** MSC8126 Functional Clock Block Diagram for Mask Set K98M

The timers, UART, TDM, and DSI modules are shown as dotted lines in **Figure 1** because they can use clocks from sources other than the 60x-compatible system bus clock. The timer clock sources are selected by the Timer Configuration Registers, TCFRA and TCFRB. If the system bus clock is the source for the timer, the timer divider is always two. The timers can also be clocked by the GPIO signals, which are clocked separately from the timer interface to the IPBus. The UART baud rate is based on the system bus clock/  $(16 \times \text{SCIBR}[12-0])$ , where the SCIBR is the SCI Baud-Rate register. The TDM processes the data with the system bus clock. The maximum TDM data bit rate processing is limited to half of the system bus clock. Each TDM has three clock zones:

- The receiver is clocked by RCLKx.
- The transmitter is clocked by TCLKx.
- The interface to the local bus is clocked by the system bus clock.

The DSI has two clearly separated clock zones:

- The DSI interfaces with the external host asynchronously or via a synchronous interface clocked by the HCLKIN signal.
- The DSI interfaces with the internal local bus via the system bus clock.

For details on clocking for the timers, UART, TDM, and DSI, consult the *MSC8126 Reference Manual* (MSC8126RM). **Table 1** shows the maximum frequencies for the SC140 core and system bus for mask set K98M. You must ensure that the system design does not exceed these maximum frequencies.

**Table 1.** Mask Set K98M Maximum Frequency Limits

	MSC8126		
	300 MHz Device	400 MHz Device	500 MHz Device
SC140 cores frequency	300 MHz	400 MHz	500
System bus and CLKOUT	100 MHz	133.3 MHz	166.7
DSI clock frequency (HCLKIN)	70 MHz	70 MHz	70 MHz

### 3 Clock Modes

All MSC8126 devices use a 5-bit MODCK value to configure the clock mode. Refer to the clock mode chart in **Section 7** for valid settings for mask set K98M. The 5-bit MODCK value is determined at reset by sampling the following:

- Two multiplexed system pins (MODCK[1–2])
- MODCK\_H field in the Hard Reset Configuration Word (HRCW), corresponding to MODCK[3–5]

The MODCK\_H field defines the three most significant bits of the MODCK value. The MODCK[1–2] pins define the two least significant bits. The following example illustrates how the two sets of values define MODCK. The 5-bit values are organized for explanation purposes as one 3-bit and one 2-bit number: xxx-yy, where:

- xxx = MODCK\_H. Three clock mode high bits from the HRCW (bits 28–30) (MODCK[3–5]).
- yy = MODCK[1–2]. Two clock mode low bits from external inputs.

**Table 2** shows an example of how to derive the MODCK value from the MODCK\_H (aka MODCK[3–5]) and MODCK[1–2] values.

**Table 2.** Clock Mode Example

Input	MODCK Determination Example
HRCW[28–30] = 011	MODCK_H = 011
HD3/MODCK1 pin is pulled up	MODCK1 = 0
HD4/MODCK2 pin is pulled down	MODCK2 = 1

The example in **Table 2** corresponds to a MODCK value of 13: MODCK\_H-MODCK[1–2] = 011-01. The clock mode (MODCK) number is the decimal equivalent of the MODCK value read as a binary value:  $01101_2 = 13_{10} =$  clock mode 13. **Figure 2** shows an example with clock mode 13 for mask set K98M and the functional clock diagram assuming a 50 MHz input clock (CLKIN).

## Excel Application

SPLL: system phase-lock loop  
 PLLRDF: PLL's input clock division factor  
 PLLFDF: PLL's feedback division factor  
 PLLODF: PLL's output clock division factor  
 BUSDF: 60x bus division factor  
 VCO: voltage control oscillator

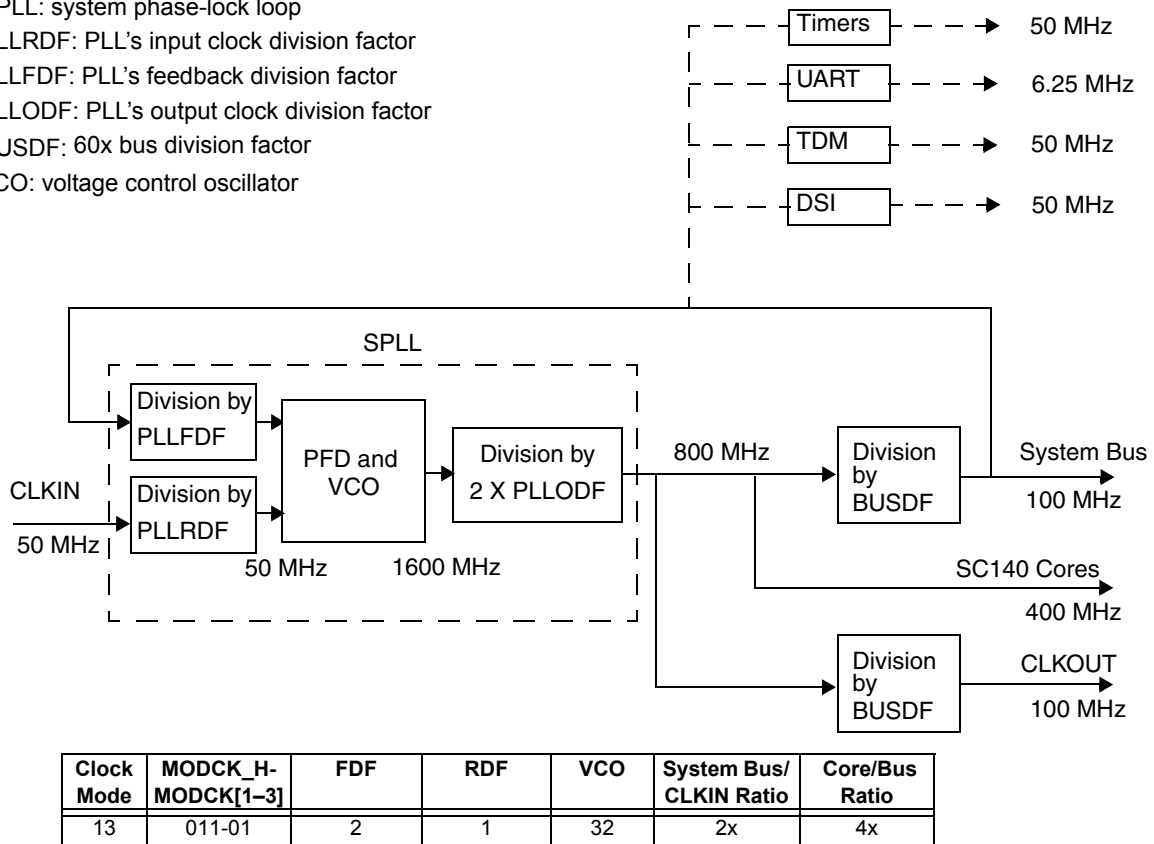


Figure 2. Mask Set K98M Clocking Example

## 4 Excel Application

This section explains how to use the Microsoft Excel file listed in **Table 3**.

Table 3. Mask Set K98M Excel File

MSC8126 Mask Set	Excel File Name
0K98M, 1K98M	MSC8126_Mask_Set_K98M.xls

When the Excel file in **Table 3** is opened, a window like that shown in **Figure 3** appears. Select **ENABLE MACROS** to enter the spreadsheet.

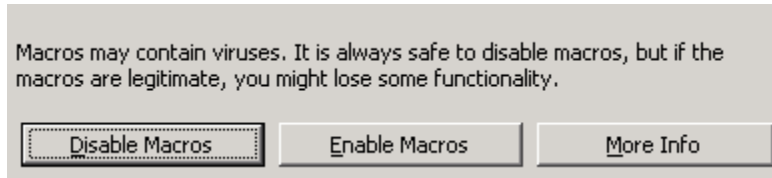


Figure 3. Opening Clock Spreadsheet in Excel

The Excel file contains the following two worksheets:

- *Clock Mode Chart*
- *Clocking Scheme*.

## 4.1 Mask Set K98M Clock Mode Chart Worksheet

Figure 4 show the *Clock Mode Chart* worksheet, which lists the valid clock modes for the mask set K98M. It requires two entries:

- **CLKIN (MHZ)** (cell C5)
- **MAX CORE FREQUENCY (MHZ)** (cell E6).

When the desired **CLKIN** frequency in MHz (input clock) and **MAX CORE FREQUENCY** in MHz are entered into cell C5 and E6, respectively, the other cell values in the worksheet update automatically. Only rows colored in yellow are valid. All values in red are invalid. Column R in the spreadsheet indicates whether the **CLKIN**, **MAX CORE FREQUENCY** frequency, and a specific clock mode constitute a valid combination.

The screenshot shows the 'Clock Mode Chart' worksheet in Microsoft Excel. The title bar indicates the file name: 'preliminary\_15Nov04\_MSC812x\_Mask\_Set\_K98M.xls'. The worksheet contains the following data:

Input fields:

- Cell C5: CLKIN (MHz): 50
- Cell E6: Max Core Frequency: 400

Summary Table:

Clock	Frequency (MHz)	
	Min	Max
CLKIN	20	133.3
F REF	20	133.3
F VCO	800	1600
CORES CLOCK	200	400
BUSES CLOCK	40	133.3
CLKOUT	40	133.3

Notes for table below:

- Rows in yellow are valid modes.
- Items in red are out of spec.

Detailed Clock Mode Selection Table:

Mode	MODCK	PLL	PLL	PLL	PLL	Bus	Bus / Clkin	Core / Bus	PLL FDF	PLL RDF (F REF)	F VCO	CORES CLOCK	BUSES CLOCK	
#	3-5	1-2	RDF	FDF	ODF	TP	DF	Ratio	Ratio	(MHz)	(MHz)	(MHz)	(MHz)	
0	000	00	2	2	2	5	3	1x	3x	25	25	600	150	50
1	000	01	1	2	2	5	3	2x	3x	50	50	1200	300	100
2	000	10	1	2	2	7	4	2x	4x	50	50	1600	400	100
3	000	11	1	4	1	7	4	4x	4x	50	50	1600	800	200
4	001	00	1	3	2	8	3	3x	3x	50	50	1800	450	150

Figure 4. Mask Set K98M Clock Mode Chart

## 4.2 Mask Set K98M Clocking Scheme Worksheet

Figure 5 displays the mask set K98M *Clocking Scheme* worksheet, which shows the various frequencies, dividers, and multipliers used in the MSC8126 clock module. It requires three entries:

- **CLKIN (MHz):** (cell C5)
- **Clock Mode:** (cell C6)
- **Max Core Freq:** (cell C7)

Figure 5 depicts an example with a clock in (CLKIN) value of 50 MHz (cell C5), a clock mode number of 13 (cell C6), and a max core frequency of 400 MHz (cell C7). Error messages are shown in cell A10. If there are no error messages, cell A10 is left blank. All values changed in the *Clock Mode Chart* worksheet do not change the *Clocking Scheme* worksheet, and vice versa.

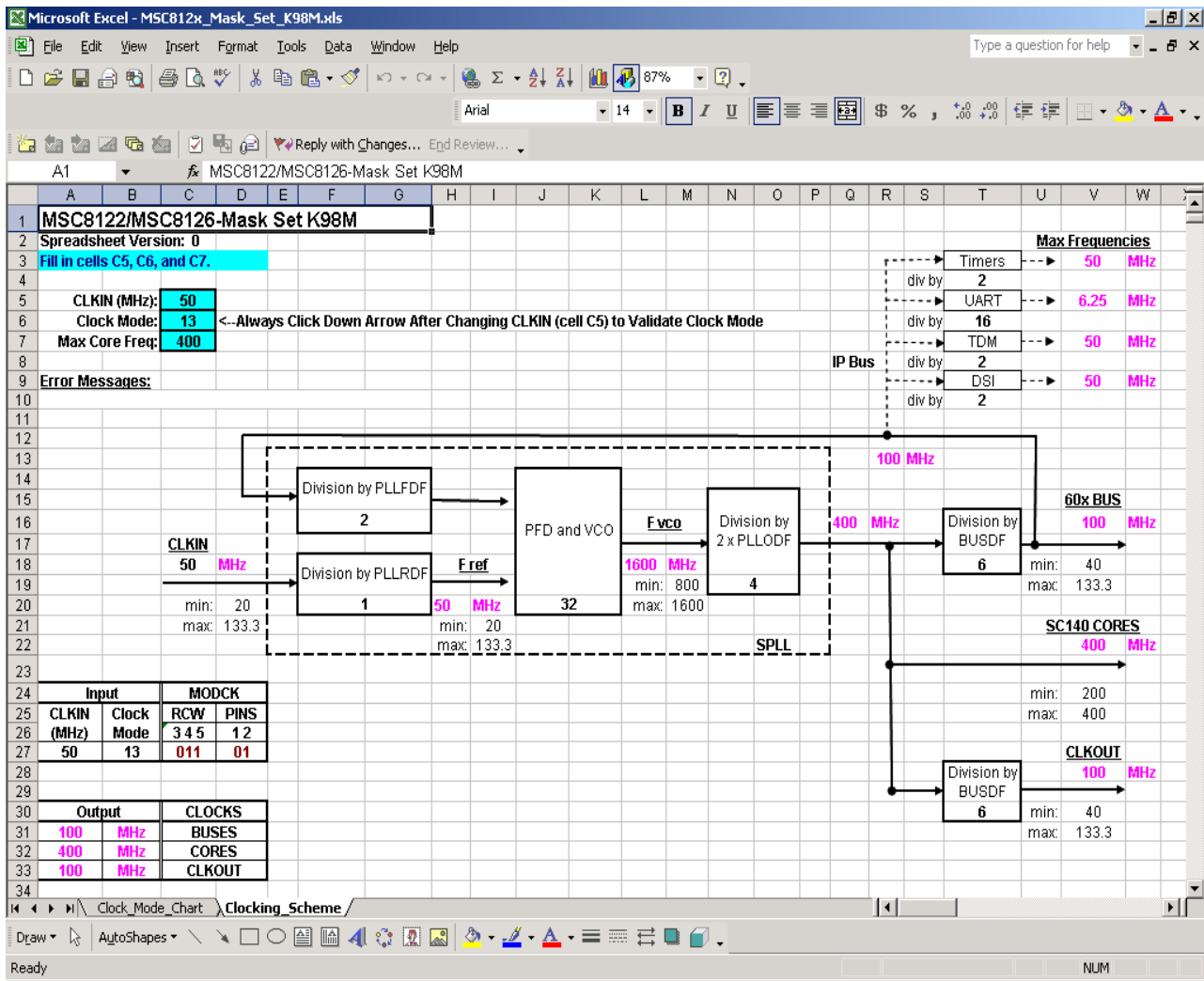


Figure 5. Mask Set K98M Clocking Scheme Worksheet Example

## 5 Excel Worksheet Quick Guide

Table 4 lists the steps for using the Excel worksheets.

**Table 4.** Excel Program Procedure

Step	Action	Comments
1	Start the Excel program and open the file that corresponds to the MSC8126 mask set.	Select MSC812x_Mask_Set_K98M.xls
2	Select a worksheet: <ul style="list-style-type: none"> <li>• Clock Mode Chart</li> <li>• Clocking Scheme</li> </ul>	If <i>Clock Mode Chart</i> is chosen, perform step 3A. If <i>Clocking Scheme Chart</i> is chosen, perform step 3B.
3A	For the <i>Clock Mode Chart</i> worksheet: <ul style="list-style-type: none"> <li>• Enter CLKIN frequency into cell C5.</li> <li>• Enter the maximum rated speed of the MSC8126 into cell E6.</li> <li>• Verify that there are no frequency violations in columns R and S.</li> </ul>	Refer to rows A22 through A55. Rows in yellow are valid modes. Items in red are out of spec.
3B	For the <i>Clocking Scheme</i> worksheet: <ul style="list-style-type: none"> <li>• Enter CLKIN frequency into cell C5.</li> <li>• Enter the Clock Mode number into cell C6.</li> <li>• Enter the maximum rated speed of the MSC8126 into cell C7.</li> <li>• Verify that there are no frequency or errata violations (cell A10).</li> </ul>	Refer to <b>Section 7</b> or the <i>Clock Mode Chart</i> worksheet for valid clock modes.  Cells A24 through D27 show the input values. Cells A30 through D33 show the output values.

When calculating clock frequencies, be sure to check the data sheet for the maximum/minimum input clock frequencies and the errata for limitations.

## 6 Errata

There are no known errata in the K98M mask set that impose clock limitations. For a complete list of errata, consult the Freescale web site listed on the back cover of this document.

## 7 Mask Set K98M Configuration Modes

Table 6 show the clock modes for mask set K98M and their respective bus/CLKIN and core/bus ratios.

**Table 5.** Clock Configuration Modes

Mode	MODCK[3–5] MODCK[1–2]	MSC8126	
		Bus/CLKIN Ratio	Core/Bus Ratio
0	000-00	1	3
1	000-01	2	3
2	000-10	2	4
3	000-11	4	4
4	001-00	3	3
5	001-01	4	3

**Table 5.** Clock Configuration Modes (Continued)

Mode	MODCK[3–5] MODCK[1–2]	MSC8126	
		Bus/CLKIN Ratio	Core/Bus Ratio
6	001-10	3	4
7	001-11	1	4
8	010-00	2	4
9	010-01	4	4
10	010-10	2	3
11	010-11	1.5	4
12	011-00	Reserved	
13	011-01	2	4
14	011-10	2	5
15	011-11	1	5
16	100-00	2	5
17	100-01	3	5
18	100-10	2	6
19	100-11	1	6
20	101-00	2	6
21	101-01	1	8
22	101-10	2	8
23	101-11	1	10
24	110-01	Reserved	
25	110-00	Reserved	
26	110-10	Reserved	
27	110-11	Reserved	
28	111-00	1	3
29	111-01	1	4
30	111-10	1	5
31	111-11	1	6

## 8 References

- MSC8126 *Technical Data*.
- MSC8126RM, *MSC8126 Reference Manual*.
- MSC8126UG, *MSC8126 User's Guide*.



---

**NOTES:**



**NOTES:**

---

**NOTES:**

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **E-mail:**

[support@freescale.com](mailto:support@freescale.com)

### **USA/Europe or Locations not listed:**

Freescale Semiconductor  
Technical Information Center, CH370  
1300 N. Alma School Road  
Chandler, Arizona 85224  
+1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GMBH  
Technical Information Center  
Schatzbogen 7  
81829 München, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064, Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor Hong Kong Ltd.  
Technical Information Center  
2 Dai King Street  
Tai Po Industrial Estate  
Tai Po, N.T. Hong Kong  
+800 2666 8080

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
P.O. Box 5405  
Denver, Colorado 80217  
1-800-441-2447 or 303-675-2140  
Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. StarCore is a trademark of StarCore LLC. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2004.