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Application Note
PowerPC Design Checklist

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This document describes the required connections of all the signals on a PowerPC microprocessor (MPC603, MPC75x, MPC74xx), microcontroller (MPC824x), or PCI bridge/memory controller (MPC10x). If a design follows these guidelines, has properly connected. It may be useful for performing schematic reviews or other design checks. This document contains the following topics:

To locate any published errata or updates for this document, refer to the website at http://www.motorola.com/semiconductors.

1.1 Introduction

The PowerPC processor and PCI bridge/memory controller family are all easy to design to, as long as some simple rules are followed regarding connections and pullups. For reference purposes, many designers refer to the application notes and example designs on the Motorola PowerPC website. This application note is a simple checklist that is useful before finalizing the design.

1.2 Connections

This section summarizes the connections and special conditions (such as pullups or pulldowns required) which may be needed for processors and memory controllers. Table 1 lists connections for the MPC603, MPC75x, MPC74x0 and MPC824x microprocessors/microcontrollers, while Table 2 lists connections for the MPC8240, MPC8245 and MPC107 microcontrollers/system controllers. The older MPC604 and MPC106 devices are not listed in the tables; the MPC603 and MPC107 entries are very similar and can be used instead.

In the tables, if a connection to a specific signal is not named, it may be one of the following terms:

- xx-yy OVDD — A pullup resistor to the OVDD power supply, with a value between xx and yy ohms.
- xx-yy GND — A pulldown resistor to the ground power connection, with a value between xx and yy ohms.
- “open” — The signal may/should be left unconnected.
- “as needed” — The connection is determined principally by the sysem.

Lastly, some of the signals have a “critical” designation:

May cause complete failure; board will likely not operate

This designator indicates signals which can cause system failure if not properly handled. If a new design is not running cycles (i.e., logic analyzer traces cannot be captured), the indicated signals should be checked first to determine if the conditions required are present. If not, due to design or manufacturing error, the part may be improperly configured into a test mode and will not operate as desired.

As an example, consider transfer start ($\overline{TS}$). On an MPC107-based design, if a pullup is not present, $\overline{TS}$ may float low, indicating to both the MPC107 and the CPU that another device is using the bus. Each will wait for the other to release $\overline{TS}$, and so the system will not start. A simple pullup insures that each device sees an idle bus.

Table 1. Processor Connections

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC824X	Connection		Notes
							if used	if not used	
	A(0:31)	✓	✓	✓	✓		as needed		Address bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted. 74x0 in address bus drive mode (see EMODE) does not need pullups in either case.
✋	$\overline{\text{AACK}}$	✓	✓	✓	✓		1K-10K OVDD		Pullup needed to insure initial startup.
✋	$\overline{\text{ABB}}$	✓	✓	✓			1K-10K OVDD		Not needed for MPC10x-based systems.
	$\overline{\text{ABB}}$/AMON0				✓		as needed	open	The MPC7400 does not check $\overline{\text{ABB}}$; it is an output only. A pullup may be used where MPC75x/MPC74x0 footprint compatibility is needed.
	AP(0:3)	✓	✓	✓	✓		as needed	1K-10K OVDD	Address parity may be pulled up if unused to minimize sleep-mode power consumption; otherwise, pullups may be omitted.
	$\overline{\text{APE}}$	✓	✓	✓			1K-10K OVDD	open	Open-drain output; pullup only if needed.
	$\overline{\text{ARTRY}}$	✓	✓	✓	✓		1K-10K OVDD		Pullup needed to insure initial startup.
✋	AVDD	✓	✓	✓	✓	✓	filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical). Avoid routing near noisy traces.
	$\overline{\text{BG}}$	✓	✓	✓	✓		as needed	100-1K GND	Pullup recommended for initial startup, or pulldown for permanently parked address bus.
✋	$\overline{\text{BR}}$	✓	✓	✓	✓		100-1K OVDD		Pullup needed to insure initial startup.
✋	BVSEL				✓		GND, HRESET or OVDD		Connect to: GND for: 1.8V OVDD HRESET “2.5V OVDD OVDD “3.3V OVDD for the MPC755 or MPC74xx, or as described in the hardware specification.
	$\overline{\text{CI}}$	✓	✓	✓	✓		as needed	1K-10K OVDD	$\overline{\text{CI}}$ may be pulled up to minimize sleep-mode power consumption; otherwise, pullup may be omitted.
	$\overline{\text{CKSTP\_IN}}$	✓	✓	✓	✓	✓	1K-10K OVDD		The $\overline{\text{CKSTP\_IN}}$ pullup may be shared with others if not used.
	$\overline{\text{CKSTP\_OUT}}$	✓	✓	✓	✓		1K-10K OVDD	open	$\overline{\text{CKSTP\_OUT}}$ is an open-drain output.
	CLK_OUT	✓	✓	✓	✓	✓	to testpoint	open	CLK_OUT is useful only for debugging, it cannot be used as a clock source.
	CSE(0:1)	✓					as needed	open	Output-only debug status; rarely used, connect to logic analyzer or float.
	$\overline{\text{DBB}}$	✓	✓	✓			1K-10K OVDD		Not needed for MPC10x-based systems.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC824X	Connection		Notes
							if used	if not used	
	DBB/DMON0				✓				DBB is an output only on the MPC74x0. A pullup may be used where MPC75x-MPC74x0 footprint compatibility is needed.
	DBG	✓	✓	✓	✓		as needed	100-1K GND	Pullup recommended for initial startup, or pulldown for permanently parked data bus.
✋	DBDIS	✓	✓	✓			1K-10K OVDD		Rarely used signal; must be pulled up. Can be shared with other pullups.
✋	DBWO	✓	✓	✓			1K-10K OVDD		Rarely used signal; must be pulled up. Can be shared with other pullups.
	DH(0:31) DL(0:31)	✓	✓	✓	✓		as needed	open	Connect only to other CPUs, local-bus I/O and bridge devices. Memory is typically on the other side of buffers (MPC106) or the MDH/MDH bus. For 32-bit bus mode, DL(0:31) may be left open with no pullups required.
	DP(0:7)	✓	✓	✓	✓		as needed	open	Pullups are not needed if parity is unused.
	DPE	✓	✓	✓			1K-10K OVDD	open	Open-drain output; pullup only if needed.
	DRDY				✓		as needed	open	MPX bus mode output only.
✋	DRTRY	✓	✓	✓			1K-10K OVDD	tie to HRESET	Tie DRTRY to HRESET to set NO-DRTRY mode. NO-DRTRY mode improves performance by eliminating an idle bus clock cycle after data transfers. DRTRY must not be tied to ground to enable NO-DRTRY mode.
	DTI(0:2)				✓		1K-10K OVDD		MPX bus mode only; pullups allow use of MPC750-devices.
	EMODE				✓		as needed	1K-10K OVDD	Connect as follows: pullup 60X bus mode HRESET MPX bus mode pulldown MPX bus mode with address bus drive mode.
	GBL	✓	✓	✓	✓		as needed	1K-10K OVDD	GBL may be pulled up to minimize sleep-mode power consumption; otherwise, pullup may be omitted.
	HIT				✓		as needed	open	MPX bus mode output only.
✋	HRESET HRST_CPU	✓	✓	✓	✓	✓	assert >= 255 bus clocks		A longer interval is acceptable, and may be needed for other devices such as the MPC10X.
✋	HRST_CTRL					✓	as needed		HRST_CTRL should be tied to HRST_CPU.
	INT	✓	✓	✓	✓		1K-10K OVDD		Pullup may be shared with others if INT not used.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC824X	Connection		Notes
							if used	if not used	
✋	L1_TSTCLK	✓	✓	✓	✓			100 - 1K OVDD	Use a strong pullup to keep noise from coupling to this pin. Do not share with other input-only pullups since asserting L1_TSTCLK during $\overline{\text{HRESET}}$ may be needed to correct errata on some devices.
	L2ADDR(16:0)		✓	✓	✓		SRAM A(16:0)	open	The L2ADDR(16:0) bus is little endian, connect to similar SRAM names.
	L2ADDR17			✓	✓		SRAM A17	open	L2ADDR17 can be used for larger SRAM
	L2ASPARE				✓		SRAM A18	open	L2ASPARE may be used for larger SRAM
✋	L2AVDD		✓	✓	✓		filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD), through a 10 ohm resistor, with two 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical).
	$\overline{\text{L2CE}}$		✓	✓	✓		SRAM SE1	open	Directly drives SRAM $\overline{\text{SE1}}$ pin. SE2 is typically tied high and $\overline{\text{SE3}}$ tied low.
	L2CLK_OUTA L2CLK_OUTB		✓	✓	✓		SRAM CLK	open	Traces must be point-to-point and equal length, equal to other SRAM trace lengths. For differential mode route using a split-T configuration.
	L2DATA(0:63)		✓	✓	✓		SRAM D(0:63)	open	L2 data bits can be rearranged at will to make routing better.
	L2DP(0:7)		✓	✓	✓		SRAM DP(0:7)	open	L2DP data bits can be rearranged at will to make routing better.
	L2SYNC_IN L2SYNC_OUT		✓	✓	✓		feedback		Connect L2SYNC_IN to L2SYNC_OUT with a trace length equal to that of the L2CLK_OUTA. If L2 is not used, the feedback loop is still required.
	L2VSEL				✓		GND, HRESET or OVDD		Connect to: GND for: 1.8V L2OVDD HRESET “2.5V L2OVDD OVDD “3.3V L2OVDD for the MPC755 or MPC74xx, or as described in the hardware specification.
✋	L2_TSTCLK	✓	✓	✓	✓			100-1K OVDD	Use a strong pullup to keep noise from coupling to this pin.
	$\overline{\text{L2WE}}$		✓	✓	✓		SRAM SGW	open	Directly drives SRAM $\overline{\text{SGW}}$ (global write) pin. $\overline{\text{SBW(AD)}}$ and $\overline{\text{SW}}$ are typically grounded.
	L2ZZ		✓	✓	✓		SRAM ZZ	open	Directly drives SRAM ZZ pin.
✋	$\overline{\text{LSSD\_MODE}}$	✓	✓	✓	✓			100-1K OVDD	Use a strong pullup to keep noise from coupling to this pin.
	$\overline{\text{MCP}}$	✓	✓	✓	✓	✓	as needed	1K-10K OVDD	Pullup may be shared with others if $\overline{\text{MCP}}$ not used.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC824X	Connection		Notes
							if used	if not used	
✋	NC	✓	✓	✓	✓	✓	open	open	Never connect anything to a NC pin unless it is defined on an upwardly compatible footprint (for upgrade purposes). For example, L2ADDR17 is NC on some BGA footprints; it is acceptable to connect this NC pad to an SRAM address line.
	PCI_SYNC_IN					✓	as needed		Clock input traces should match those for other PCI devices. Connect to PCICLK if PCI clock tree is not used.
	PLL_CFG(0:3)	✓	✓	✓	✓		as needed		Pullups and pulldowns, jumpers to OVDD and GND, or digital logic may be used.
	PLL_CFG(0:4)					✓	as needed		Only pullups and pulldowns should be used. Jumpers to OVDD and GND, or digital logic, may be used only if debug mode is NEVER enabled.
	$\overline{\text{QACK}}$	✓	✓	✓	✓	✓	1K-10K GND; HRESET logic	1K-10K GND	COP emulators require $\overline{\text{QACK}}$ asserted to single-step. 603 devices require $\overline{\text{QACK}}$ asserted during $\overline{\text{HRESET}}$ to prevent reduced-bus mode.
	$\overline{\text{QREQ}}$	✓	✓	✓	✓		as needed	open	Output typically used only with MPC10X and/or COP interface.
	$\overline{\text{RSRV}}$	✓	✓	✓	✓		as needed	open	$\overline{\text{RSRV}}$ is a little-used output-only pin.
	SCK					✓	1K-3K OVDD	open	SCK is open drain.
	SDA					✓	1K-3K OVDD	open	SDA is open drain.
	$\overline{\text{SHD(0:1)}}$				✓		1K-10K OVDD	open	In 60X mode, SHD pins are ignored; otherwise pullup if used.
	$\overline{\text{SMI}}$	✓	✓	✓	✓	✓	1K-10K OVDD		Pullup may be shared with others if $\overline{\text{SMI}}$ not used.
	$\overline{\text{SRESET}}$	✓	✓	✓	✓	✓	as needed	1K-10K OVDD	$\overline{\text{SRESET}}$ need not be asserted during power-up reset.
	SYSCLK	✓	✓	✓	✓		as needed		Clock input traces should match those for other PowerPC-bus devices.
✋	$\overline{\text{TA}}$	✓	✓	✓	✓		1K-10K OVDD		Pullup needed for initial startup.
	$\overline{\text{TBEN}}$	✓	✓	✓	✓	✓	as needed	1K-10K OVDD	May be pulled down to disable TBU/TBL/DEC registers (rarely useful).
	$\overline{\text{TBST}}$	✓	✓	✓	✓		1K-10K OVDD		Pullup needed for initial startup.
	TC(0:1)	✓					as needed	open	TC outputs indicate data vs. instruction cycles for 603 only. Commonly used for logic analyzer headers (compare with $\overline{\text{WT}}$ for 75x processors and TT[0] for 74x0 processors).
	TCK	✓	✓	✓	✓	✓	as needed	open	TCK has a weak (>=20KΩ) internal pullup.
	TDI	✓	✓	✓	✓	✓	as needed	open	TDI has a weak (>=20KΩ) internal pullup.
	TDO	✓	✓	✓	✓	✓	as needed	open	TDO has a weak (>=20KΩ) internal pullup.

Table 1. Processor Connections (Continued)

Critical	Signal	MPC603	MPC750	MPC755	MPC74X0	MPC824X	Connection		Notes
							if used	if not used	
✋	TEA	✓	✓	✓	✓	✓	1K-10K OVDD		Pullup needed for initial startup.
✋	TEST0					✓		100-1K OVDD	Use a strong pullup to keep noise from coupling to this pin.
	TLBISYNC	✓	✓	✓			assert during HRESET if needed	1K-10K OVDD	TLBISYNC selects 32-bit bus mode on 60X devices; assert during HRESET if needed. TLBISYNC must be pulled up on the MPC750. TLBISYNC on the MPC7400 is not supported, so pull it up.
	TMS	✓	✓	✓	✓	✓	as needed	open	TMS has a weak (>=20KΩ) internal pullup.
✋	TRST	✓	✓	✓	✓	✓	actively drive with HRESET and source	100-1K GND	TRST has a weak (>=20KΩ) internal pullup, but do not leave it floating or pulled up. TRST must be asserted to initialize the boundary scan chain. If COP is not used, a pulldown is sufficient. If COP is used, use discrete logic to merge the COP TRST source and the target system HRESET.
✋	TS	✓	✓	✓	✓		1K-10K OVDD		Pullup needed for initial startup.
	TSIZ(0:2)	✓	✓	✓	✓		as needed		TSIZ bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted.
	TT(0:4)	✓	✓	✓	✓		as needed		TT bus may be pulled up to minimize sleep-mode power consumption; otherwise, pullups may be omitted. TT0 indicates instruction vs. data information for debugging on MPC74x0.
	VOLTDET	✓	✓	✓			as needed	open	VOLTDET definition varies by device; may be connected to GND, OVDD, or VDD (core) depending on device and mask revision.
	WT	✓	✓	✓	✓		as needed	1K-10K OVDD	WT may be pulled up to minimize sleep-mode power consumption; otherwise, pullup may be omitted. WT indicates instruction vs. data information for debugging on MPC75x (only).

Table 2 lists only the memory/PCI/system controller signals of the devices, not the 60X bus signals (if any). For example, the MPC107 does not have an entry for the TS signal, since TS should already have been properly handled in Table 1 when the (required) PowerPC CPU is connected.

Table 2. Memory/PCI/System Controller Connections

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	AD(31:0)	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If the PCI port is not used, the bus must be pulled up or the PCI bus parked.
✋	AVDD	✓	✓	✓	filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical).
✋	AVDD2		✓	✓	filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical).
	$\overline{\text{C/BE(3:0)}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	CKE	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal. If low-power is not a concern, CKE can be wired to '1' at the SDRAM device and the CKE can be left open.
✋	CPU_CLK(0:2)	✓			as needed	open	CPU_CLK signals must have trace length added to match any delay on the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback path. Refer to the MPC107 Design Guide (AN1849/D) for details.
	$\overline{\text{CS(0:7)}}$	✓	✓	✓	SDRAM $\overline{\text{CS}}$	open	Standard SDRAM control signal. Each $\overline{\text{CS(0:7)}}$ pin must control one 64-bit (or 32-bit) array of memory. Each SODIMM or DIMM will have one or two arrays of memory on it with one, two or four usable chip-selects. Standard wiring is: SODIMM (64 only):One $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS0}}$, second $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS1}}$. DIMM (as 64-bits):One $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS0}}$ and $\overline{\text{CS2}}$, second $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS1}}$ and $\overline{\text{CS3}}$. DIMM (as 32-bits):One $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS0}}$, second $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS2}}$, third $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS1}}$, fourth $\overline{\text{CS(0:7)}}$ to $\overline{\text{CS3}}$.
	CTS1			✓	RS232 receiver	1K-10K OVDD	RS232 signal: Clear to send.
	$\overline{\text{DEVSEL}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	DQM(0:7)	✓	✓	✓	SDRAM DQ(0:7)	open	Each DQM must be associated with corresponding MDH/MDL byte lanes: DQM0⮜-⮞MDH(0:7) DQM1⮜-⮞MDH(8:15) DQM2⮜-⮞MDH(16:23) DQM3⮜-⮞MDH(24:31) DQM4⮜-⮞MDL(0:7) DQM5⮜-⮞MDH(8:15) DQM6⮜-⮞MDH(16:23) DQM7⮜-⮞MDH(24:31) If an 8-bit SDRAM device is attached to MDH(0:7), then DQM0 should be connected to the DQM pin, and so forth. Any parity SDRAM devices can use any DQM(0:7) signal (it will have to share).
	$\overline{\text{FOE}}$	✓	✓	✓	as needed	open	$\overline{\text{FOE}}$ is not needed if non-writable devices (PROM) is used for the boot code (or if the boot code is on PCI).
	$\overline{\text{FRAME}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	$\overline{\text{GNT}}(4:0)$	✓	✓	✓	as needed	GNT0: 1K-10K LVDD, others open	If the arbiter is disabled, $\overline{\text{GNT0}}$ becomes “REQ” and should be pulled up on a PCI motherboard or private PCI bus.
✋	IDSEL	✓	✓	✓	one of AD(31:0)	GND	IDSEL should be connected to GND for host systems and to one address line of AD(31:0) for agent systems. If the PCI port is not used, it should be grounded.
	$\overline{\text{INTA}}$				as needed	open	In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller. In host mode, $\overline{\text{INTA}}$ may be used to assert interrupts to other devices, such as a second processor.
	$\overline{\text{IRDY}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	$\overline{\text{IRQ}}(0:4)$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	$\overline{\text{INT}}(0:4)$ should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card.
✋	LAVDD	✓	✓	✓	filtered VDD		Must be connected to core voltage (VDD), not I/O (OVDD) through a 10 ohm resistor, with (2) 2.2uF ceramic caps on the AVDD pin. Trace lengths should be short, but do not need to be thick (~15mW typical).

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	$\overline{\text{LOCK}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	MAA(0:2)		✓	✓	to logic analyzer	open	MAA assists logic analyzers in recovering addressing information
	MDH(0:31) MDL(0:31)	✓	✓	✓	as needed		All flash, SDRAM/DRAM, and PortX I/O devices connect to MDH/MDL, not to the DH/DL processor data bus (if any).
	$\overline{\text{MIV}}$		✓	✓	to logic analyzer	open	$\overline{\text{MIV}}$ assists logic analyzers in recovering addressing information
	OSC_IN	✓	✓	✓	1K-10K OVDD	1K-10K OVDD	OSC_IN recommended only for embedded host systems, not for PCI agent cards due to clock skew.
	PAR(0:7)	✓	✓	✓	as needed	open	All flash, SDRAM/DRAM, and I/O devices connect to PAR(0:7), not to the DH/DL processor data bus (if visible). For Flash and I/O, PAR(0:7) is used for addressing, not flash or I/O parity.
	PAR	✓	✓	✓	as needed	1K-10K LVDD	PAR should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	PCI_CLK(0:4)	✓	✓	✓	as needed	open	PCI clocks to target PCI devices should have equal lengths. If not used, disable clock drivers in the CDCR register.
✋	PCI_SYNC_IN	✓	✓	✓	PCI_SYNC_OUT		PCI_SYNC_IN is the primary clock input for the chip, the OSC_IN pin is just an isolated clock buffer. If the buffer is not used, the PCI clock “CLK” connects to PCI_SYNC_IN with the same consideration any other PCI clock gets: max of 2.0 ns skew on a motherboard, max 2.5” trace length on a plug-in card.
	PCI_SYNC_OUT	✓	✓	✓	PCI_SYNC_IN		PCI feedback path should have a trace length to PCI_SYNC_IN of equal lengths to other PCI clocks.
	$\overline{\text{PERR}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	PMAA(0:2)		✓	✓	to logic analyzer	open	PMAA assists logic analyzers in recovering addressing information
	$\overline{\text{RCS0}}$	✓	✓	✓	to boot ROM or 100-1K pulldown	open	RCS0 is used for reset startup code. A pulldown on RCS0 selects PCI boot mode.
	$\overline{\text{RCS1}}$	✓	✓	✓	as needed	open	Local ROM or PortX chip select.
	$\overline{\text{RCS(2:3)}}$	✓		✓	as needed	open	Local ROM or PortX chip select.

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	$\overline{\text{REQ}}(4:0)$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	If the arbiter is enabled, $\overline{\text{REQ}}(4:0)$ should be pulled up on a PCI motherboard or private PCI bus. If PCI is not used, ground $\overline{\text{REQ}}0$ (which becomes $\overline{\text{GNT}}$) to park the PCI bus and maintain valid PCI state.
	RFC (RTC)	✓		✓	to LF oscillator	open	Refresh clock is independent of all other clocks.
	RTS1			✓	RS232 driver	open	RS232 Request-To-Send output
	SCK	✓	✓	✓	1K-3K OVDD	open	SCK is open drain.
	SDA	✓	✓	✓	1K-3K OVDD	open	SDA is open drain.
	SDBA0	✓	✓	✓		open	Standard SDRAM address signal.
	SDBA1	✓	✓	✓		open	Standard SDRAM address signal.
	SDCAS	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal.
	SDMA12/SDBA1		✓		SDRAM A12 and/or SDBA1	open	Standard SDRAM address signal. Connects to SDBA1 or A12, depending on SDRAM size. For modules, connect to both A12 and SDBA1.
	SDMA(11:0)	✓	✓	✓	SDRAM A(11:0)	open	Standard SDRAM address signal.
	SDMA(13:12)	✓		✓	SDRAM A(13:12)	open	Standard SDRAM address signal.
	SDMA14			✓	SDRAM A14	open	Standard SDRAM address signal.
✋	SDRAM_CLK(0:3)	✓	✓	✓	SDRAM CLK	open	Standard SDRAM clock signal. Clocks to the SDRAM should have equal-length traces, and generally match the trace length of the SDRAM.
✋	SDRAM_SYNC_IN	✓	✓	✓	SDRAM_SYNC_OUT		Connects to SDRAM_SYNC_OUT usually, except when zero-delay buffers are inserted between feedback path.
✋	SDRAM_SYNC_OUT	✓	✓	✓	SDRAM_SYNC_IN		SDRAM feedback path should have a trace length at least equal to that of SDRAM_CLK to SDRAM clock pin path lengths. Additional delay can be added to increase hold time for SDRAM modules.
	$\overline{\text{SDRAS}}$	✓	✓	✓	SDRAM CKE	open	Standard SDRAM control signal.
	$\overline{\text{SERR}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).

Table 2. Memory/PCI/System Controller Connections (Continued)

Critical	Signal	MPC107	MPC8240	MPC8245	Connection		Notes
					if used	if not used	
	SIN1			✓	RS232 receiver	open	RS232 Received data.
	SOUT1			✓	RS232 driver	open	RS232 Transmitted data.
	$\overline{\text{STOP}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
✋	$\overline{\text{SUSPEND}}$	✓			1K-10K OVDD		$\overline{\text{SUSPEND}}$ requires a pullup.
	$\overline{\text{TRDY}}$	✓	✓	✓	as needed 1K-10K LVDD	1K-10K LVDD	Should be pulled up on a PCI motherboard or private PCI bus, but not on a plug-in peripheral card. If PCI is not used, pull up (or park the PCI bus).
	TRIG_IN	✓		✓	TRIG_OUT	1K-10K OVDD	TRIG_IN is usually connected to TRIG_OUT, or a logic analyzer.
	TRIG_OUT	✓		✓	TRIG_IN or CKSTP_IN	open	TRIG_OUT is usually connected to TRIG_IN, CKSTP_IN, or a logic analyzer.
	$\overline{\text{WE}}$	✓	✓	✓	as needed	open	$\overline{\text{WE}}$ is not needed if non-writable devices (PROM) is used for the boot code (or if the boot code is on PCI).

1.3 L2 Cache SRAM Connections

The MPC750, MPC755 and MPC74X0 processors support a “backside” L2 cache on a private cache bus. The L2 interface uses standard asynchronous, pipelined burst or late-write SRAM devices in a non-pipelined manner. The connections are shown in the following table:

Table 3. L2 Cache SRAM Connections

SRAM Signal	Connection	Notes
A(16:0)	L2ADDR(16:0)	Connect buses; order is not important since burst mode is not used.
A17	L2ADDR17	If present and/or needed. For forward compatibility, tie to a weak (1K-10K pulldown) since LA17 = $\overline{CE3}$ on some SRAM devices.
A18	L2ASPARE	If present and/or needed.
$\overline{ADV}$	L2OVDD	Deasserted since burst mode not used.
$\overline{ADSC}$	GND	Asserted to continually accept addresses.
$\overline{ADSP}$	L2OVDD	Deasserted since burst mode not used.
D(0:63)	L2DATA(0:63)	Connect buses; order is not important since byte access modes are not used. DP bits may be intermixed with D bits if and only if parity-capable SRAMs are always used; otherwise, connect DP only to DP.
DP(0:7)	L2DP(0:7)	Connect buses; order is not important since byte access modes are not used. DP bits may be intermixed with D bits. DP bits may be intermixed with D bits if and only if parity-capable SRAMs are always used; otherwise, connect DP only to DP.
$\overline{G}$ $\overline{OE}$	GND	Since the L2 is chip-select-controlled, it is normally in output mode unless being written to. $\overline{OE}$ may tied low.
CK K	L2CLK_OUTA L2CLK_OUTB	For single-ended clocks, tie one clock to each of two SRAMs without sharing. Keep trace lengths matching other L2 traces. For differential clocks, tie “A” to the active high clocks and “B” to the active low clocks. Route the clocks in a “Y” manner so the stubs have the same, minimal, length.
$\overline{LBO}$	GND or VCC	GND is for PowerPC bursts order; however, burst mode is not used so may be tied high or low.
$\overline{SB(A:D)}$	GND or L2OVDD	Byte write modes are not used.
$\overline{SGW}$	L2WE	Write cause global writes.
$\overline{SW}$	L2OVDD	Byte write modes are not used.
$\overline{SE1}$	L2CE	Connect SRAM chip select.
SE2	L2OVDD	Second chip-select not used.
$\overline{SE3}$	GND	Third chip-select not used.
ZZ	L2ZZ or GND	Optional; not all SRAMs have ZZ.

In addition, the L2SYNC_OUT pin should be connected to the L2SYNC_IN pin using a trace length equal to the ones used on the L2CLK_OUT(A:B) traces.

1.4 Power

The PowerPC family has restrictions on the amount of time any power pin can be at a non-standard voltage in relation to another power pin. Typically these event occur during power-up and power-down. When the restrictions are not met, if the amount of time exceeds approximately 500uS, damage to the part may occur.

If the power supply can sequence all the I/O voltage (OVDD), L2 I/O voltage (L2OVDD), and core voltage (VDD) within the specification limits, or stabilize within 500 uS, then no further design work is needed.

Otherwise, power supply sequencing assistance is needed. The easiest way is to apply a diode voltage sourcing network as shown in the hardware specifications, but other means such as MOSFETs configured as linear regulators are suitable as well. The diode solution supplies just under the targeted operating voltage, but within the differential allowances in the hardware specification. Each device has slightly different allowances, so refer to the hardware specifications for particular examples of diode networks for each device.

Note that the diode network is needed for each non-compliant power supply. However, it is not needed between all power supplies, only between those which are too slow. Thus, if OVDD (typically 3.3V) is stable first and last, the others can be derived from it alone.

1.5 Clocks

All clocks should be carefully routed to be of equal lengths within similar domains (PowerPC system bus, memory bus, or PCI bus). Devices with integrated clock drivers make this relatively easy; see the hardware specifications, or the MPC107 Application Guide for further details.

1.6 References

The reference materials shown in Table may be useful to the designer. To locate the documents, go to http://www.motorola.com/ and search for the document title.

Table 4. Reference Material

Description	Document
MPC107 Hardware Specification	MPC107EC/D
MPC107 Design Guide	AN1849/D
PowerPC 603e™ Hardware Specifications (PID6)	MPC603EEC/D R2
PowerPC 603e Hardware Specifications (PID7t)	MPC603E7TEC/D R3
MPC750A Hardware Specification	MPC750EC/D
MPC7400 Hardware Specifications	MPC7400EC/D
MPC8240 Integrated Processor Hardware Specifications	MPC8240EC/D

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