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68K ColdFIRE® MICROPROCESSORS

Application Note

Evaluating ColdFire® in a 68K Target System: MCF5307 to MC68EC020 Gateway Reference Design

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Motorola's 68K family has been the market leader in embedded applications for many years. As a result of this, there is a great wealth of experience in the industry surrounding the architecture. The highly competitive nature of the embedded systems market compels designers to strive to find the best trade-off between price and performance for microprocessors. Methods used by microprocessor manufacturers to improve processor performance such as pipelining or increasing on-chip cache can be very expensive with respect to silicon area. To overcome this problem and minimize cost with maximum performance, it may be necessary to implement changes in the architecture. This can result in difficulties when a designer wishes to upgrade their design. There may be implications for hardware and software compatibility which would not be present if the architecture remained unmodified.

The ColdFire architecture has been designed specifically for high performance, cost sensitive embedded applications. In doing this, the 68K architecture was analyzed and the way that embedded systems designers use the architecture was examined. As a result, the features of the architecture used less frequently in embedded system design were removed.

The ColdFire architectures' foundation in Motorola's 68000 architecture allows designers to take advantage of the established tool support, code evolution, and engineering expertise. It uses a variable length RISC instruction set to optimize both code density and allow one instruction to be issued every clock cycle where possible. The ColdFire instruction set is a subset of the 68K instruction set, that is compatible at both assembler and binary levels. The programming model is also identical to the 68K, with the exception that it has a simplified stack pointer and exception stack frame.

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The Gateway reference design which will be discussed is an integrated circuit board which will bridge an existing MC68EC020 system to the ColdFire MCF5307 microprocessor, to evaluate the ease of upgrading to a higher performance architecture. It can be used to evaluate system enhancements such as on-chip instruction and/or data cache and bursting to external memory. It can also be used to port a customer's system code to the ColdFire architecture in situ as opposed to the traditional method of initially porting code to an evaluation platform. This paper is intended to describe the use and operation of the Gateway board.

In using the Gateway solution, the 68K processor initialization code has to be configured to run on the internal register map of the ColdFire processor. Although the ColdFire architecture is derived from the 680x0 family with a simplified set of instructions and addressing modes, assembler programs while straightforward to port to ColdFire may require some modification before they will run. To help customers with this translation process, Motorola has funded the development of an assembler code converter - PortASM/68K, written by MicroAPL Ltd. in the U.K.

(Consult http://www.mot.com/SPS/HPESD/tools/companion.html for more information.)

This utility will run on either PC's (under DOS, Windows 3.x, Windows95/98 & Windows NT) or Sun Workstations (under SunOS or Solaris) and is available free of charge via download from the web. This converter not only converts the 68K assembler code to ColdFire assembler but analyses how the original code operates allowing the analyzer to produce optimized ColdFire code in two passes, rather than just a straight translation.

1.1 Design Considerations

The MC68EC020 is a low-cost, (high performance) embedded derivative of the popular 32-bit MC68020 Microprocessor. The major differences between the MC68020 and the MC68EC020 is that the MC68EC020 has a 24-bit address bus and does not implement the /ECS, /OCS, /DBEN, /IPEND or /BGACK signals.

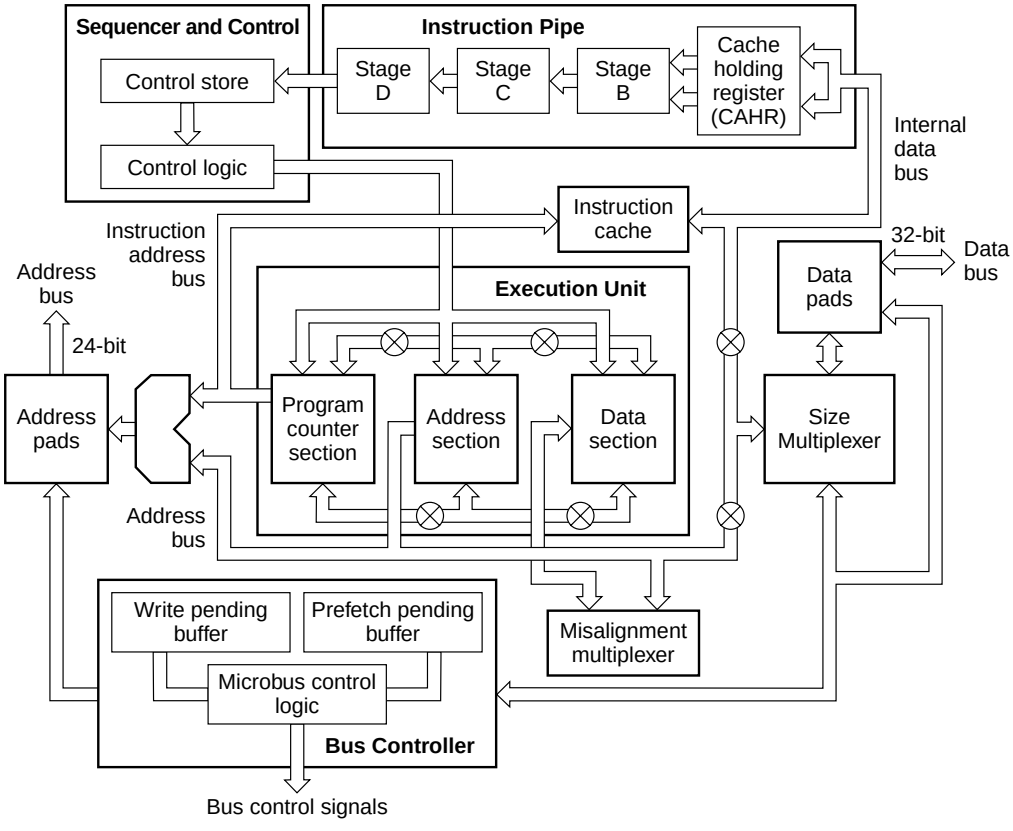

Figure 1. MC68EC020 Block Diagram

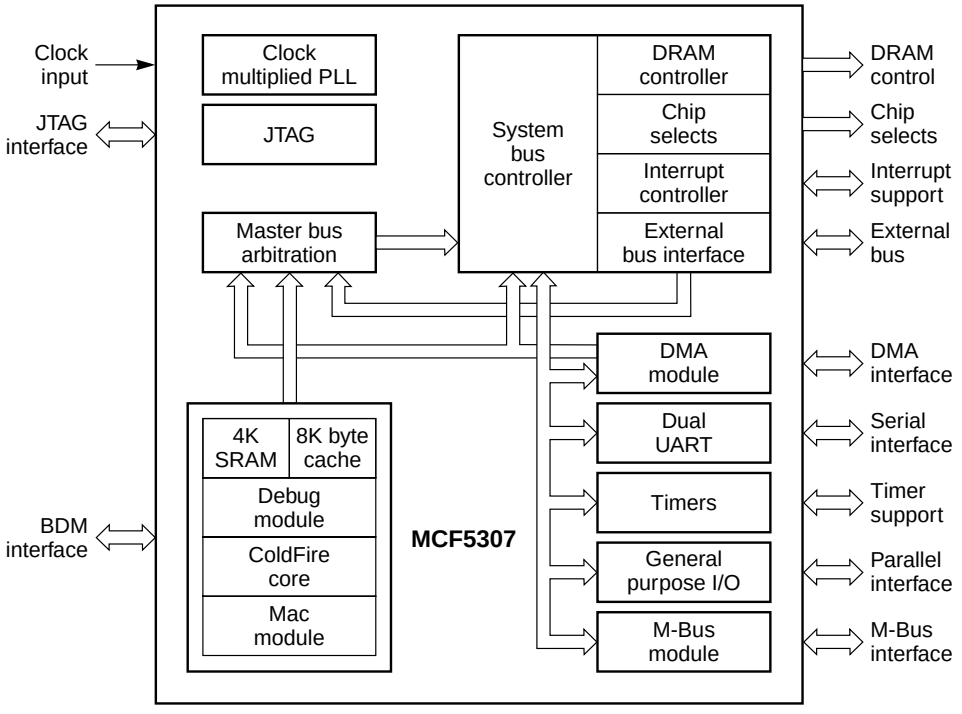

Figure 2. MCF5307 Block Diagram

A key feature required for debugging a microprocessor system is memory. This allows the designer to download and run code. The ColdFire MCF5307 microprocessor has 4Kbytes of on-chip Static RAM (SRAM) and a DRAM control module built onto the silicon from which both asynchronous and synchronous external memory can be “gluelessly” interfaced. The DRAM controller offers the designer a clear cost saving by reducing the component count of the system. This module also provides the flexibility to interface to multiple memory configurations.

In addition to requiring DRAM or SRAM memory for debugging software, many designers require non-volatile storage in the form of FLASH memory to store boot code or data that has been collected by the system. Data or code stored in FLASH memory can be accessed, modified or erased via the BDM port.

With this in mind, the MC68EC020 to MCF5307 Gateway Reference Module was designed with 4 Mbytes of Fast Static RAM, 1 Mbyte FLASH ROM and an additional RS-232 compatible serial communications port. It consists of two printed circuit boards, an interconnect board that connects to the 68K target which derives the 3.3V supply needed by the MCF5307 from the 5V target hardware supply and a microprocessor / memory board which contains the ColdFire processor. This second board provides additional hardware performing many tasks such as control processing from external hardware, pulling active low control signals to a high logic level and decoupling all power supplies to suppress noise. Given the modules incorporated into the design, the reference module can be considered a self-contained ColdFire sub-system

1.2 MC68EC020 PGA—MCF5307FT, Gateway Reference Design

This section includes the following subsections:

- MCF5307 CPU, Clock, RESET and BDM Circuit
- RS232 Communications Port
- MC5307FT Microprocessor Connection
- FSRAM and Flash Memory Connections
- PLL PSU and Initialization of MCF5307 Out of Reset
- Test Points, Decoupling and Pull-Up Resistors

1.2.1 MCF5307 CPU, Clock, RESET and BDM Circuit

Figure shows the main circuit diagram for the ColdFire MCF5307 including selectable clock, RESET circuitry and BDM connectivity.

1.2.1.1 Clock Circuit

The clock supply to the MCF5307 Microprocessor is selectable via jumper JP1. The Clock source can be either from a local 45MHz crystal oscillator (SMT), (jumper position 2 / 3), or externally from the CLKIN input pin, (jumper position 1 / 2) i.e the target hardware. The crystal oscillator uses the same 3.3V supply as the MCF5307 microprocessor.

1.2.1.2 Reset Circuit

The main reset signal, RSTI, is controlled by the MAX708TCSA chip illustrated in Figure . The MAX708TCSA chip provides the circuit with a guaranteed reset output during power up / down and brownout conditions. (Brownout is the term given to abnormally low power supply voltages). The reset threshold voltage for this device is set at 3.08V and an additional 1.25V threshold detection circuit is included on-chip to indicate power fail / low battery conditions. The added advantage of using this type of device is that it does not require additional components.

The MAX708TCSA chip is powered by a 3.3V supply and is activated by bridging RESET jumper JP2. The RESET line is pulled up to a logic high level via a 4.7K-ohm resistor (R2). A red LED is attached to the reset line to indicate that a reset has taken place either through the MAX708TCSA chip or from the BDM port. Switch S1, connected to the MAX708TCSA chip, provides the user with the ability to manually reset the system if required.

1.2.1.3 Background Debug Mode (BDM) Connector

To allow the full debug capabilities of the MCF5307 microprocessor, a 26-way BDM connector has been included on the Gateway Reference Board. Pin 7 on the connector, Reset, is connected to 3.3V through a 4.7K resistor to prevent false switching.

1.2.1.4 Pull-up Resistors, LED's and Miscellaneous Connections

The green surface mount LED, D2, which is connected to the 3.3V supply and current limited by the 470-ohm resistor, R4, indicates the power supply onto the Gateway board. The red LED, D1 indicates that a RESET has been asserted either by the MAX708TCSA or by an external device through the BDM target connector.

The test mode signals on the MCF5307 microprocessor determine whether the device operates in BDM or JTAG test mode. The MTMOD0 is the key signal that determines this selection so the MTMOD[3:1] signals should be tied low to ground. To ensure that the MCF5307 microprocessor assumes control of the bus, the bus grant (/BG) signal must be tied to ground through a 4.7K resistor. Similarly, the test clock signal must be tied to ground (again through a 4.7K resistor) when it is not being used.

The MCF5307 microprocessor should be powered via 3.3V supply and connected to appropriate ground connections as indicated on the circuit diagram.

1.2.2 RS232 Communications Port

The schematic in shows how a standard 5V tolerant RS232 communications port can be created using a Motorola MC145407DW 5V driver / receiver. The MC145407DW combines three drivers and receivers to meet electrical standards EIA-232-E and CCITT V28. The six drivers on the MC145407 are designed to guarantee a charge pump output of ± 5 V while operating from a single 5V power supply. RS232 logic levels are obtained by an internal voltage doubler and inverter arrangement that converts +5V to ± 10 V.

The RS232 control signals are fed into the Gateway board through connector CON8 that is powered via a 5V DC supply. Capacitors C20-23 provide high /low frequency bypass to minimize noise in the system. Capacitors C18 and C19 are the charge pump capacitors that determine the slew rate of the charge pump therefore governing the overall operation of the MC145407DW chip. Setting the value of C18 and C19 to 10uF, gives the same slew rate output characteristics of the MC145407DW chip as that given in the electrical specification section of the data sheet. Note, the correct polarity of the electrolytic capacitors must be observed when constructing the gateway board!

(Consult http://www.mot-sps.com/books/dl136/pdf/mc145407rev1.pdf for more information on this device.)

1.2.3 MC5307FT Microprocessor Connection

The diagram in Appendix E shows the jumper connections to the MC5307 Microprocessor. Four 50-way connectors are used to breakout the signals from the chip into the dual in line connectors (DIL). Connectors J3-2, J4-2, J5-2 and J6-2 allow the MC68EC020 target hardware control signals to connect directly to the control signals on the MCF5307 via the Gateway Reference board. This diagram also shows jumper JP16 which is used to connect the reset on the target device to the ColdFire reset.

1.2.4 FSRAM and Flash Memory Connections

The schematic shown in Appendix F illustrates the connections of the on-board FLASH ROM (MBM29F800A3BT80) and the 128Kx8 Asynchronous Fast SRAM (MCM6926AWJ8). This configuration provides 1 Mbyte of Flash ROM and 4 MBytes of FSRAM memory.

The MCM6926A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. The static design of this part eliminates the need for external clocks or timing strobes and only requires three control signals for operation – output enable (/G), chip enable (/E) and write enable (/W).

Chip select 5 (/CS5) controls the chip selects for all the FSRAM chips and the output enable signal (/OE) on the MCF5307 microprocessor controls the output enable of all memory chips – both the FLASH ROM and FSRAM. Write enable of the FSRAM chips is independently controlled through the (Byte) Write Enable signals (/WE[0:3]) directly from the MCF5307 microprocessor. Chip select 5 was chosen for the FSRAM to allow lower order chip selects to be used for interfacing to devices on the target hardware.

Pull-up resistors R5-R8 (10K) are required for stable FLASH operation and these are connected to /BYTE, RY/BY, RP and WP active low pins on the chip. The pull-up resistor attached to the /BYTE pin on the FLASH device sets the bus mode to 16-bit data bus mode. If this pin is pulled low the bus mode is set to 8-bit.

Chip select 0 is used to control access to the FLASH memory block and is selectable via jumper JP3 (See Appendix I). This jumper is included in the design to allow /CS0 to be used to boot from the target hardware, rather than local FLASH ROM. The ready / busy line on the FLASH memory block is sensed directly using Address pin 28 on the MCF5307 Microprocessor. [By configuring the appropriate pin in the Pin Assignment Register of the MCF5307 ColdFire, Address pin 28 can be set up for general purpose I/O.]

Both of the memory chips (FLASH & FSRAM) are connected to the MCF5307 data bus (D0..31) and address bus (A0..27).

1.2.5 PLL PSU and Initialization of MCF5307 Out of Reset

When the Gateway board is first powered up, the MCF5307 microprocessor must be configured into a known initial state. This is achieved using eight jumpers (JP5-JP12) and the MC74LCX541T low-voltage CMOS Octal Buffer. Jumpers JP5 and JP6 are used to set the divide ratio of BCLK/PSTCLK that is sampled during reset. In a similar fashion, jumpers JP7 and JP8 are used to set the frequency range of CLKIN and therefore the range at which the MCF5307 PLL will be operating.

Jumper JP9 controls the configuration of the pin assignment register. The system is configured as a 16 bit wide parallel port PP[15:0] if this bit is logic zero (jumper in the 2 /1 position). However, if this bit is logic one (jumper in position 3 / 1), alternative multiplexed pin functions are setup when the corresponding bit in the pin assignment register is set to a one. (PP[15:8] are general purpose I/O and multiplexed with A[31:24]. PP[7:0] are multiplexed with /DREQ[1:0], /TIP, TM[2:0] and TT[1:0] signals).

Jumpers JP10 – JP11 are used to define the size of the /CS0 port immediately after reset. Jumper JP12 sets the automatic acknowledge of chip select zero.

PVDD, the power supply for the on-chip PLL, is supplied via the main 3.3V power supply. This power source is smoothed out by a 470nH inductor and low / high frequency noise is removed using bypass capacitors C16 and C17.

On reset, the inputs from the 8 different jumper switches (JP5-JP8) are latched directly onto signals D0-D7 of the MCF5307 microprocessor's data bus. The high impedance inputs on the MC74LCX541 significantly reduce current loading to the input drivers and allow the inputs to be safely driven from 5V devices. This makes the MC74LCX541 particularly suitable for memory address driving and all TTL level bus oriented transceiver applications.

1.2.5.1 PAL Control Equations—U10

A bus arbiter is required to arbitrate between the buses of the MC68EC020 target hardware and the MCF5307 microprocessor. PAL U10 performs this function. All of the logic equations assume that the system is not held in RESET.

The direct memory acknowledge (DMACK) signal is generated from the transfer type pins (TT1 and TT0) on the MCF5307. If the TT0 signal is asserted and the TT1 signal is not asserted, the bus cycle is encoded as an emulator access and the DMACK signal becomes asserted.

The transfer type pins (TT[1:0]) and the transfer modifier pins (TM[2:0]) are both used to determine the type of bus access and additionally the address space that can be accessed. If both of the transfer type pins are asserted then the bus access to the MC68EC020 is a normal mode access. If transfers are made in CPU space then the transfer modifier pins are asserted. Hence, if both the transfer type and modifier pins are asserted, the bus cycles on the MC68EC020 must access normal CPU space.

Alternatively, if both the transfer type and modifier pins are all de-asserted, the transfer modifier pins carry the interrupt level being acknowledged. Thus in this case, interrupt level 7 would be acknowledged.

The bus is granted to the target hardware when the bus request from the target is asserted and the bus is not already granted to the MCF5307 microprocessor.

Similarly, the bus is granted to the MCF5307 microprocessor as soon as possible after receipt of a valid bus request signal. The bus will be granted to the MCF5307 when either the MCF5307 has requested the bus or when the target hardware is not requesting the bus and the bus is being driven.

Appendix A illustrates all of the relevant control equations and simulation setups for coding PAL U10.

1.2.5.2 PAL Control Equations—U11

The transfer acknowledge bus sizing control signals are controlled by PAL U11.

The MC68EC020 can dynamically interpret the port size of the addressed device during each bus cycle. Unfortunately, the MCF5307 Microprocessor cannot perform this type of dynamic bus sizing. When the MCF5307 is the bus master, however, it can use the size pins (SIZ[1:0]) to indicate the requested transfer size for bus cycle encoding. When the MC68EC020 is the bus master the size pins will be inputs.

The SIZ0 pin on the MCF5307 Microprocessor is asserted when the DSACK0 signal is not asserted and the DSACK1 signal is asserted. Similarly, the SIZ1 signal is asserted when the DSACK1 signal is not asserted and the DSACK0 signal is asserted. (The DASCK0/1 signals on the MC68EC020 are logically opposite to the SIZ0/1 signals on the MCF5307).

PAL output pins 14 and 15 are connected to hardware test pads. Example logic for coding PAL output pin 14 has been given in Appendix B. The example code asserts signal “SPARE” (Pin 14) when both the DSACK signals are asserted indicating that the Data bus port size is encoded for 32 bits. (The NC on pin 15 could be coded in a similar fashion for other user specific functions.)

If the target device is driving the bus and asserts any of the DSACK signals then the transfer acknowledge signal on the MCF5307 is asserted. Note that this control line requires a pull-up resistance of 1Kohms to ensure a fast negation of this signal, which in turn prevents false cycles on the bus. The SIZ0 and SIZ1 signals generated by the PAL are tied high internally to prevent glitches during reset. The TA signal is set to default to a data bus size of 32 bits on reset using the “SPARE” control line and DSACK0 / 1 signals.

Appendix B illustrates the corresponding set of PAL control equations for generating the TA bus sizing and test pad control signals.

1.2.6 Test Points, Decoupling and Pull-Up Resistors

The schematic shown in Appendix I detail the key signals that can be accessed through test points positioned throughout the board to aid debugging. The basic signals that are accessible are /TS, /AS, /CS5, /TA, R/W, GND and VDD (3.3V).

Also listed on this schematic page are the signals that must be pulled-up to a high logic level to avoid false signaling. Each signal that requires a pull-up is tied to 3.3V using a 4.7Kohm resistor.

Jumper JP4 on the schematic selects BDM debug operation or JTAG operation of the test module on the MCF5307 microprocessor. If the jumper is placed in position 2 / 3, BDM operation will be selected. Similarly, if the jumper is placed in position 1 / 2, the Gateway board will select JTAG operation. This signal is then fed into the MCF5307 microprocessor on test mode pin MTMOD0.

The schematic also shows the decoupling capacitors that need to be connected to the power and ground pins of all on-board chips to minimise the effects of noise in the system. Note the use of both 0.1uF and 1nF capacitors to inhibit both low and high frequency noise in the system.

Jumper JP3 is used to select either on-module FLASH chip select or off-module user chip select. If the jumper is in position 2 /3, off-module user chip select is activated and the local FLASH chip select if the jumper is in position 1 / 2.

For the purposes of I/O debugging, three surface mount LED's (D3, D4 and D5) are connected onto the spare MCF5307 ColdFire address lines at A[29:31] via 470 ohm resistors (R11-13). As detailed previously, these spare address lines can be configured as general I/O pins by setting the appropriate values in the pin assignment register of the MCF5307 microprocessor.

Appendix A
PALASM Control Equations for PAL U10

```
TITLE                   U10_BUS_ARBITRATION
PATTERN                 P00001
REVISION                1
DATE                    5th March 1998
AUTHOR                  Pete Highton
COMPANY                 Motorola SPS (c) 1998


CHIP    U10       PALCE16V8

PIN     1         CLK             COMBINATORIAL
PIN     2         /RESET          COMBINATORIAL
PIN     3         /TT0            COMBINATORIAL
PIN     4         /TT1            COMBINATORIAL
PIN     5         /BR_TGT         COMBINATORIAL
PIN     6         /BR             COMBINATORIAL
PIN     7         /BD             COMBINATORIAL
PIN     8         /WR             COMBINATORIAL
PIN     9         /AS             COMBINATORIAL
PIN     10        GND
PIN     11        NC
PIN     12        /TM0            COMBINATORIAL
PIN     13        /TM1            COMBINATORIAL
PIN     14        /BG_TGT         COMBINATORIAL; O/P
PIN     15        /BG             COMBINATORIAL; O/P
PIN     16        /TM2            COMBINATORIAL
PIN     17        FC1             COMBINATORIAL; O/P
PIN     18        /DMACK          COMBINATORIAL; O/P
PIN     19        /DS             COMBINATORIAL; O/P
PIN     20        VCC


EQUATIONS


BG = (BD + (BR * /BR_TGT)) * /RESET
BG_TGT = BR_TGT * /BG * /RESET          ; Bus grant to the target H/W
FC1 = /TT0 * /TT1 * /TM0 * /TM1 * /TM2 * /RESET; Set FC1=1 for ;interrupt level
7 ack.
DMACK = /TT0 * TT1                      ; More info. on TM settings!
DS = AS * /RESET                        ; Delay write cycle DS by 1 clock.
```

Appendix B
PALASM Control Equations for PAL U11

```
TITLE                   U11_TA_BUS_SIZING
PATTERN                 P00002
REVISION                1
DATE                    5th March 1998
AUTHOR                  Pete Highton
COMPANY                 Motorola SPS (c) 1998

CHIP    U11       PALCE16V8

PIN     1         CLK             COMBINATORIAL ; Input
PIN     2         /DSACK0         COMBINATORIAL ; Input
PIN     3         /DSACK1         COMBINATORIAL ; Input
PIN     4         /CS0            COMBINATORIAL ; Input
PIN     5         /CS1            COMBINATORIAL ; Input
PIN     6         /CS2            COMBINATORIAL ; Input
PIN     7         /CS3            COMBINATORIAL ; Input
PIN     8         /CS4            COMBINATORIAL ; Input
PIN     9         /CS5            COMBINATORIAL ; Input
PIN     10        GND
PIN     11        NC
PIN     12        /CS6            COMBINATORIAL ; Input
PIN     13        /CS7     COMBINATORIAL       ; Input
PIN     14        SPARE1
PIN     15        NC
PIN     16        SIZ1            COMBINATORIAL ; Output
PIN     17        SIZ0            COMBINATORIAL ; Output
PIN     18        /TA             COMBINATORIAL ; Output
PIN     19        /BD             COMBINATORIAL ; Input
PIN     20        VCC


EQUATIONS

SIZ1 = DSACK1 * /DSACK0 * /BD       ; Asserted for word transfer and not bus
                                    ; master.
SIZ1.TRST = VCC
SIZ0 = /DSACK1 * DSACK0 * /BD       ; Asserted for byte transfer and not bus
                                    ; master.
SIZ0.TRST = VCC
TA = (DSACK0 + DSACK1) * BD         ; TA generated if either DSACKx signal
                                    ; asserts while bus master.
SPARE1 = (DSACK0 + DSACK1)
TA = VCC
TA.TRST = SPARE1
```

```
;---------------------------------- Simulation Segment ------------
SIMULATION

TRACE_ON DSACK0 DSACK1 TA

SETF  /DSACK0 /DSACK1
CLOCKF CLK
CLOCKF CLK


SETF DSACK0
CLOCKF CLK
CLOCKF CLK

SETF  /DSACK0 /DSACK1
CLOCKF CLK
CLOCKF CLK
SETF DSACK1
CLOCKF CLK
CLOCKF CLK
SETF  /DSACK0 /DSACK1
CLOCKF CLK
CLOCKF CLK


TRACE_OFF
```

Appendix C—Schematics

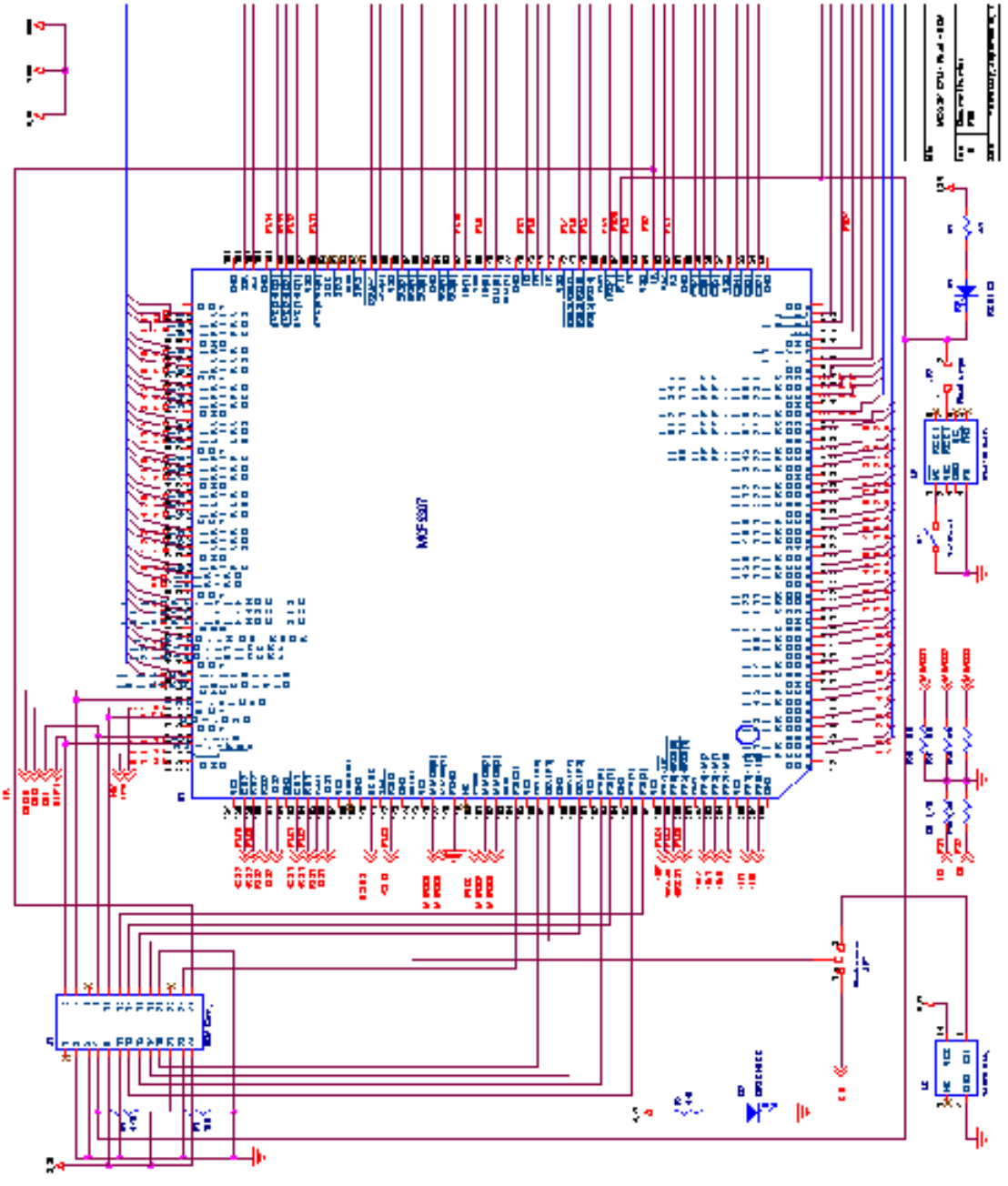

Figure 3. MCF5307 CPU, RESET & BDM Connections

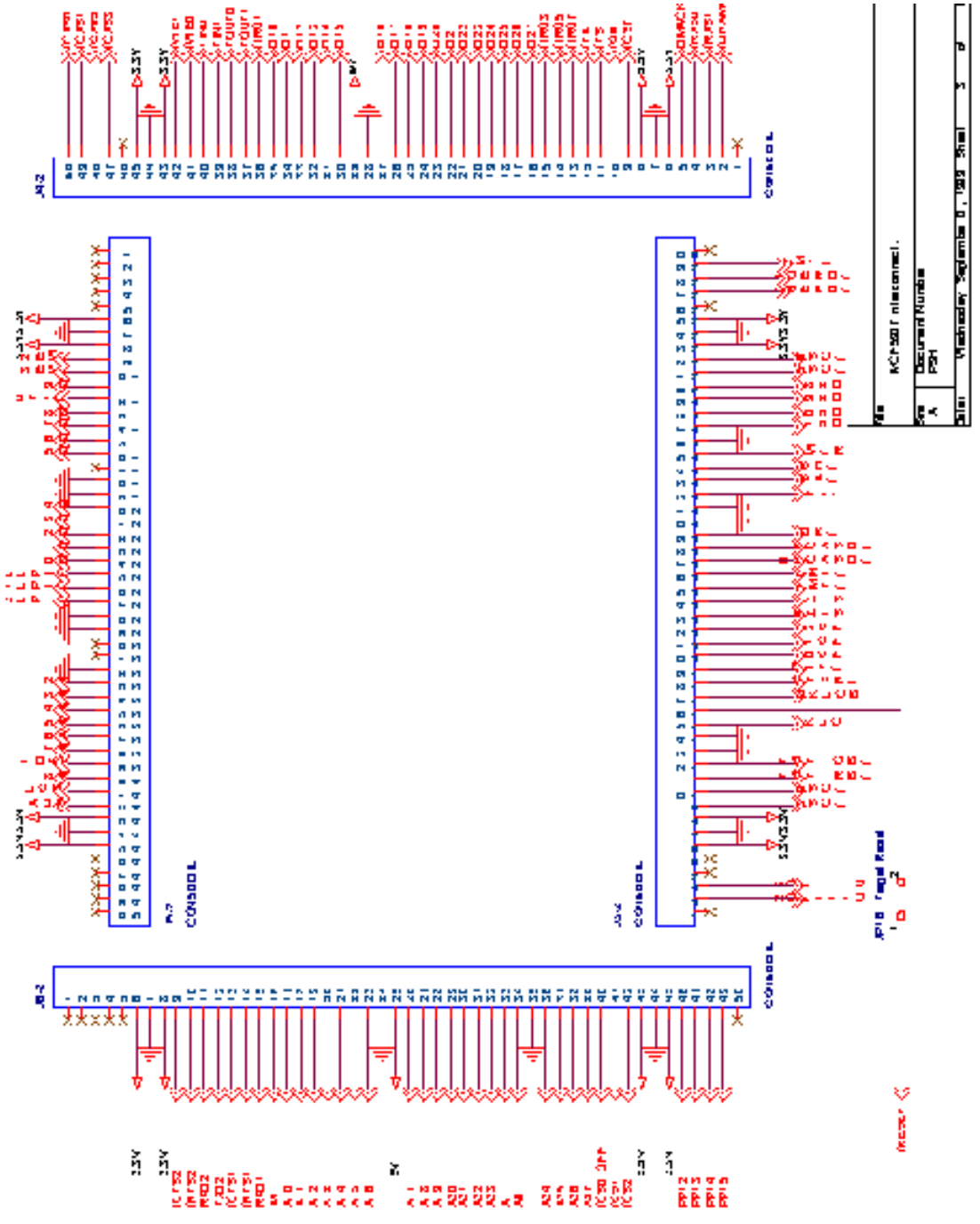

Figure 4. RS232 Serial Communications Port

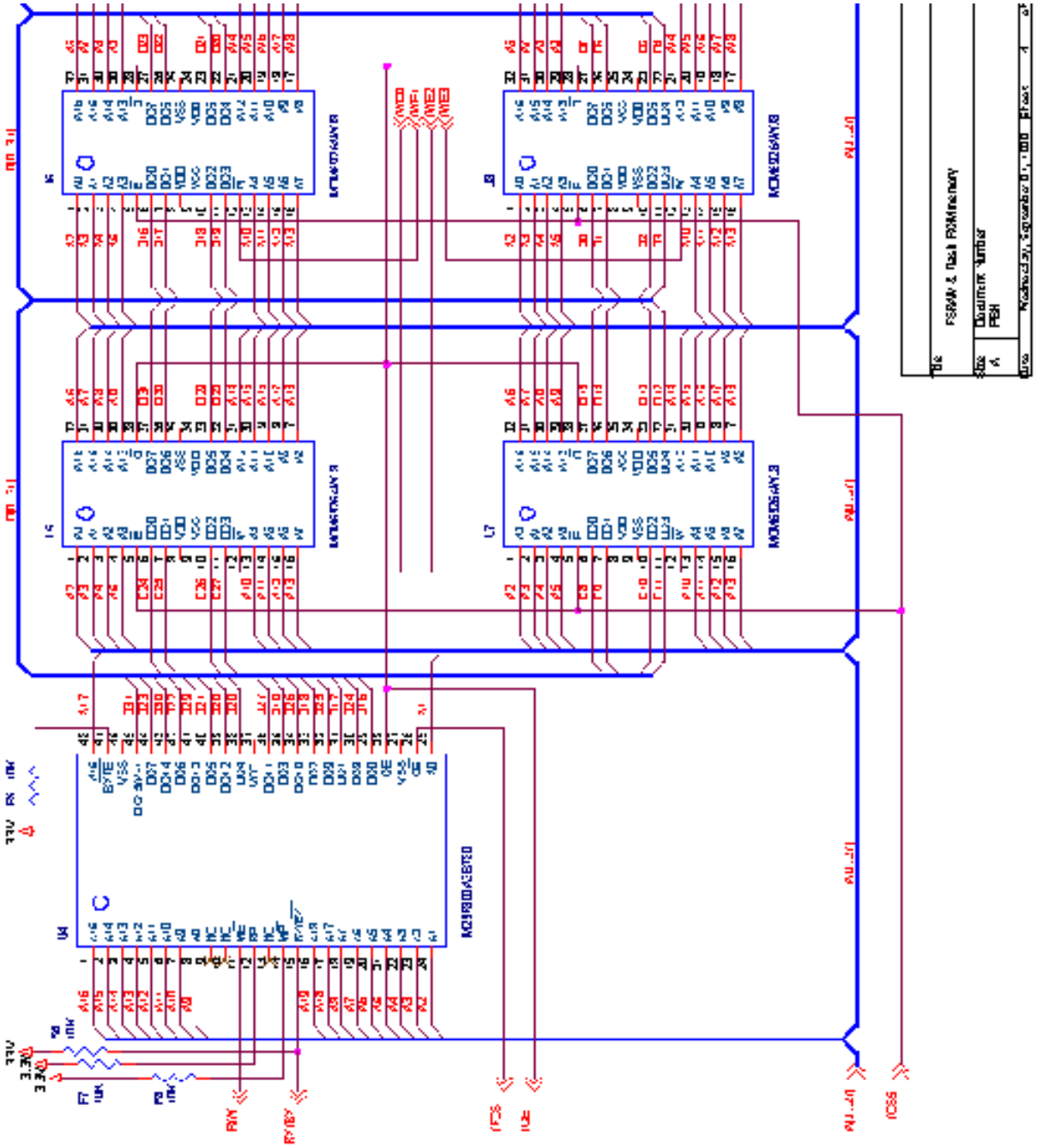

Figure 5. FS RAM and FLASH ROM Memory

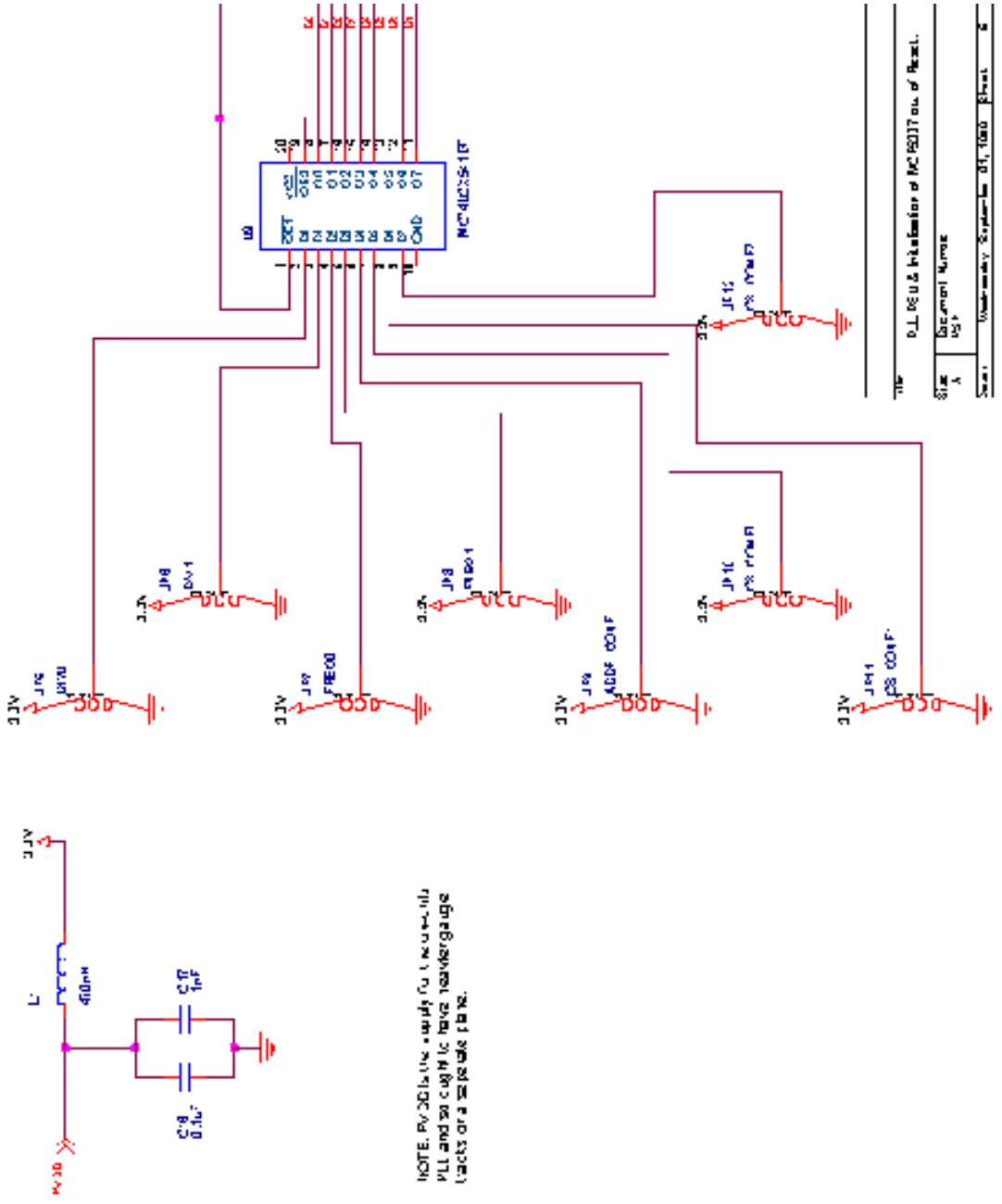

Figure 6. Flash & ROM Memory

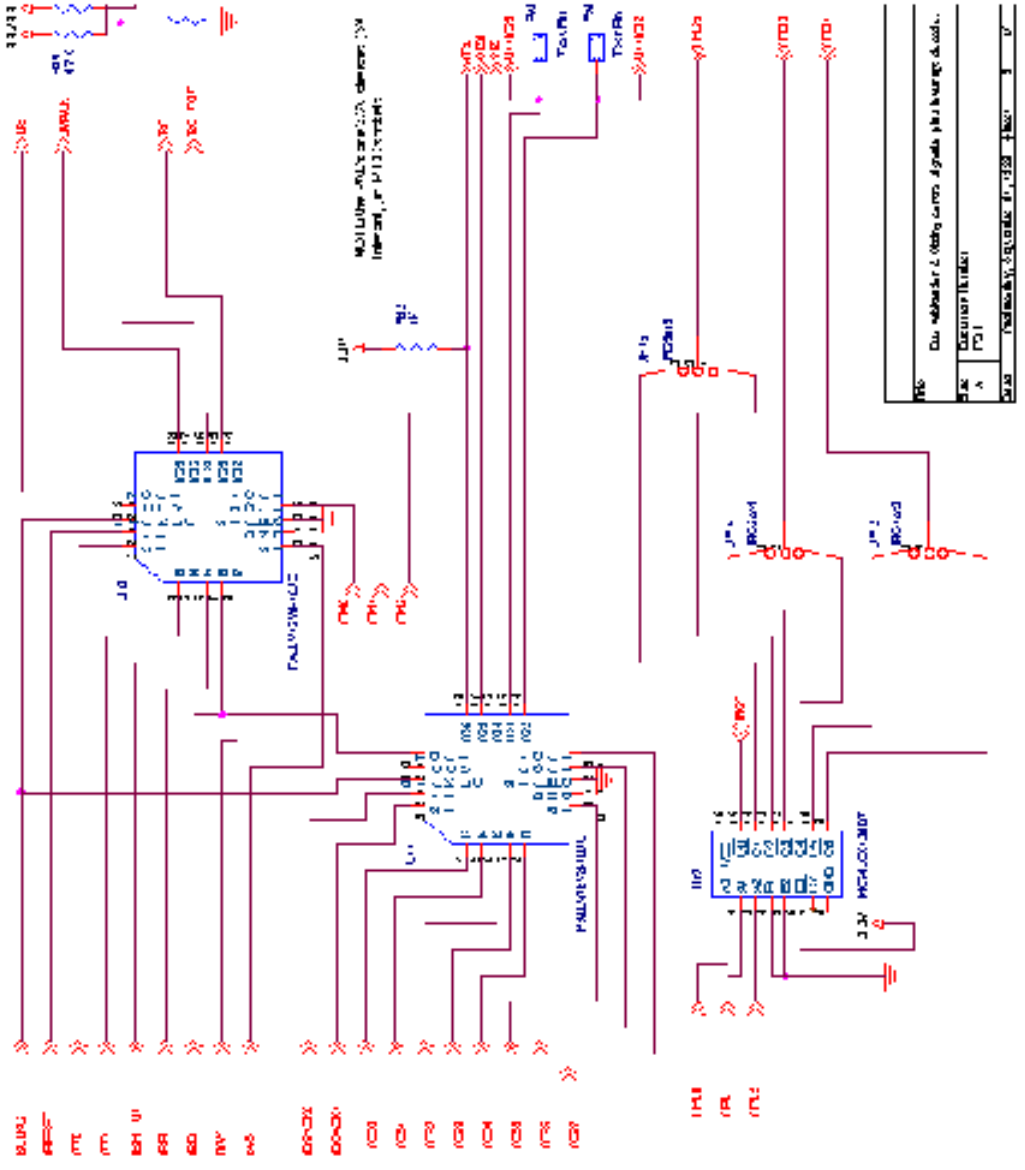

Figure 7. Bus Arbitration and Control Signals

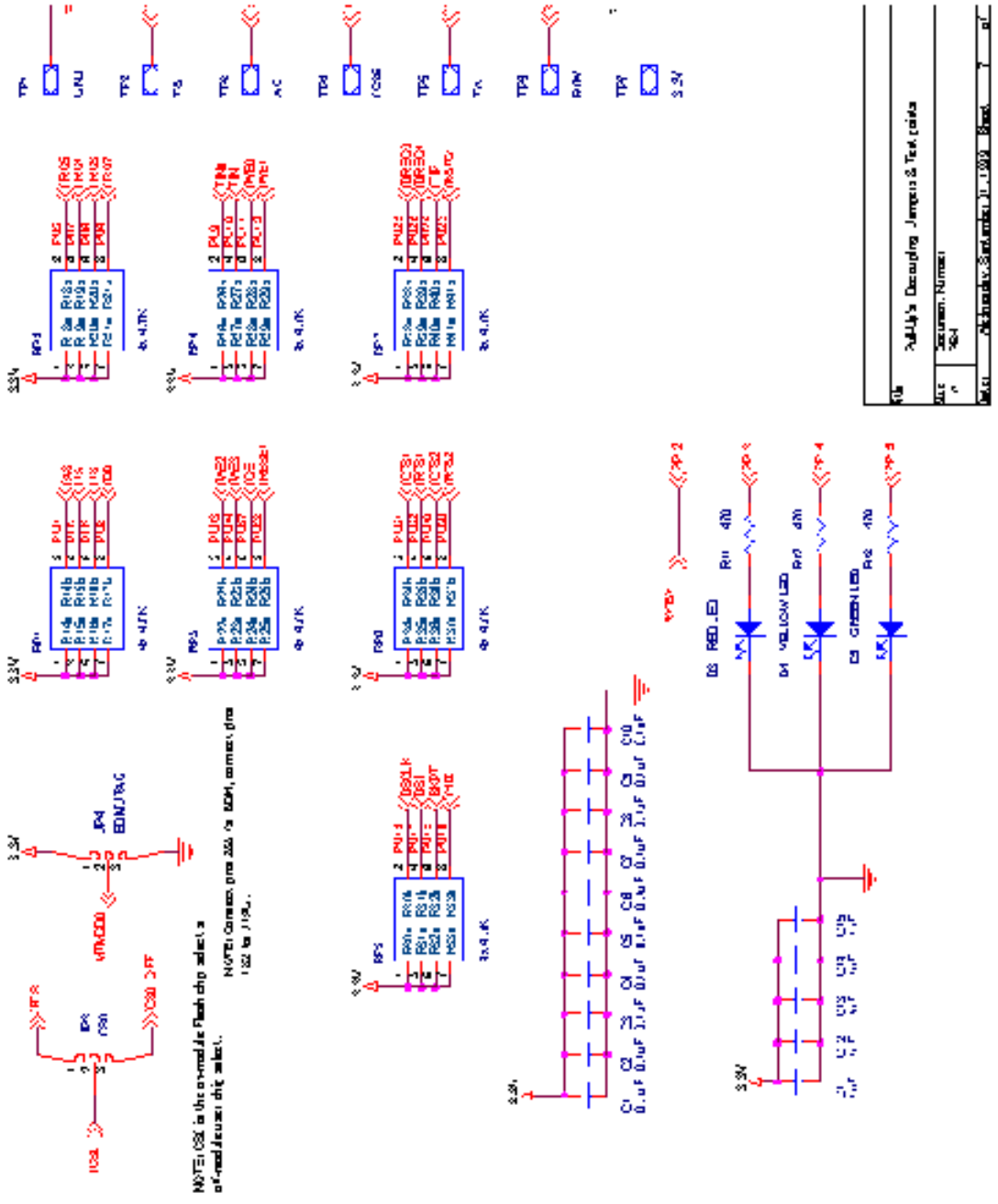

Figure 8. Decoupling

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