$\pm$1.5g Dual Axis Micromachined Accelerometer Power Supply Rejection Ratio (PSRR) Suggestions

by: Peter Schultz
Product Engineer

COMPONENT DESCRIPTION

The MMA6200Q series is a two axis (X and Y) accelerometer family with sensitivity parallel to the device's mounting plane. The device utilizes variable capacitance sensing elements and a two-channel interface IC all in a 16-pin QFN package.

This section provides a general description of the device power supply rejection ratio (PSRR), how it affects device performance, and suggestions for improvement.

INTRODUCTION TO POWER SUPPLY

Rejection Ratio

The power supply rejection ratio is a measure of how well the device rejects the noise on the power supply line. The MMA6200Q series is capable of being used in several different applications. In some cases it may be possible for supply line noise to adversely affect the output signal. This phenomenon can create large output signals when the supply line noise frequencies are roughly equal to the device's oscillator frequency and/or harmonics. The oscillator drives the g-cell sampling as well as the internal low pass filter. When the difference between the frequency of the noise on the supply and the oscillator frequency is less than the low pass filter cutoff frequency the aliased signal passes through the filter. This aliased signal is then amplified internally by the device creating an even more adverse effect. This noise at the output can be as much as ten times the amplitude of the input noise at the oscillator frequency or its harmonics.

IMPROVING THE POWER SUPPLY

Rejection Ratio

If the power supply contains noise approaching the oscillator frequency, large amounts of noise may be observed at the output of the device. This does not become an issue until the noise frequency is a little larger than the oscillator frequency; a little larger here meaning still within the internal low pass filter's bandwidth. In application a simple low pass filter at the input helped to resolve this issue by attenuating much of the offending noise before it enters the device.

A simple two element low pass filter at the input of the device, made up of a resistor in series with a capacitor in shunt with V_{dd}, works rather well (see Figure 1).

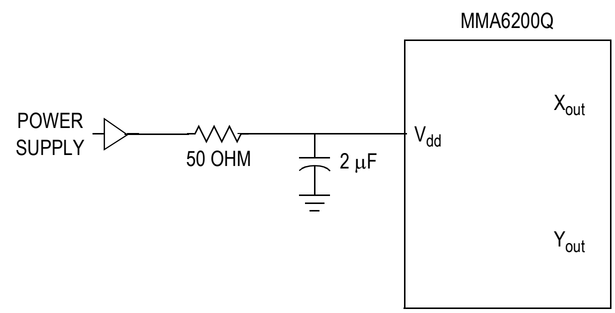

Figure 1. RC Input Loading for PSRR at V_{dd}

With this combination of a 50 ohm resistor and a 2 µF capacitor there is a large reduction in the PSRR, roughly 10X. This is now well below unity gain; meaning at the output of the device there is noticeably less noise than was supplied to the device, at the oscillator frequency and/or its harmonics. The first harmonic is at the oscillator frequency of roughly 15 KHz. The following illustration shows the effect on the PSRR when placing different values of capacitance at the input and retaining the 50 ohm resistor. There is six harmonics represented in the illustration the first of which is at about 15 KHz. These data points at the different harmonics represent the ratio of the output noise to the input noise. Depending on the application needs one can use this illustration to help determine the capacitive needs for the filter (see Figure 2). The plot is given in Log scale.

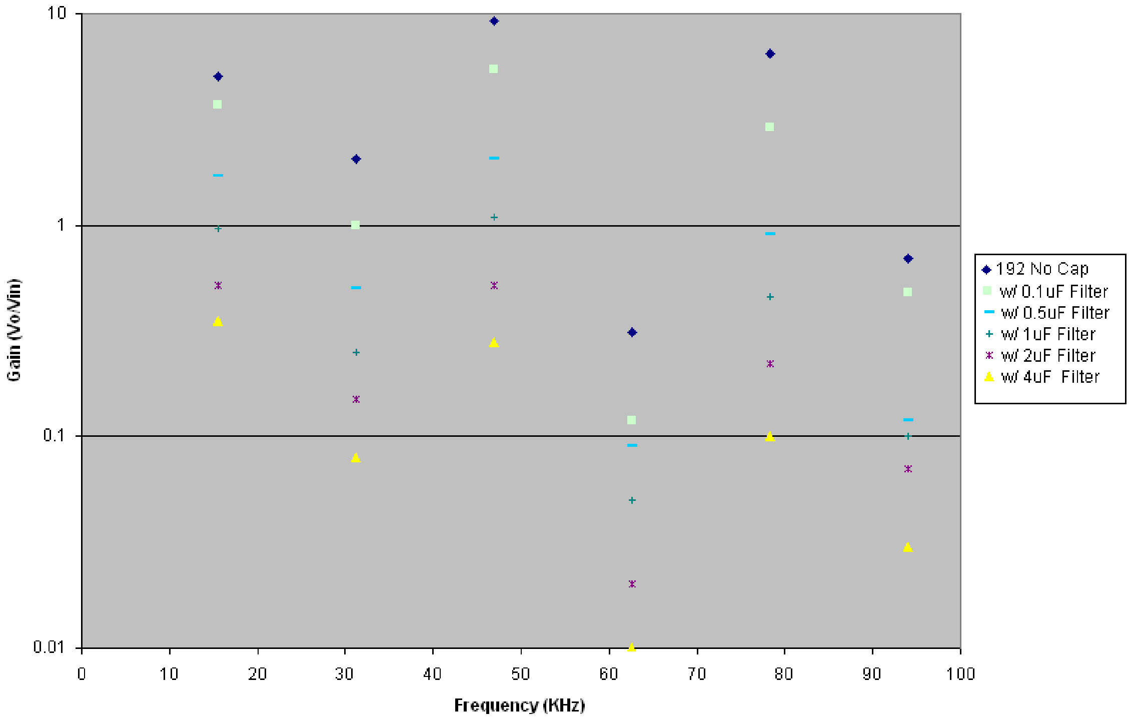

Figure 2. PSRR with 50 Ohm and Varying Input Capacitance

One can see the PSRR has improved by roughly a factor of 10 with a 2 μF capacitor at the input. Not only can the plot be used as a guide in the design of an input filter, it can also help put in perspective the possible amplitudes of the signal and about what frequencies they may occur. From looking at the plot one can see that for a capacitance of 1uF the gains at the two most predominate noise frequencies is unity. This means the aliased signals will not be larger in amplitude than the input noise that created it; giving the recommended smaller capacitance filter in the following illustration (see Figure 3).

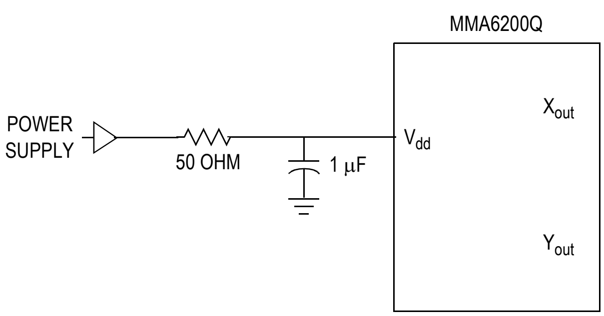

Figure 3. Recommended RC Input Loading for PSRR at V_{dd}

With cost as one of the deciding factors, this is a recommended filter design for reducing the PSRR. One should note however that variations in the individual devices and the different axes of the device produce plots that may look significantly different. The intent here is only to give an idea of the effects of different capacitances on the oscillator induced frequency gains. One must also remember to absorb any impedance the source may have into the RC filter as the source will also add its own impedance to the network.

If the series resistance and/or reactance is increased the amount of noise at the output will be decreased. The series reactance can be increased with the use of an inductor in series with the resistor (see Figure 4). This is more advantageous then adding more resistance due to the fact that it does not produce a large DC voltage drop.

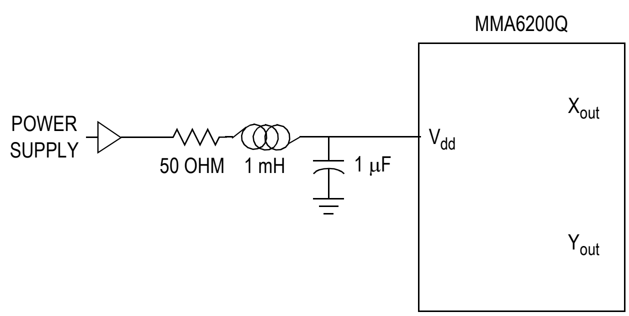

Figure 4. Recommended RCL Input Loading for PSRR at V_{dd}

The device was designed to operate with 3.3 Vdc at V_{dd}. If this input voltage is allowed to drop by more than half a volt the device may not operate correctly; hence the use of an inductor. With the use of an application board there was found to be greater than a factor of two drop in the output noise at the first harmonic with the use of the 1 mH inductor. The later harmonics incur a larger improvement due to the higher reactance of the inductor at the higher frequencies. As a result there was greater than a factor of eight improvement with the third and fifth harmonics. This RC and RLC circuit produced the following PSRR plot (see Figure 5).

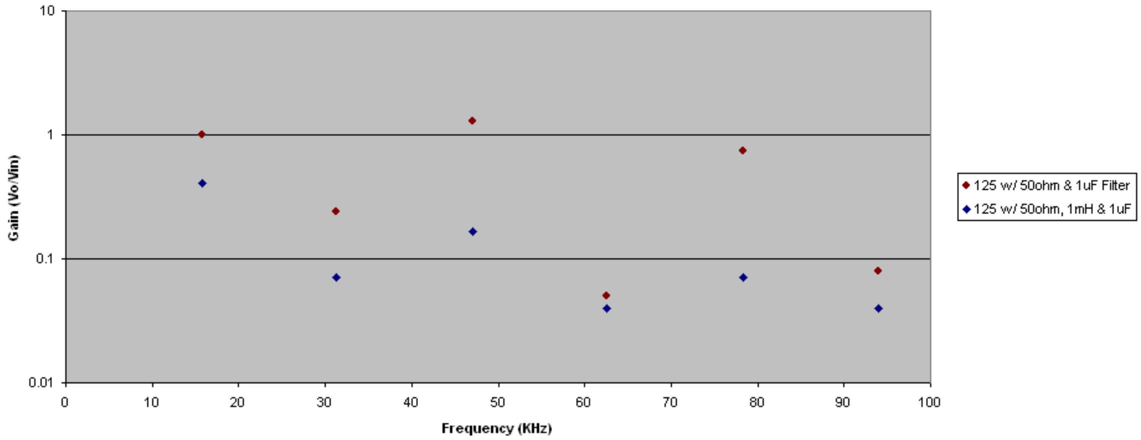

Figure 5. PSRR with RC and RLC Input Filter

If a smaller capacitance is desired in application with no inductor one can increase the value of just the series resistor. However one must take into consideration the tradeoffs involved. In order to get roughly the same improvement in the PSRR with a 0.5 μF capacitor as there was with the 50 ohm and 2 μF RC combination one must increase the series impedence to 150 ohms (see Figure 6).

This alternate RC circuit produces the following effect on the PSRR (see Figure 7). Notice the similarity in the gain when compared with the 50 ohm 2 μF filter. It is still well below unity for this configuration.

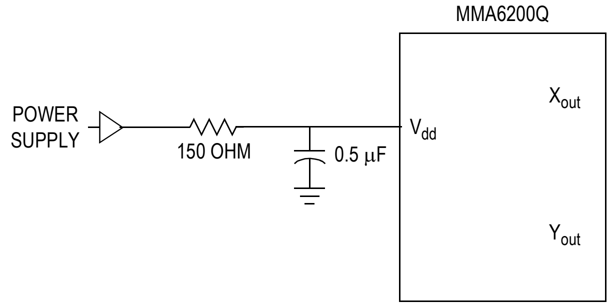

Figure 6. Alternate RC Input Loading for PSRR at V_{dd}

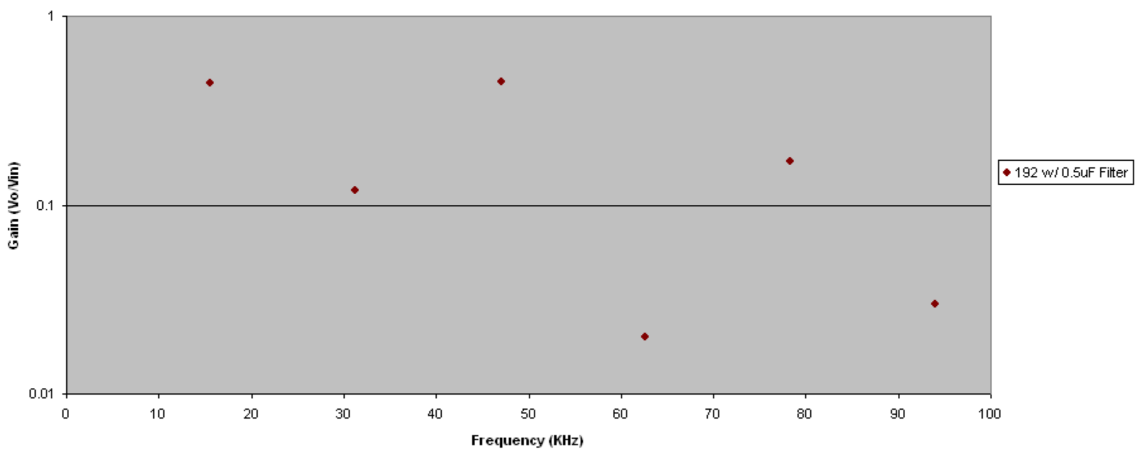

Figure 7. PSRR with 150 Ohm and 0.5 μF Input Capacitance

As stated before this large value of resistance creates a DC voltage drop at the input of the device. However, it could be reduced some and still achieve less than unity gain. With the same voltage at the input of the filter the output voltage of the device is lowered. In this case it drops by roughly 5 percent. In turn, this loss in DC voltage also lowers the ratio-metric error. However if the voltage at Vdd is allowed to drop much lower than 2.7 volts the device may not operate at all. If cost and space permits, one should consider, as stated previously, the substitution of a series inductor in place of at least part of this series resistance. This can greatly decrease the DC voltage drop problem.

To get a 150 ohm impedance at the frequency of the first harmonic we have X = 2*pie*(15 KHz)*L = 150 ohm. Solving for L gives the somewhat large value of 1.6 mH for the inductor. A 1 mH inductor at 15 KHz has an impedance of about 95 ohms and these devices can be had in quantity (1000 or more) for less then twenty cents each.

CONCLUSION

The MMA6200Q series family of devices require external RC and possibly L components to correct power supply rejection ratio issues caused by noisy power supply lines. This may not be of concern in many applications; however, it may be in some. The preceding gives an introduction to power supply rejection ratio as well as some information to better understand this potential problem. Also included are some example filters, the effects on PSRR, as well as suggested choices.

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Japan:
Freescale Semiconductor Japan Ltd.
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ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
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