AN1941

Modeling Thermal Effects in RF LDMOS Transistors

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INTRODUCTION

The temperature effects in high power amplifiers are an important consideration when simulating in an elevated temperature environment. An improperly modeled biasing network can show a required gate voltage (V_{GS}) for a desired current probe (I_{DS}) that may be completely inaccurate. As an example, this application note illustrates the different results obtained from a simulation using two models: Motorola's MRF19125 Root model and MET (Motorola Electro Thermal) model. All examples contained within this application note are based on simulation results from Agilent® EEsof® EDA Advanced Design System (ADS).

ROOT MODEL

The Root model is a data–based model that is created from the HP Root FET Model generator. The model generator creates a device–specific, large–signal model from small–signal S–parameter and measured DC data. The Root model predicts device performance as a function of bias, frequency and power level. This model enables circuits to be simulated that contain devices for which measured data exists but good physical or empirical models do not.

MET MODEL

The MET model is an electro thermal model that can account for the dynamic self–heating effects inherent in high power RF LDMOS transistors. The LDMOS MET model is an empirical large–signal, nonlinear model. The MET model can accurately represent the current–voltage characteristics and their derivatives at any bias point and temperature.

Two simulations are illustrated in this application note. Figure 1 shows the generic components used for the simulations. The first simulation compares the Root and MET models and shows the potential errors associated with the Root model vs. the MET model at higher quiescent currents. The second simulation is a sweep of heatsink temperature and shows the effect of temperature on the current probe (I_{DS}) at various gate voltages (V_{GS}) at a constant drain voltage (V_{DS}).

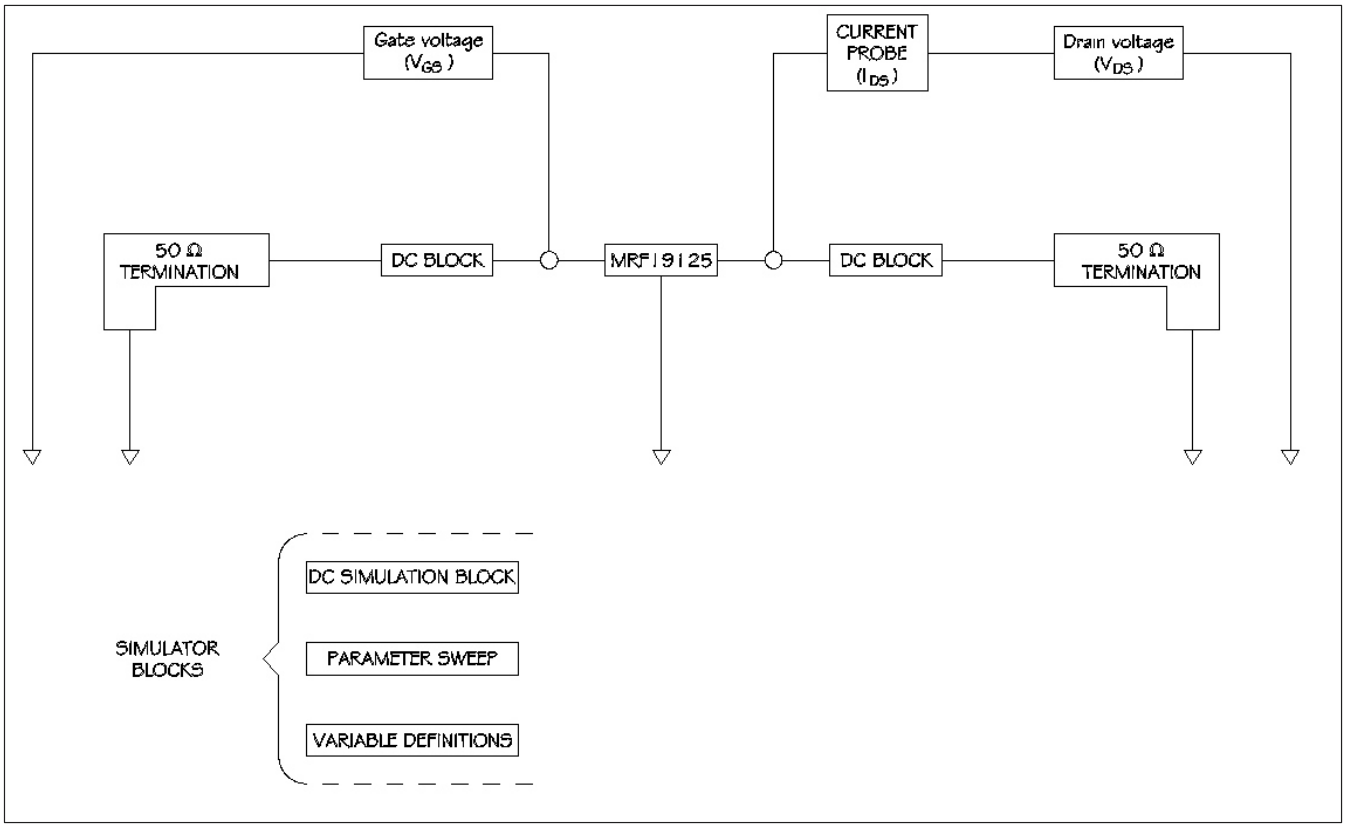

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Figure 1. Basic Block Diagram of Generic Components Used to Set Up Simulation

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ROOT MODEL VS. MET MODEL SIMULATION SETUP

In the Root vs. MET model simulation, a family of curves is generated using a basic DC simulation (DC1) and a parameter sweep (Sweep1) (Figure 2). The simulator outputs IV curves for the Root and the MET models superimposed on each other.

- Variables are defined as I_{DS}, V_{GS}, V_{DS} and T_{FLANGE} (Δvoltage, $\Delta V = \Delta°C$, from the dynamic heating effect).
- The DUT is terminated with 50 Ω termination ports.
- DC blocking caps with values appropriate for the band of operation are used.
- Parameter Sweep is set up with V_{DS} defined as the global sweep variable.
- DC1 calls on a separate simulation named Sweep1, which then sweeps V_{GS}.

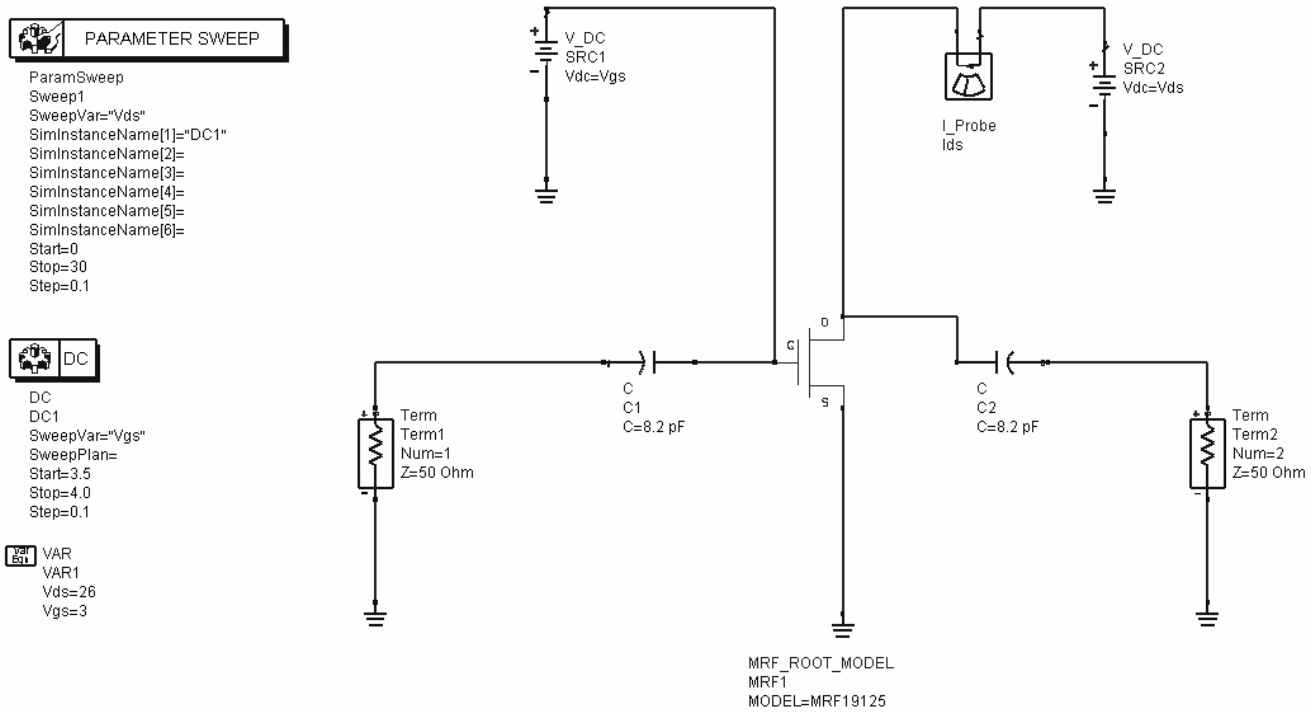

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Figure 2. ADS Schematic Used for MRF19125 Root vs. MET Model Simulation

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TEMPERATURE SWEEP SIMULATION SETUP

In the temperature sweep simulation, another family of curves is generated using the same simulator blocks, DC1 and Sweep1 (Figure 3). The following changes are made to sweep temperature:

- Variables are defined as Ids, V_{GS}, V_{DS} and T_{FLANGE} (voltage equivalent to die temperature, 1 V/1°C).
- The DUT is terminated with 50 Ω termination ports.
- DC blocking caps with values appropriate for the band of operation are used.
- Parameter Sweep is set up with V_{GS} defined as the global sweep variable.
- DC1 calls on a separate DC simulation named Sweep1, which then sweeps T_{SNK}.

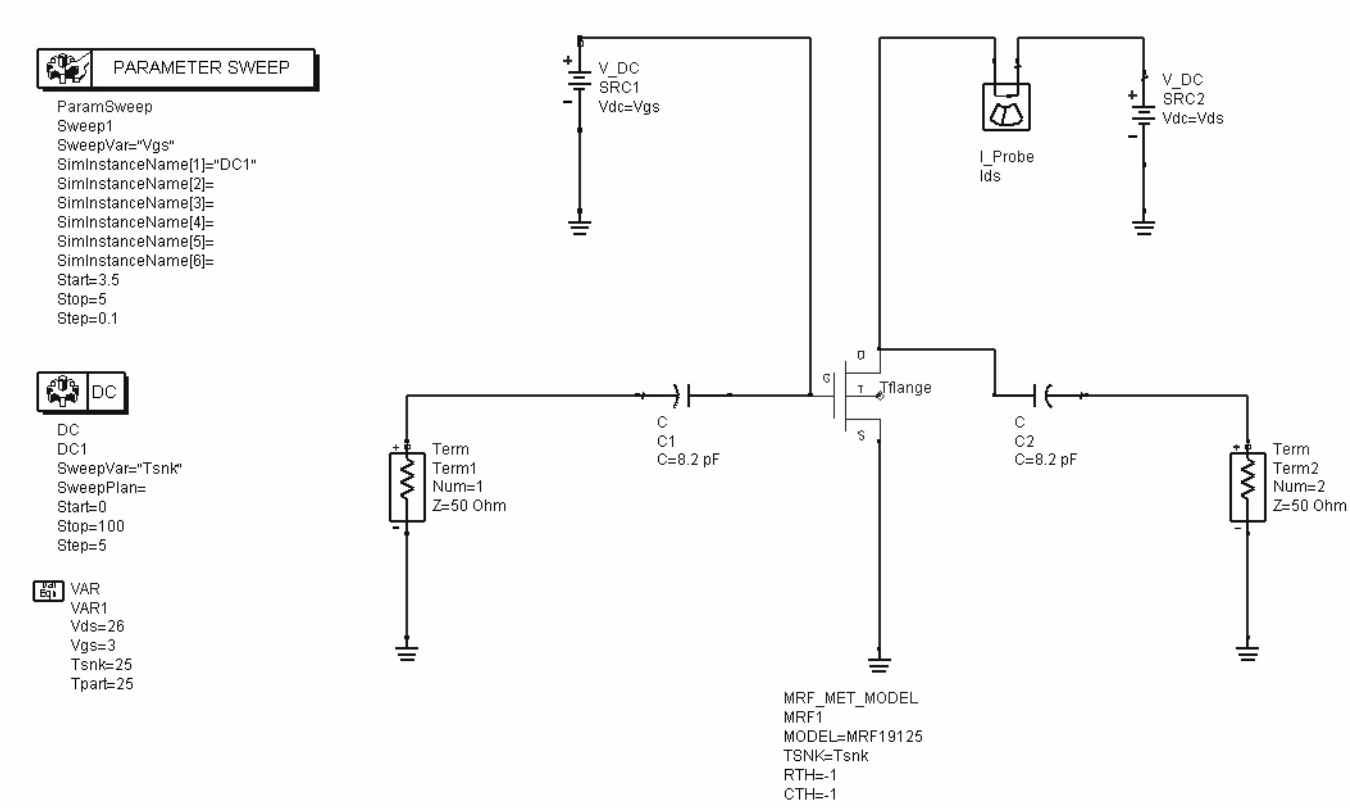

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Figure 3. ADS Design Used for the Temperature Sweep Simulation of the MRF19125 MET Model

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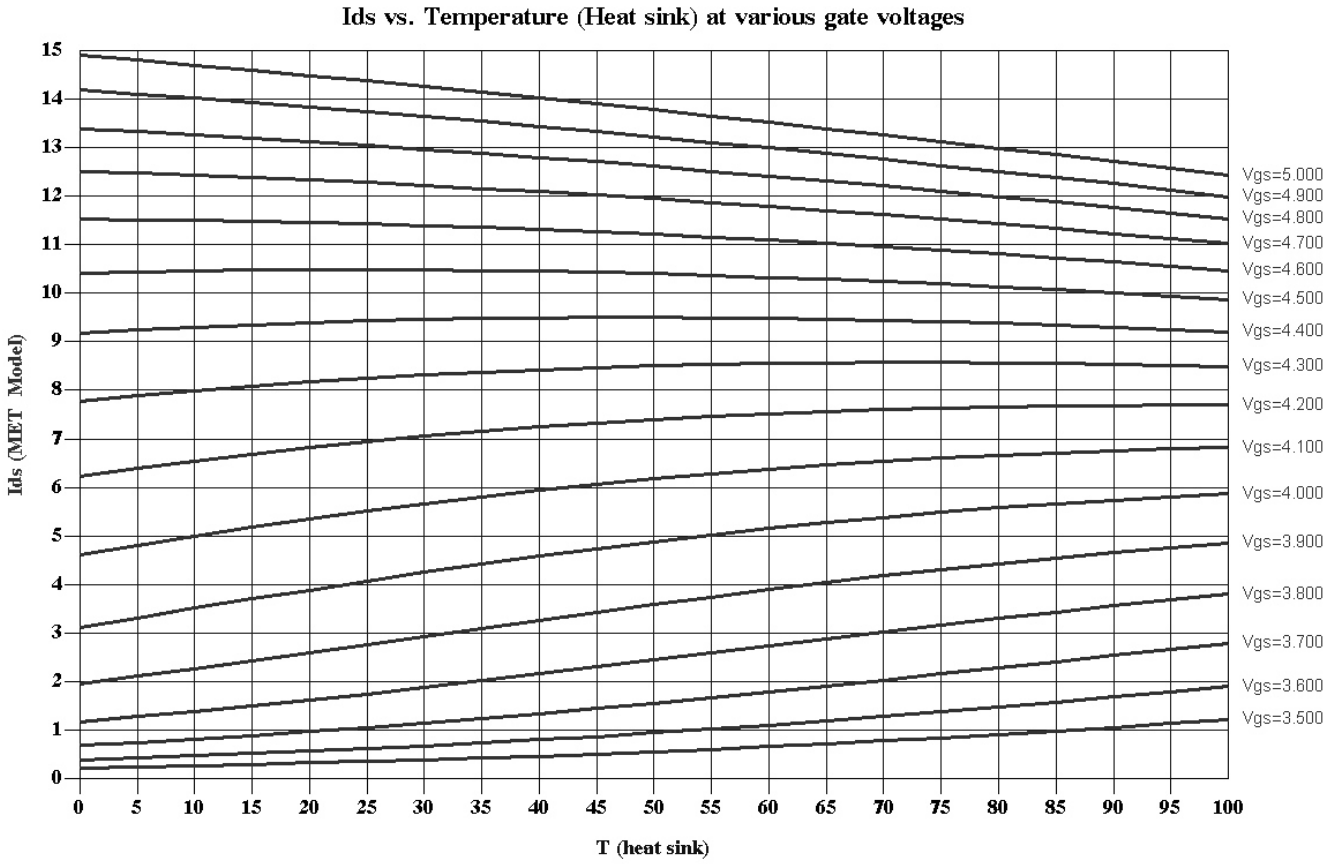

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Figure 4. MET Model $T_{(heat\ sink)}$ Sweep Simulation at Constant V_{DS} and Parametric Values of V_{GS}

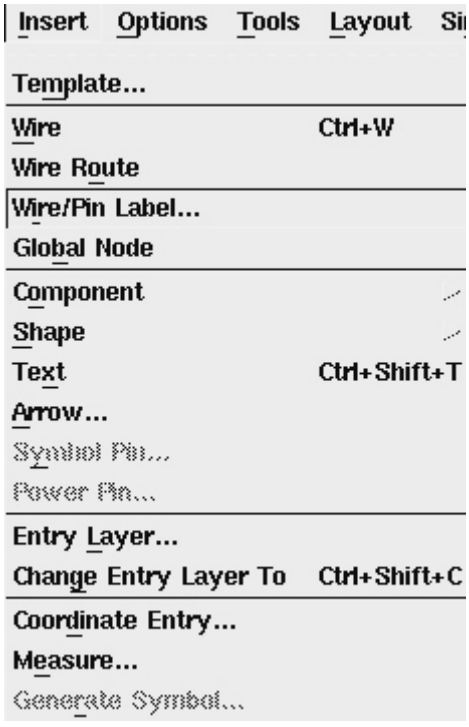
RESULTS

The results shown in Figure 4 illustrate the importance of careful selection of a fixture's operating temperature and V_{GS}. At lower quiescent currents (200 mA to 1000 mA), the drain–source current has little dependence on temperature. However, at higher levels of current (1000 mA to 3000 mA), the greater slope of the curves indicates the increased dependence on temperature. Figure 4 does not directly show the effects of die temperature because $T_{(heat\ sink)}$ is the temperature taken at the flange, not on the die. To plot I_{DS} vs. $T_{(die)}$, the following equation is needed to solve for $T_{(die)}$ directly at each V_{GS}:

$$T_{(die)} = T_{(heat\ sink)} + T_{(flange)}$$

- $T_{(heat\ sink)}$: User–defined as a constant.
- $T_{(flange)}$: Calculated by ADS. The thermal port on the part must be labeled using the WIRE/PIN LABEL function with the identical variable as in the equation. The WIRE/PIN LABEL function allows wires or pins to be defined with labels that can be used during simulation or in post–simulation calculations.

1. From the design file, click on Insert | Wire/Pin Label:



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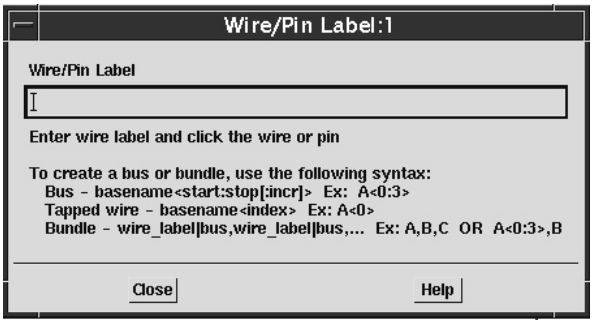
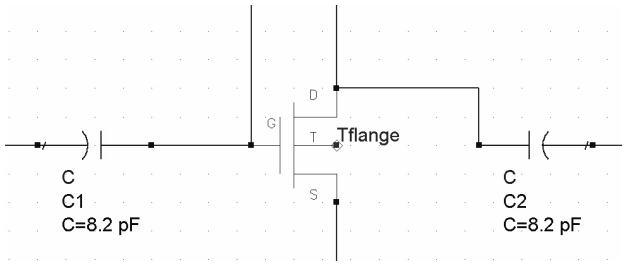
2. Enter the label for the thermal port.



3. Click on the port labeled “T” on the DUT.
4. The thermal port has been labeled.



5. ADS then calculates $T_{(flange)}$ using the following equation:

$$T_{(flange)} = \theta_{JC} * P_{DISS}$$

The thermal resistance, θ_{JC}, is predefined by ADS as R_{TH}. The data sheet value for this will be used if the user sets $R_{TH} = -1$.

CONCLUSION

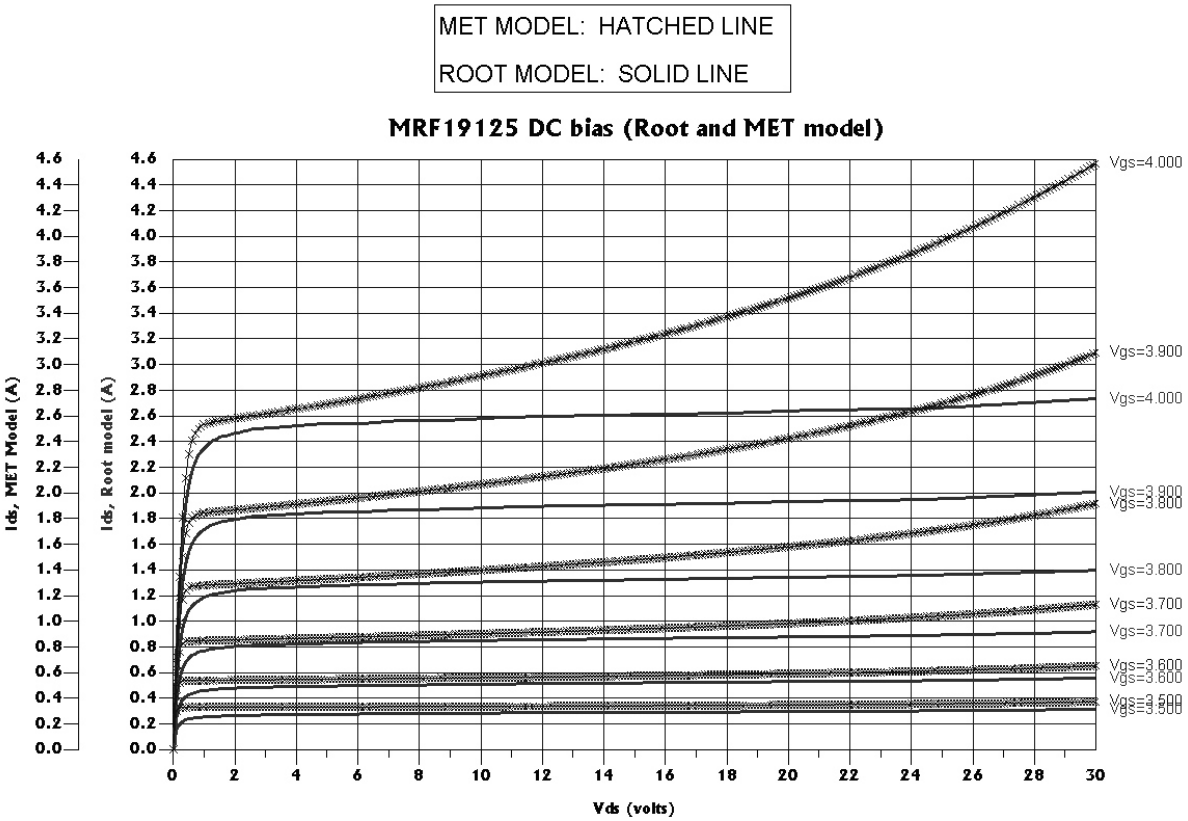
Figure 4 shows the overall T_{FLANGE}, I_{DS} and V_{GS} characteristics. The data from this multivariate plot can be used in an RF simulation in conjunction with other RF characteristics, such as drain efficiency, to create a more accurate expression for V_{GS}. This would be equivalent to a temperature compensation circuit.

Figure 5 shows the superimposed IV curves of the Root model and the MET model at 25°C and illustrates the potential for error between the two models. As shown, the models tend to agree with each other at lower V_{DS} and lower I_{DQ}. However, the models tend to deviate at more practical levels of drain–source currents and voltages. A typical bias condition for the MRF19125 is V_{DS} = 26 V with a quiescent current of 1100 mA. The Root model shows that the required gate voltage is approximately 3.79 V, whereas the MET model more accurately shows the required gate voltage to be 3.71 V. Although the difference of only 80 mV between the two models may seem insignificant, it would account for a difference of 600 mA in I_{DQ} at this drain voltage.

There are advantages and disadvantages for using each of the model types in more advanced RF simulations in ADS. These topics are beyond the scope of this application note and will be discussed in subsequent ADS user application notes.

To access all Motorola RF LDMOS Model libraries, go to:

http://www.motorola.com/rf/models



NOTE: For better viewing on the Web of Step 4 graphic and Figure 5, click on link for larger versions of graphics.

Figure 5. Root and MET Model IV Curves Superimposed

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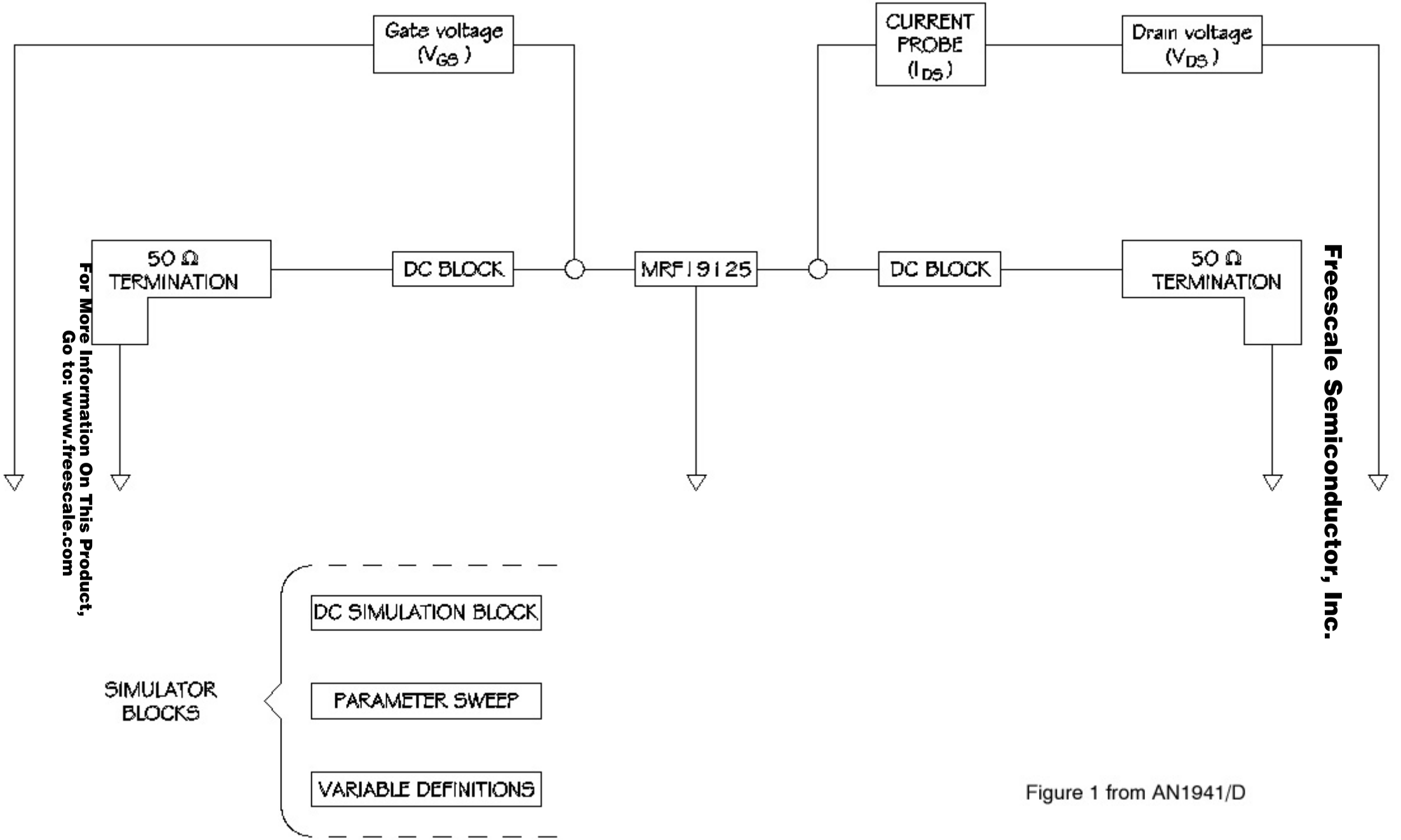

Figure 1 from AN1941/D

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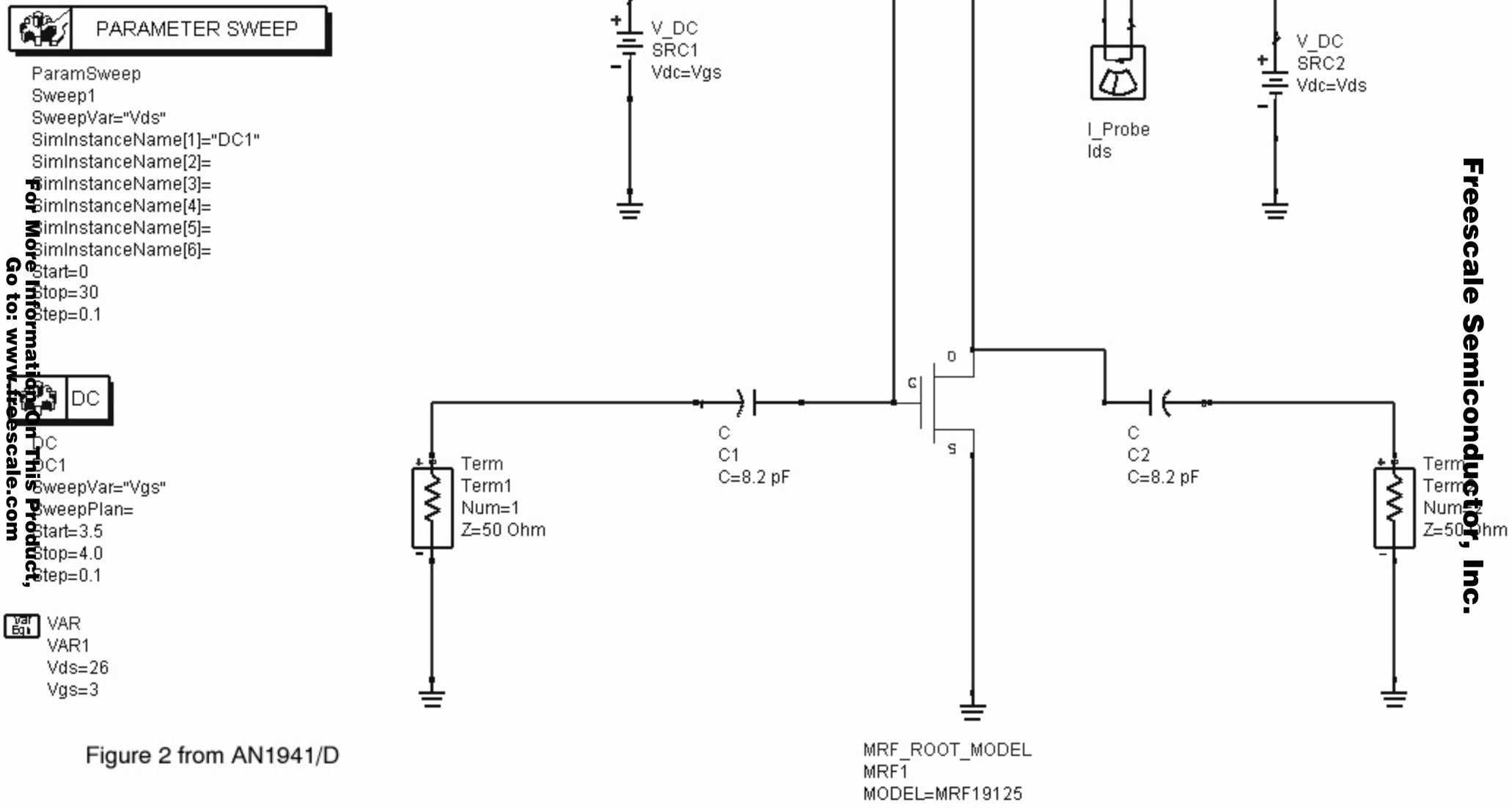

Figure 2 from AN1941/D

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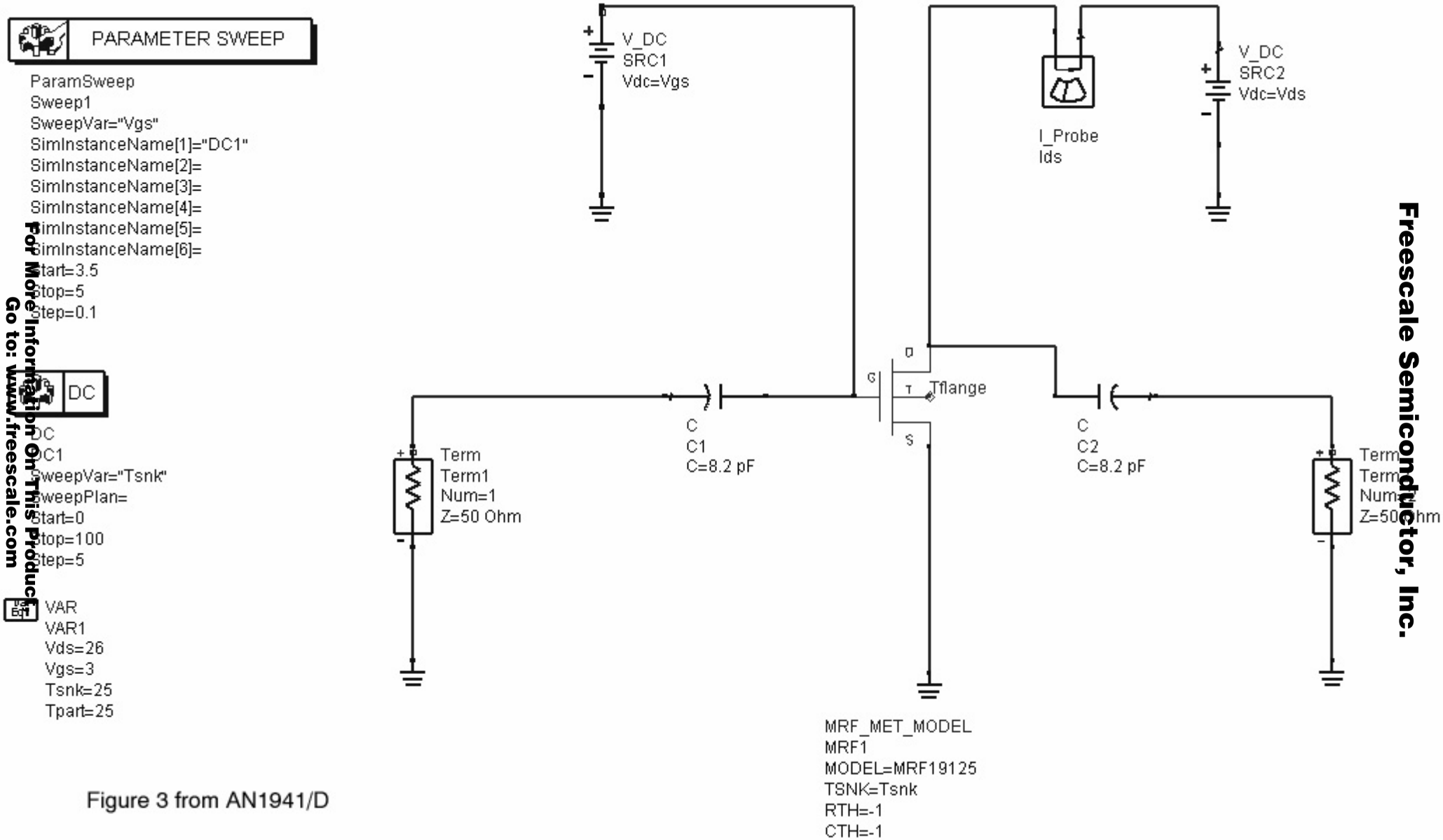

Figure 3 from AN1941/D

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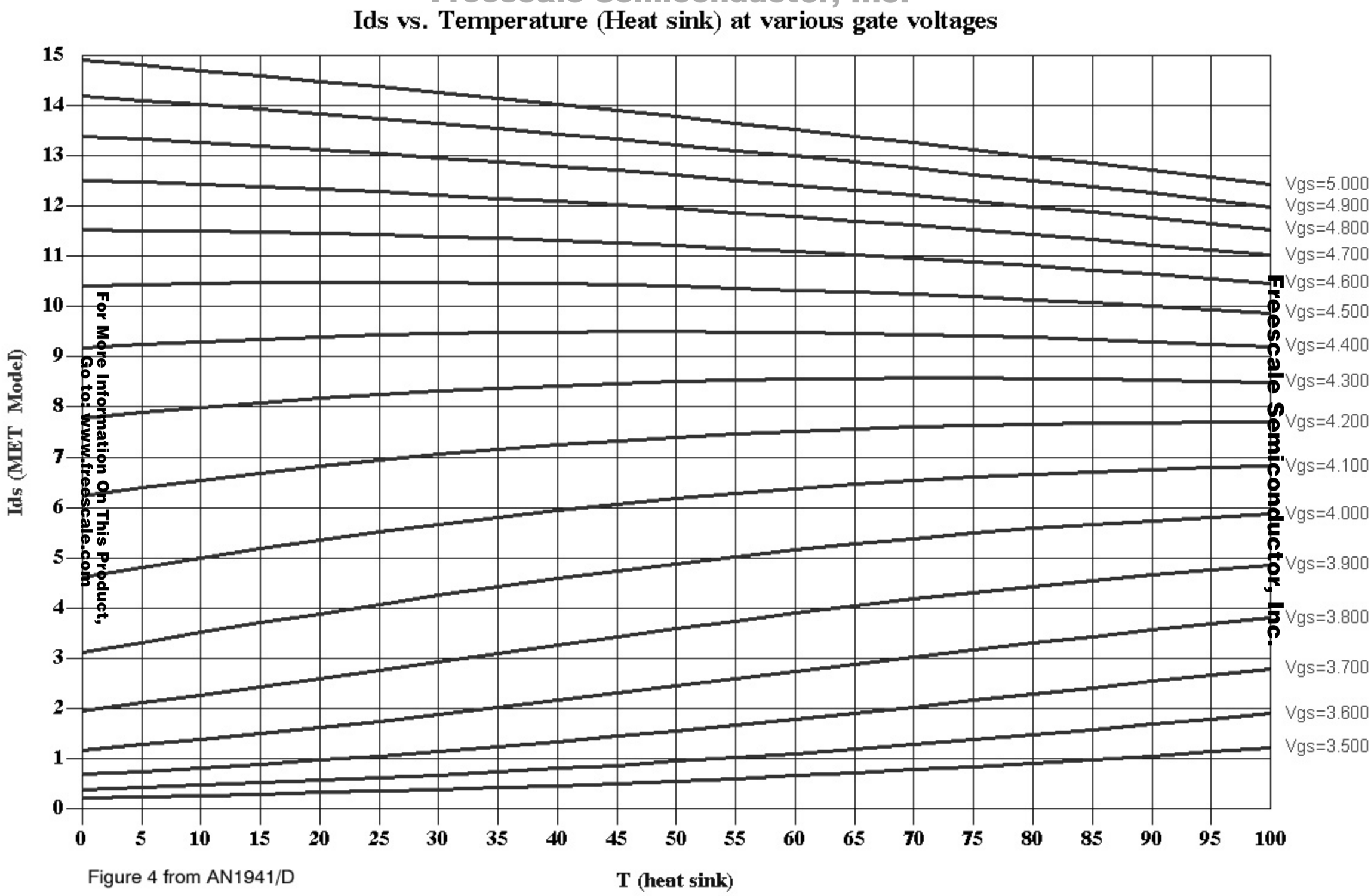

Figure 4 from AN1941/D

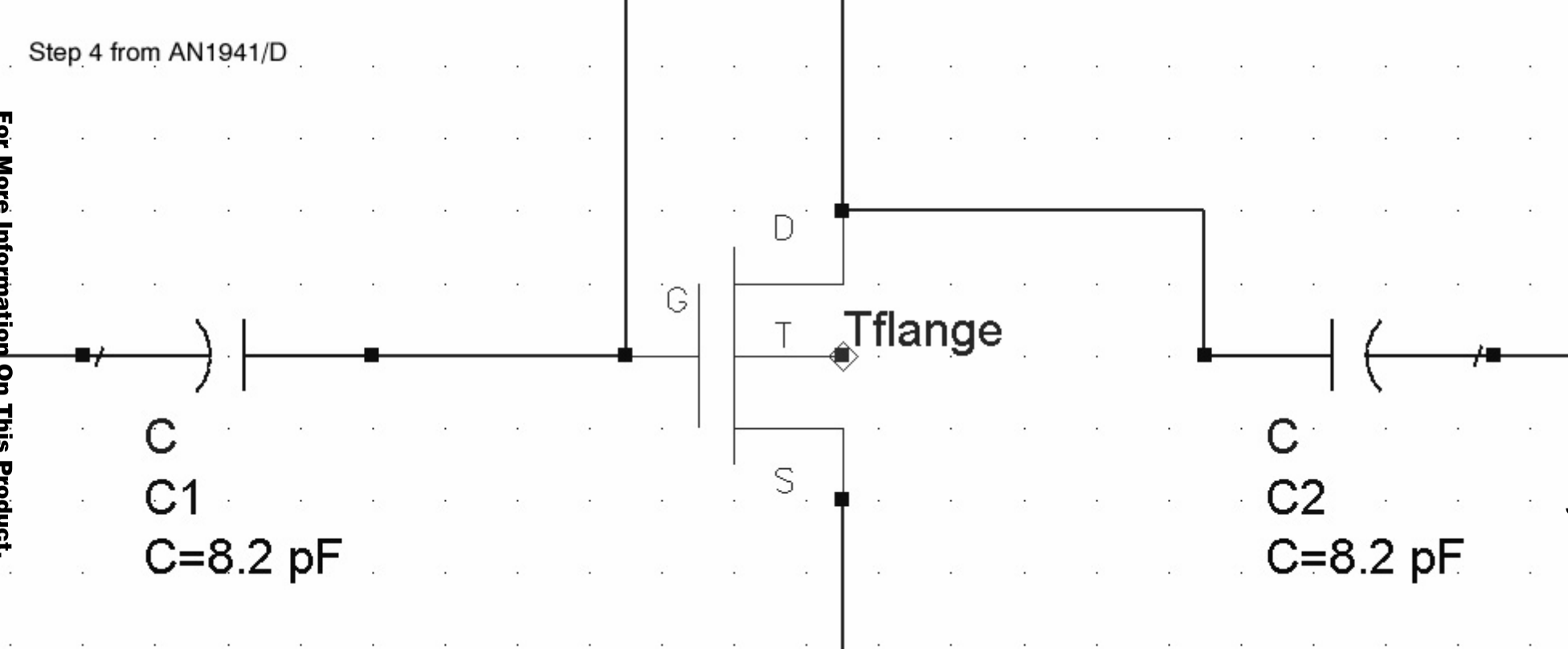
Step 4 from AN1941/D
D
G
T
Tflange
S
C
C1
C=8.2 pF
C
C2
C=8.2 pF

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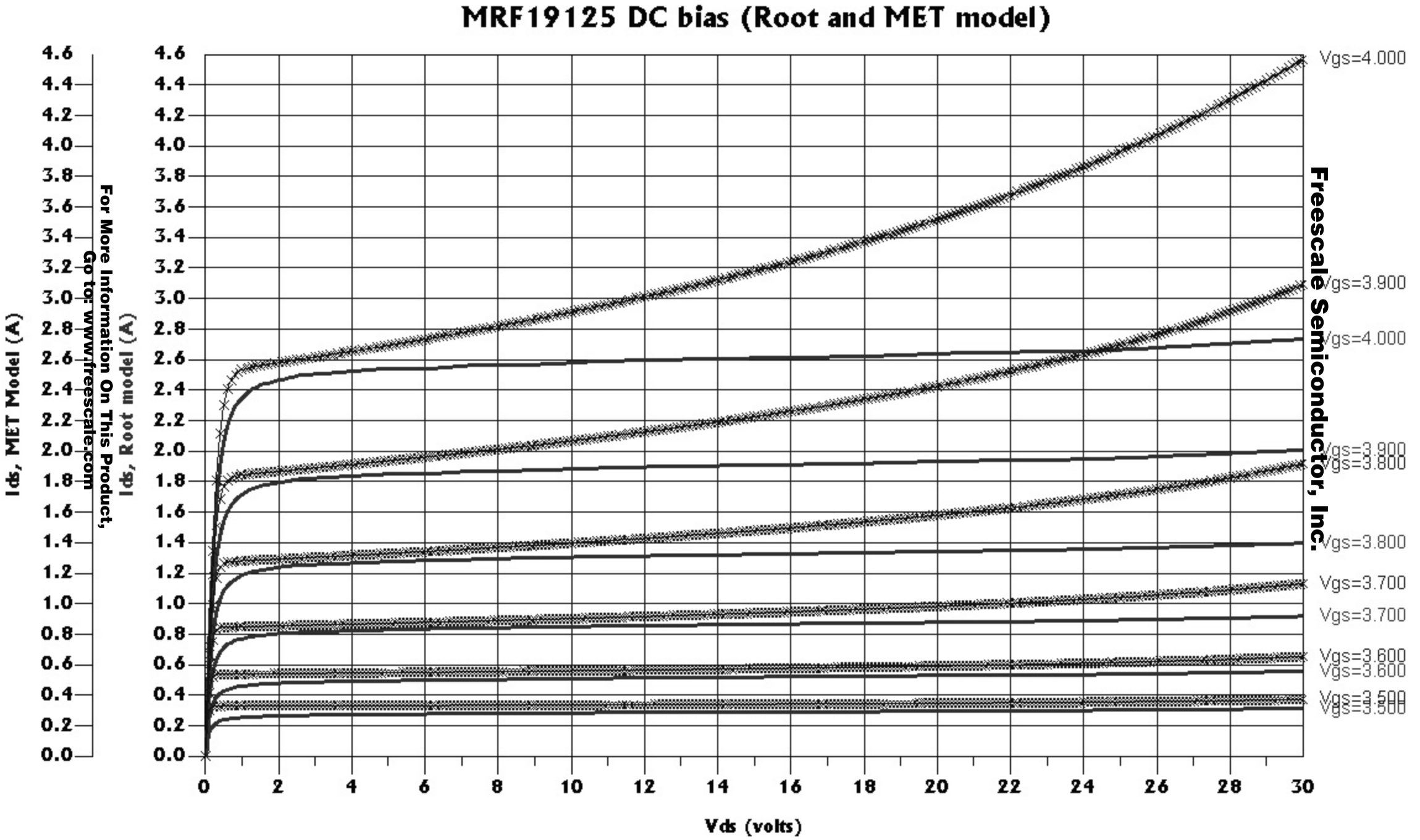
Figure 5 from AN1941/D

MET MODEL: HATCHED LINE

ROOT MODEL: SOLID LINE



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