AN1889
APPLICATION NOTE

ESBT
STC03DE170 IN 3-PHASE AUXILIARY POWER SUPPLY

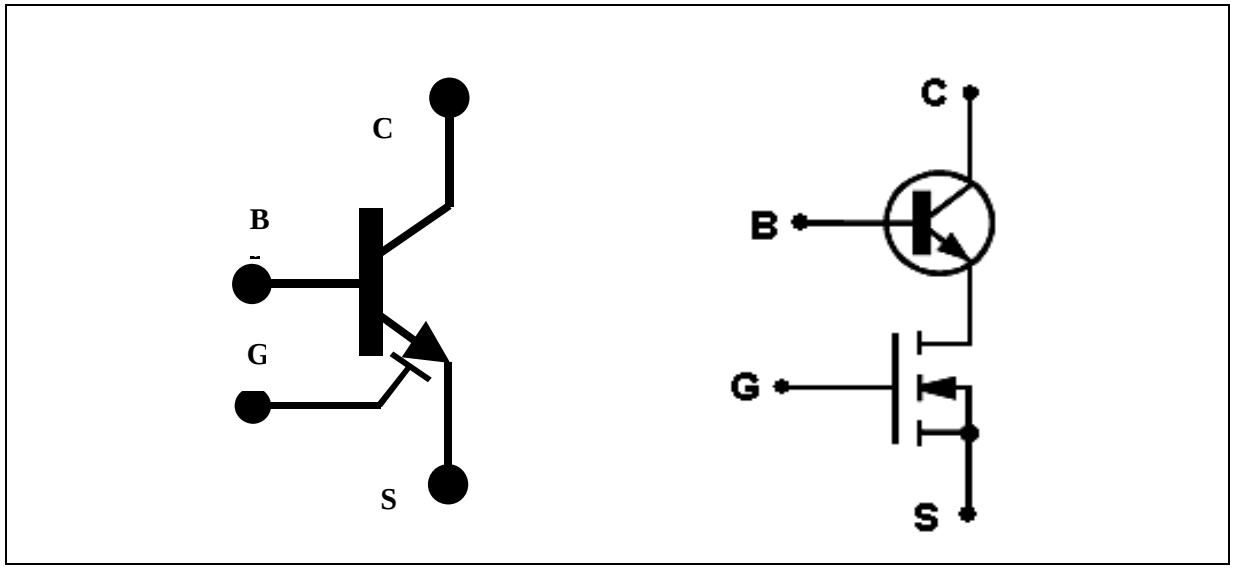
1. INTRODUCTION

The need to choose a high value of the fly-back voltage is well known to power supply designers when efficiency and high duty cycle become important requirements. Three-phase auxiliary power supplies, starting from a bulk voltage of 750V, require theoretically power transistors with a block voltage capability higher than 1200V. Practical considerations linked to better efficiency and safe margin may impose to choose devices with even higher breakdown voltage (i.e. 1500V, 1700V). Looking at the power switches currently available, while power bipolar transistors are strongly limited in switching frequency operation, power MOSFETs show a much lower current capability, which may limit their use to low power applications. Recently available in the market, the ESBTs (Emitter Switched Bipolar Transistors) represent a valuable and cost effective alternative for all those applications where high voltage and high switching frequencies are a must.
This application note describes the realization of a 50W 3-phase auxiliary power supply by using the STC03DE170 as main switch for the fly-back converter. Particular attention has been given to the transformer design as well as to the ESBT driving circuit requirements.

2. ESBT: THEORY AND EVOLUTION

The "emitter switching" concept was widely investigated a few decades ago with the aim of improving the trade-off between switching and conduction losses mainly in high voltage applications.

Figure 1: ESBT Symbol and Equivalent Circuit



The configuration can be easily implemented by using discrete components and basically consists in a high voltage Power Bipolar Transistor driven by a low voltage Power MOSFET, the two devices result connected in cascode configuration, as shown in fig.1. It is clear that the structure requires two supplying sources: one to ensure the necessary current to the base of the power bipolar transistor and the second to drive the gate of the Power MOSFET. Practically, the Power Bipolar Transistor is biased with a constant voltage source between its base and ground while a PWM controller could directly drive the gate of the Power MOSFET.

The On condition is guaranteed just by switching on the Power MOSFET. Being the On voltage drop on the Power MOSFETs negligible compared the $V_{CE(sat)}$ of the power bipolar transistor, we can consider as a first approach the emitter of the power bipolar transistor grounded as shown in fig.2a.

The driving circuit associated to the base supplies the current needed to saturate the power bipolar transistor, so that the main conduction losses are those related to the $V_{CE(sat)}$ plus the losses on the input of the power bipolar transistor itself. As a figure of merit, for devices rated at 1200V we can note that the current density (and consequently in reverse proportionality the output voltage drop) on Power Bipolar Transistor is 10 times bigger than that of an equivalent high voltage power MOSFET.

Starting from the ON-state and switching off the Power MOSFET, the drain current falls instantaneously down to zero, so that the output current changes its path to the ground through the base of the transistor itself (see fig.2b).

Figure 2: ESBT Switching Operation

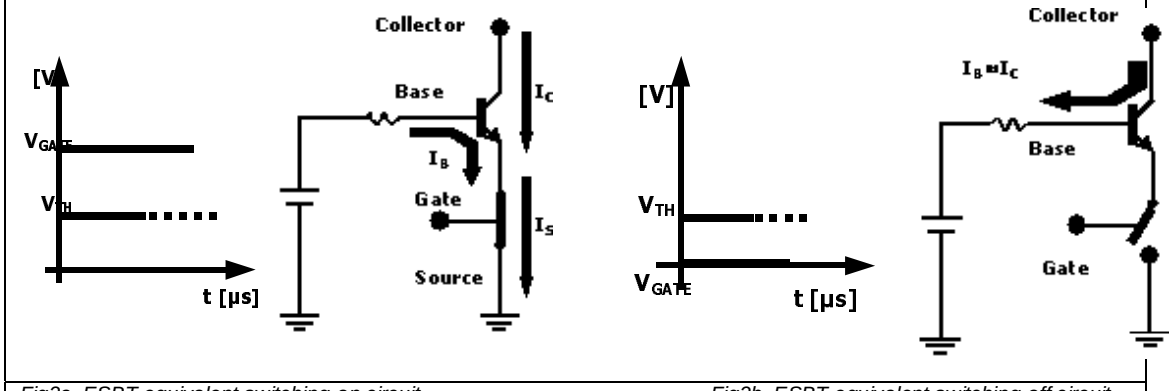
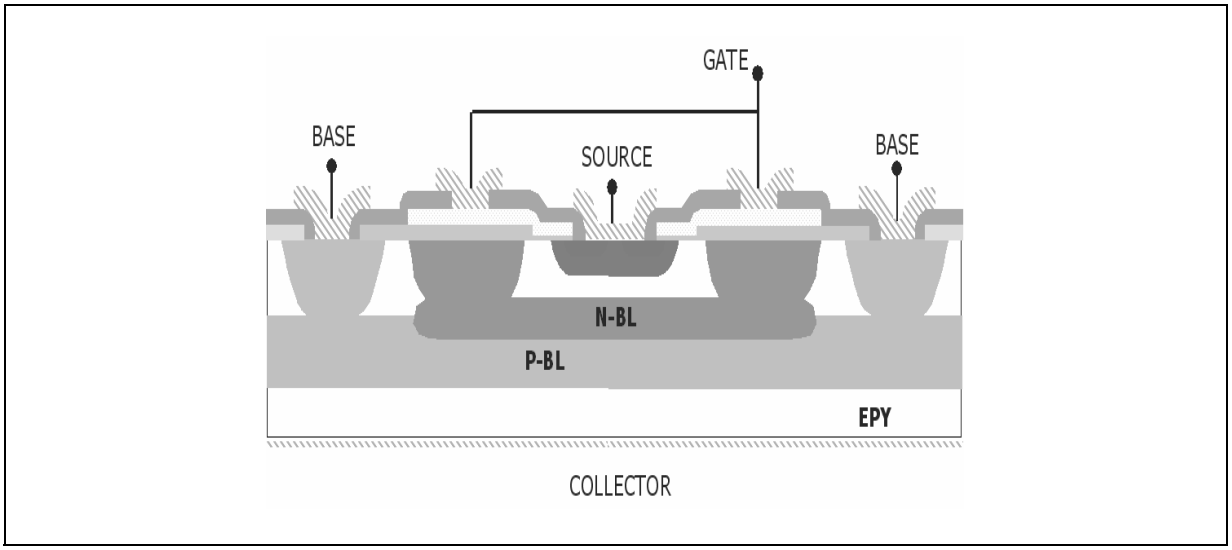


Fig2a. ESBT equivalent switching-on circuit *Fig2b. ESBT equivalent switching-off circuit*

Being the negative base current equal to the collector current, the resulting turn-off time is by far lower than any traditional power bipolar transistor and comparable with that of a high voltage Power MOSFET. In fact, thanks to the floating emitter configuration, the high value of the reverse base current results in a fast removal of the charges stored in the base, achieving both reduced storage time and, most important, the structure results virtually free of that tail current that characterizes all power bipolar based devices. It is worth to be noted that the configuration gives an extra safety margin in reverse safe operating area, by increasing the ruggedness versus the secondary breakdown, in fact since the emitter is open the phenomenon of crowding current under the emitter finger (with possible creation of hot spot) is practically absent.

Cascode configuration can be implemented in a single four or five pins package either as hybrid or as a monolithic single chip solution that combines a vertical NPN Power transistor and a low voltage standard MOSFET. The choice of a suitable value of thickness and resistivity for the collector drift layer coupled with the most appropriate edge termination allows in principle to design devices with blocking voltage up to 3.5 KV. The integration of a low voltage Power MOSFET inside the monolithic structure had represented the main challenge in designing the ESBT. In particular the power MOSFET has been integrated inside the emitter region of the Power bipolar stage realizing a sort of a sandwich structure: thanks to the adopted solution the silicon area depends only by the BJT size in spite the whole switch is formed by the series connection of the two devices.

Figure 3: ESBT Cross Section



As shown in figure 3, a DMOS structure is diffused on a higher resistivity layer overlaying the highly doped emitter region (NBL in the cross section). In terms of diffused and deposited layers the DMOS structure is quite similar to that of a standard low voltage power MOSFET even if, of course, its layout is arranged to match the emitter geometry of the BJT stage. Finally the base contact are placed on a diffused layer deep enough to reach the base buried layer (PBL).

As previously mentioned to switch-on the ESBT it is necessary to positively bias the gate with a voltage higher than its threshold (typically 3.5 V for the device in subject), this will generate, like in all voltage driven transistors, the inversion of the portion of the body region under the gate oxide of the vertical n-channel MOSFET, so that the emitter results connected to the ground. In the mean time the base driver supplies the current needed to saturate the BJT stage leading the ESBT to a high on-state current density due to the high injection of electrons from the N+ emitter region, similarly to the case of pure power bipolar transistors. The On-voltage drop is represented by the Collector-Source saturation voltage, say the $V_{CS(sat)}$), and it is consequently given by the contribution of the $V_{CE(sat)}$ of the bipolar stage plus the small voltage drop of the low voltage MOSFET. Being the bipolar behavior predominant, the voltage drop results not very sensitive to the temperature variations.

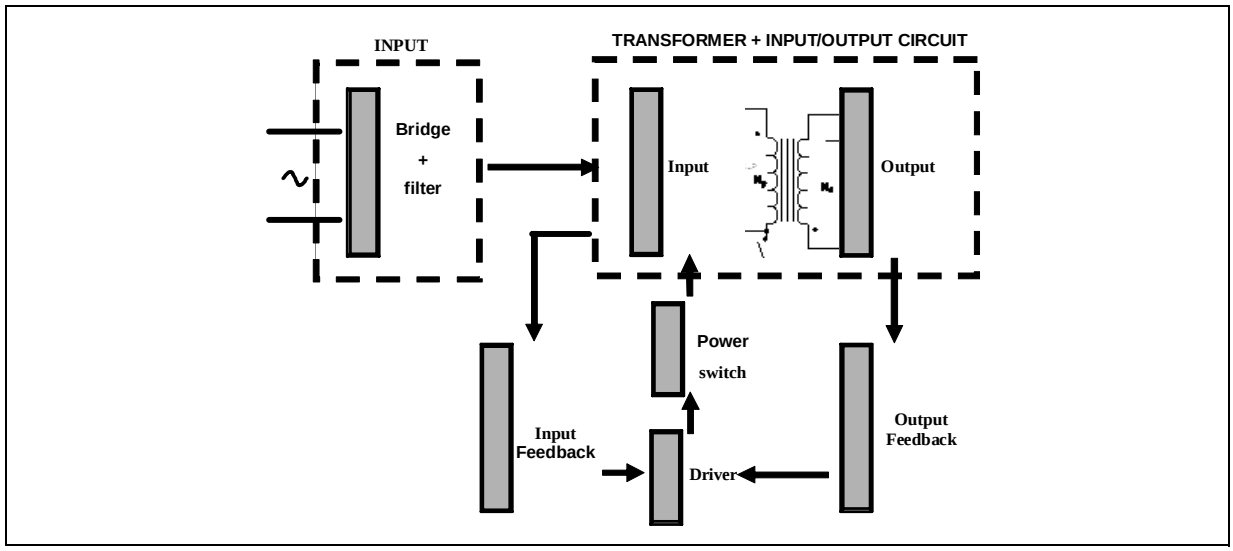
With zero bias in the gate and with grounded base the device behaves like a reverse biased diode during the off state. The switching-off behavior had already been deeply analyzed at the beginning of this chapter. It is important to add that the sandwich structure gives an uniformity of the current density across the whole area of the device. In fact the MOSFET placed over the BJT (in series with its emitter) acts as a sort of "ideal ballast emitter resistor" for all of the elementary cells that form the whole transistor. This

gives to the device not only excellent power dissipation but also the suitability to be paralleled with similar devices.

3. APPLICATION DESCRIPTION

An auxiliary power supply can be schematized in its main functional parts as illustrated in the simplified block schematic diagram shown in figure 4.

Figure 4: SMPS Simplified Block Schematic Diagram



Basically the input voltage is rectified and filtered first, then transferred to the primary side of the transformer directly through the input circuit of the transformer. This part of the power supply fixes the voltage clamping at the desired value, the start-up network is also present in this block to ensure the functionality of the converter during the first pulses. The blocks power switch and driver, by converting the waveforms from continuous state into alternated high frequency, allow the transformer, generally operating in discontinuous fly-back mode, to transfer the stored energy to its secondary side and then to the load through the output circuit. This basically consists in an ultrafast p-n diode (or Shottky diode) + bulk output capacitor fixing the maximum acceptable output ripple. When necessary, for a more precise and lower ripple level, an additional LRC block, working as output post filter network, can be added.

Power regulation can be achieved through the blocks input feedback (primary regulation) or output feedback (secondary regulation). By giving to the driver information on the load requirement, they adapt the input power varying the duty cycle accordingly.

This application note illustrates all design steps needed for the project of a 50W 3-phase fly-back converter in discontinuous mode using an ESBT as primary switch.

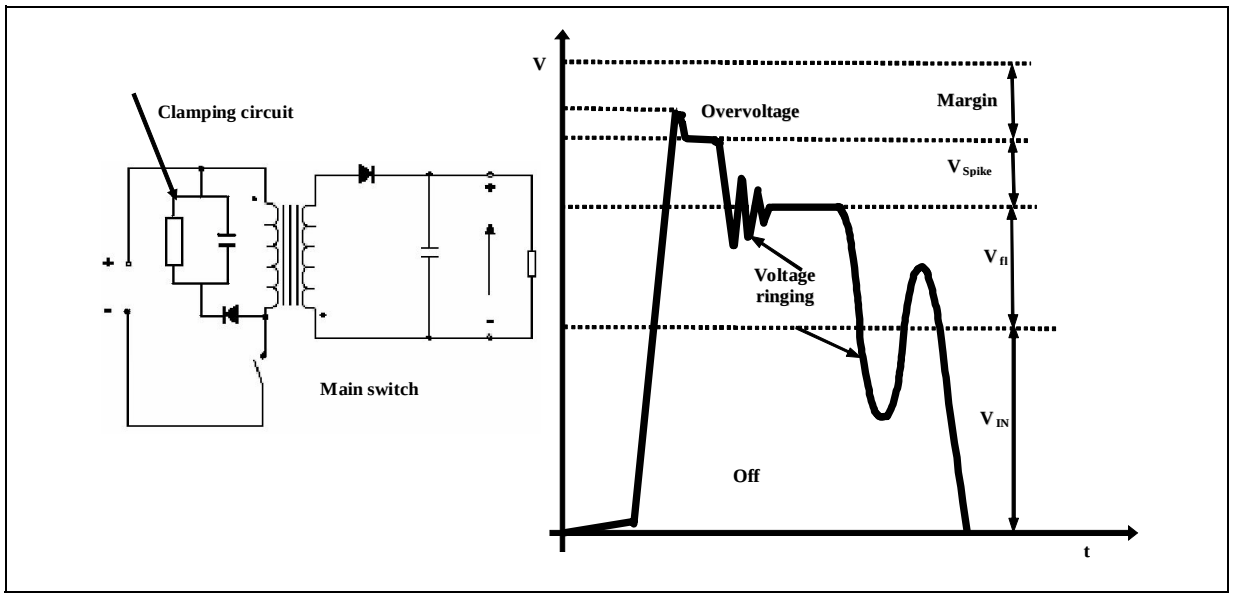
In this application note the bridge diode + filtering will not be analyzed while the output circuit will be just mentioned. Most of the attention has been focused on the transformer design and on the optimization of the driving circuit of the ESBT to allow better performance in practical applications.

Theoretical results had been validated through a realization of a demo board, its electrical parameters and component will be shown step by step in the next paragraphs and summed up at the end of the present note.

4. PRE-DESIGN REQUISITE

Figure 5 below reported shows the simplified fly-back schematic plus the voltage qualitative behavior (not in scale) that the switch has to sustain during turn-off operation (Point T in the figure).

Figure 5: Simplified Fly-back Schematic Diagram



V_{IN} is the maximum input rectified voltage that in 3-phase auxiliary power supplies can be as high as 750V.

V_{fl} is the reflected fly-back voltage; this is one of the most important parameter in the transformer design since the input-to-output turn ratio strongly depends on it. The voltage ringing across V_{IN} is generated by the primary inductance that resonates with the equivalent capacitance at the point T in the figure. This capacitance is mainly due to parasitic capacitances of the transformer and main switch.

V_{spike} is the voltage generated by the leakage inductance of the transformer at primary side. It must be noted that the energy generated by the mutual inductance at the primary of the transformer cannot be transferred to the secondary until the leakage inductance is fully demagnetized. It is the clamping circuit that fixes the value of the voltage at which the demagnetization process occurs. The voltage ringing in the figure across V_{fl} is generated by the leakage inductance that resonates with the equivalent capacitance at point T mentioned before.

The highest overvoltage peak is due to the delay of the diode in the clamping circuit. A good safety margin must take care of this overvoltage and some transient spikes at start-up.

Transformer design is the major part in a power supply project. A few degrees of freedom are available to the designer starting from the target data, and most of them are linked each other so that the final project is often achieved through a re-iteration process.

The table below lists the converter specification data and the first parameters that a designer has to fix from scratch when a new project of a fly-back converter is going to be approached. In the last column the values chosen for the present board are reported.

Table 1: Converter Specification Data and Fixed Parameters

Symbol	Description	Values
V_{inmin}	Rectified minimum Input voltage	250
V_{in}	Rectified maximum Input voltage	750
V_{out}	Output voltage	24
V_{AUX}	Auxiliary output voltage	15
P_{out}	Maximum Output Power	48
η	Converter Efficiency	80%
F	Switching frequency	50 kHz
$V_{flyback}$	Reflected fly back voltage	500 V
V_{spike}	Max over voltage limited by clamping circuit	200 V

The first choice to be made is the transformer turn ratio N_P / N_S, where N_P *and* N_S are respectively the number of primary and secondary windings. The calculation of turn ratio is correlated to the maximum voltage rating of the transistor to be used as primary switch. In fact looking at the below formula for fly-back operation, the voltage at the point T in figure 5 is given by:

$$V_T = V_{dcmax} + \frac{N_P}{N_S}(V_o + V_{F,diode}) + V_{Spike} + margin \quad (4.1)$$

Obviously

$$\frac{N_P}{N_S}(V_o + V_{F,diode}) = V_{fl} = \text{the fly-back voltage}$$

and

V_{spike} = the over voltage limited by the clamping circuit

must be chosen from the designer taking care that the total voltage at point T in figure 5 does not exceed the maximum breakdown voltage of the device chosen as power switch according to the formula1.

Once fixed the V_{spike}, the choice of the designer is limited to fix the fly-back voltage taking into account the voltage capabilities offered by the standard transistors available. It is worth noticing that the higher the fly-back voltage the higher the max duty cycle acceptable: higher duty cycle at fixed output power, leads to lower IRMS with a consequent overall better efficiency at primary side and an easier design of wide input range converter.

In this case the use of ESBT, having devices with breakdown voltage capability as high as 1700V can help in that. For the realized demo board with STC03DE170 we can fix:

Margin=250V V_{Spike}=200V

while $V_{F,diode}$ being lower than 1V can be neglected, so that V_{fl} results being 500V. From equation (4.1) we can now easily calculate the transformer turn ratio.

$$\frac{N_P}{N_S} = \frac{BV - V_{dcmax} - V_{Spike} - margin}{V_o + V_{F,diode}} = \frac{1700 - 750 - 200 - 250}{24 + 1} = 20 \quad (4.1a)$$

The second step is to ensure that the converter operates in discontinuous mode, the below formula will guarantee that the energy on the primary coil will be completely transferred to the secondary before the

next cycle occurs

$$V_{dc\,min} T_{on\,max} = \frac{N_P}{N_S}(V_o + V_{F,diode}) T_{reset} = V_{fl} T_{reset} \quad (4.2)$$

The next formula, giving a safe margin, guarantees the complete demagnetization of the primary side.

$$T_{onmax} + T_{reset} = 0.8T_S \quad (4.3)$$

Where T_{onmax} is the maximum on time, T_{reset} is the time needed to demagnetize the transformer inductance and T_S is the switching time.
Combining (4.2) and (4.3) T_{onmax} results being:

$$T_{onmax} = \frac{V_{fl} 0.8T_S}{V_{dcmin} + V_{fl}} \cong 10.66\mu s \quad (4.4)$$

The next step is to calculate the peak current. Fixed the output power to 48W and the desiderated efficiency (80% in this case), we have also the freedom to choose the switching frequency. At this purpose, 50 kHz has been selected. The first step is to calculate the primary inductance. By using an approximated formula that does not take into account the losses on the power switch, on the input bridge and on the rectified network, we have:

$$P_{IN} = 1.25P_{OUT} = \frac{\frac{1}{2} \cdot L_P I_P^2}{T_S} = \frac{\frac{1}{2} V^2_{dcmin}\, T^2_{onmax}}{L_P T_S} \quad (4.5)$$

Hence

$$L_P = \frac{V^2_{dcmin}\, T^2_{onmax}}{2.5 T_S P_{OUT}} = 2.95mH \quad (4.6)$$

From here now we can calculate the peak current on primary.

$$I_p = \frac{V_{dcmin}\, T_{onmax}}{L_P} = 0.9A \quad (4.7)$$

It is important also to determine the maximum value of Irms primary current to fix the number of the primary turns as shown in the next section.

$$I_{rms(primary)} = \frac{I_p}{\sqrt{3}} \sqrt{\frac{T_{onmax}}{T_s}} = 0.38A \quad (4.8)$$

5. FLY-BACK TRANSFORMER DESIGN

Once defined the turn ratio, the needed primary inductance and the peak current, to complete the design of the transformer we still need to determine the magnetic core material, its geometry, and the exact number of primary turns. The choice of correct size and material of transformer is often an iterative process that may require several try and error steps before finding the optimal choice. Standard soft ferrite with gaped core and E-type geometry is a common choice for fly-back operation. The calculation of the product of the areas A_P (cross sectional active area of the core multiplied by window area available for winding) shown in the formula below can help find the dimension of the core.

$$A_p = 10^3 \left[\frac{L_p I_{rms(primary)}}{\Delta T^{1/2} K_u B_{max}} \right]^{1.316} \quad [cm^4] \quad (5.1)$$

Where ΔT is the maximum temperature variation with respect to the ambient temperature, K_U is the utilization factor of the window (say the portion of the window used for winding that generally ranges between 0.4 and 0.7), and B_{max} is the maximum flux in the core.

By the way all ferrite manufacturers report tables with the suggested core type and size for given output power and frequency.

For our project the type ED2924-PC40 ferrite material from TDK has been chosen. Next step is to determine the air gap length (l_g) of the core and the inductance of a single turn (A_L) needed to calculate the exact number of primary turns.

The core must not saturate even at high temperature and in overload conditions (like start-up or secondary short circuit), the level of this current in the present project can reach 1.6A. By imposing the I_{DCmax} =1.8A for safety margin, ferrite's manufacturer supplies the following values for the selected ED2924-PC40 core:

$l_g = 0.8$ [mm] $A_L = 0.13$ [mH]

By knowing A_L, the exact number of both primary and secondary turns can be easily calculated.

In fact, being the primary inductance:

$$L_P = N_P^2 A_L \quad (5.2) \qquad \Rightarrow \quad N_P = 150$$

Finally from formula (4.1a) $N_S = 7.5$

The closest higher integer has been chosen for the demo board

$$N_S = 8$$

At this point we can also calculate the auxiliary winding needed to supply the driver. In our case the driver used is the UC3842 that from its specification can be driven with 15V. By applying again formula1 we can calculate the primary-to-auxiliary turn ratio:

$$\frac{N_P}{N_{AUX}} = \frac{V_{fl}}{V_{Aux} + V_{F,diode}} = \frac{500}{15+1} = 31 \Rightarrow N_{Aux} = 5$$

Before carrying on with the wire dimension calculation, we can preliminary verify if the selected core is acceptable from a thermal point of view during its normal operation.

Through the Ampere's law we can calculate the B field in normal operation:

$$N_P I_p = \oint Hdl = \sum H_i l_i = H_g l_g + H_{fe} l_{fe} = \frac{B}{\mu_o} l_g + \frac{B}{\mu_{fe}} l_{fe} \quad (5.3)$$

Being μ_{fe} the magnetic permeability in the iron much higher than μ_o (the magnetic permeability in the air) we can neglect the last item in the formula (5.3)

$$N_P I_p = \frac{B}{\mu_o} l_g \quad \Rightarrow \quad B = 170mT$$

From the ferrite datasheet the power dissipation is 150mW/cm^3, knowing that the total volume of the core is about 5cm^3 the total power dissipation in the core is about P_{fe} = 750mW.

The thermal resistance of the selected core is 24 $^oC/W$, knowing that

$$P_{fe} = \frac{\Delta T}{R_{th}} \quad \Rightarrow \quad \Delta T = 18\,^oC$$

This value allows the designers to operate in safe condition since we have to add also the losses due to the winding with a further consequent increase in temperature.

The next step is the wire dimension calculation, from both primary and secondary side. First we must

assume the maximum losses on the copper. Normal practice is to choose a dissipation level comparable with the one achieved in the core, practically we can chose 1W.

From the Joule's law we can calculate the resistance of both primary and secondary winding.

$$R_P = \frac{P_{CU}}{2I_{PRMS}^2} \Rightarrow R_P = 3.46\Omega \qquad R_S = \frac{P_{CU}}{2I_{SRMS}^2} \Rightarrow R_S = 0.0174\Omega$$

From that, knowing the copper resistivity at 100 ^{o}C (ρ_{100} =2.303 10^{-6} Ω cm), and the average wind length L_t (L_t = 4.1cm), we can easily calculate the wire sections (in cm^2)

$$A_{PCU} = \frac{\rho_{100} N_p L_t}{R_p} = 4.08 \cdot 10^{-4} \quad \Rightarrow \quad d_p = 0.022 \quad [cm]$$

$$A_{SCU} = \frac{\rho_{100} N_s L_t}{R_s} = 4.30 \cdot 10^{-3} \quad \Rightarrow \quad d_s = 0.074 \quad [cm]$$

For practical consideration, to better optimize the transformer window utilization and in the main time in accordance with the above calculation, it has been chosen:

d_p = 0.025 [cm] d_S =0.05 [cm] (2 in parallel)

The choice at secondary side of 2 wires of 0.05 mm in parallel vs. one of 0.074 mm has been made to minimize the skin effect.

During the transformer construction particular care must be put in minimizing the parasitic impedances, in particular the leakage inductance and the winding capacitance. Practically the leakage inductance should not exceed 3% of the primary inductance. The use of interleaved winding is a common method to reduce leakage inductance. Practically half of the primary turns is firstly wound, then the secondary turns and finally the last half of the primary that must result series connected with the first half-wind of the primary. To avoid an excessive increase of the winding capacitance the second half of the primary must be connected with the switch.

The final transformer has been realized from TDK in accordance with the above specification, its relative part number is SRW2924ED-E02V015. The table below summarizes the most important parameters of the above-mentioned transformer:

Table 2: Transformer Parameters

Symbol	Description	Values	Dimension
A_e	Effective cross section Area	85.78	mm^2
l_e	Effective magnetic path	58.65	mm
V_e	Effective core volume	5030	mm^3
A_{CW}	Cross sectional winding area	115.45	mm^2
l_g	Air gap lenght	0.8	mm
A_L	Single turn inductance	130	nH/n^2

6. OUTPUT CIRCUIT

For the purpose of the present note the transformer has been designed with just one output power section (48W) and one auxiliary output section to supply the driver. As already mentioned in the fly-back operation, it is during turn-off that the energy stored in the primary is transferred to the secondary. In a first approach we can neglect the energy absorbed by the auxiliary output, so that almost all the peak secondary current, about 18A at maximum load, flows through the output capacitor, causing a voltage ripple due to the ESR of the capacitor itself. In order to fix the output voltage ripple lower than 1V, the ESR from the Ohm law must be lower than 0.055Ω.

Fixed a time constant of 100µsec so that ($ESR*C_o=100*10^{-6}$ s) the capacitor should be higher than 1818µF and taken also into account 20% margin, a C_o of 2200µF has been selected.

Next step is to determine the output diode. For discontinuous mode operation ultra fast or schottky diodes are recommended. The diode must be able to sustain the output voltage plus the maximum reflected voltage according to the formula below

$$V_{RRV} = V_{out}\left(1+\frac{V_{inmax}}{V_{fl}}\right) \quad (6.1)$$

Practical considerations impose to add a safety margin of about 20-25%. Good choice is to consider also diodes with current capability about twice higher then the DC output current I_{out}.

7. CLAMPING CIRCUIT

The clamping circuit has the important function to avoid that the overvoltage generated by the leakage inductance of the primary winding exceeds a pre-fixed value (V_{spike}).

A simple RCD clamping network has been chosen for its simplicity. A different choice, like LCD, thanks to its loss-less performance, could help in achieving a better efficiency that goes beyond the purpose of the present work. The dimensioning of this clamping circuit can be achieved by using the following formulas:

$$C_{min} = \frac{L_{LK} I_{peak}^2}{(V_{fl}+V_{spike})^2 - V_{fl}^2} \quad (7.1)$$

$$R_{min} = \frac{1}{f \cdot C_{min} \ln\left(1+\frac{V_{spike}}{V_{fl}}\right)} \quad (7.2)$$

Supposing that the leakage inductance is about 5% of the primary inductance, and I_{peak}, maximum current in stressful conditions, (like start-up or short circuit) is equal to 1.6A, we can achieve

C_{min} = 1nF and R_{min} = 60KΩ

Generally these minimum values could lead to excessive power dissipation in the clamping circuit, in fact the power losses generated in the clamping circuit are proportional to:

$$P_R \propto \frac{V_{fl}^2}{R_{clamp}}$$

It is better to choose R_{clamp} much higher than the minimum calculated, the clamping capacitor has to be

increased as well. From tests in the bench the relevant values chosen for the board are:

C_{clamp} = 6.8 nF R_{clamp} = 220KΩ

8. ESBT DRIVING CIRCUIT

As already mentioned in the chapter 2, a simple constant voltage is enough to supply the base of the ESBT, nevertheless it could not be sufficient to properly drive the device when very high voltage level and/or high switching frequencies are handled. First problem is related to the dynamic saturation phenomenon always present in all "bipolar devices" during turn-on operations. This phenomenon is related to the delay of the voltage drop between Collector and Emitter to reach the static value (V_{CESAT} in any bipolar datasheet). It is evident that the higher is the working frequency, the worse this effect will be. A common used method to moderate this effect consists in heavily injecting the base with minority carriers in the fastest possible way, practically by providing a very high current peak at turn-on. The consequent high base current acts in contrast with the need not to over saturate the device since this will badly impact the turn-off loss: as a result, in fact, the benefits got at the turn-on could become a weakness for the turn OFF performance. A particular modulation of the base current that allow the optimization of both switching phases can be achieved with the circuit in the figure below.

Figure 6: ESBT Driving Circuit and Relevant Waveforms

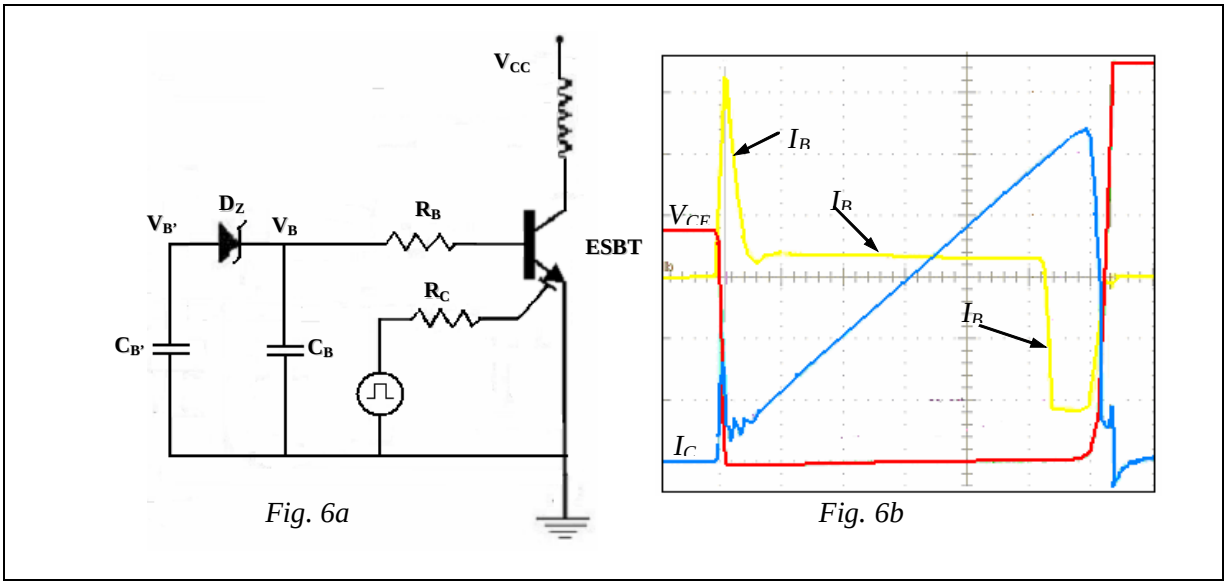


Fig. 6a *Fig. 6b*

With reference to fig. 6a $V_{B'}$ is kept constant thanks to the electrolytic capacitor $C_{B'}$, while V_B can be chosen according to the device characteristic and the peculiarity of the topology in use. By using a relatively low (non electrolytic) C_B value, V_B will be higher than $V_{B'}$ during the first part of the turn-on, accomplishing the current spike need. From this value, both the maximum current value and duration of the initial spike can be adjusted: the lower is the capacitor value, the shorter will be the spike duration and the higher will be the voltage V_B limited only by the zener voltage.

A small R_B is enough to control the base current both at Turn ON and Conduction.

The zener diode allows a tight base current control, by setting the exact difference between V_B and $V_{B'}$, finally linked with the base current spike. The relevant waveforms in fly-back operation are those reported in figure 6b. The proposed circuit allow us to achieve an optimization of base current behavior in

the first zone described in figure 6b without jeopardizing the turn-off behavior: the big pulse of base current during the first instants of turn-on (achieved thanks to the proper choice of the capacitor C_B) strongly acts in reducing the effect of dynamic saturation, while the capacitor $C_{B'}$ plus the resistor R_B supply the correct level of base current during all the on state. It is evident that the real advantage of the proposed circuit is the possibility to set $V_{B'}$ (affecting the all ON stage) independently from the voltage needed (V_B) to get the desired current spike.

It is worth noticing that the proposed circuit provides also an energy recovery function, which minimizes the power needed to supply the base. The smaller capacitor stores all charges coming from the base during the storage time, and gives them back to the base during the next turn-on.

In a practical driving circuit V_B can be set in order to obtain $I_{B1} = -I_{B3}$ (see figure 6b), while $V_{B'}$ must provide the right saturation level for the most stressful working condition (that is the highest IC). This condition is characterized by the flat zone where the base current $I_B = I_{B2}$, shown in figure 6b, is practically constant and fixed according to the gain of the transistor used at maximum current. This sort of "fixed voltage driven" method may cause some problems at low load conditions and in general all the times the device works at low current level, in fact in this case the storage time will be longer (over saturation effect), with consequent worse turn-off performance.

It is clear that a proportional base biasing could positively impact the device performance at lower current too. In the driving circuit reported in fig.7 a current transformer associated with the base of the ESBT implements a proportional base biasing and provides two further advantages: firstly designer does not need to get a constant voltage anymore, secondly, the current transformer provides an IB current with the same shape as the collector current.

Figure 7: ESBT Proportional Driving Circuit and Relevant Waveforms

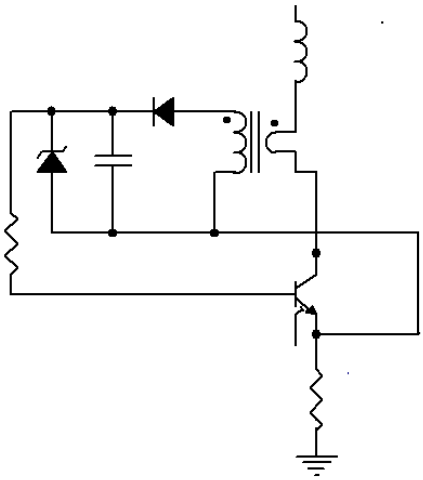


Fig. 7a

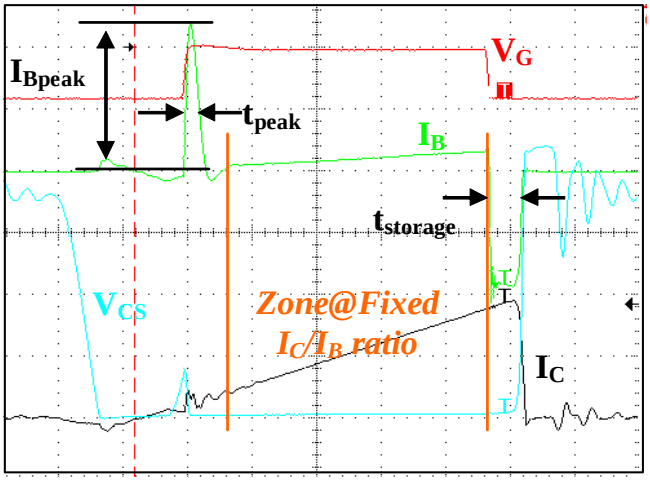


Fig. 7b

As visible from figure 7 the driving network must guarantee a zone with fixed IC/IB. This is imposed by the transformer turn ratio. From the characteristic of the chosen transistor (STC03DE170), it is recommended a turn ratio equals to 5 in order to ensure the right saturation level of the transistor that

exhibits H_{FE} equal to 5 at I_C=1.8A, V_{CE} = 1V, so that in our current transformer we fix as first approach:

$$\frac{N_P}{N_S} = \frac{1}{5}$$

9. CURRENT TRANSFORMER CORE SELECTION

The main challenge now is to choose the core material, its shape and dimension. A correct design of this current transformer has to take into consideration some constraints that, being in contrast each other, lead to a few iterative design steps. The needs to have magnetic permeability as high as possible to minimize the effect of magnetization inductance, is in contrast with the need of a negligible inductance with respect to that of primary transformer. In fact, being the primary winding of the fly-back transformer in series with the primary winding of the current transformer, the relevant inductance would be seen as an increase of the leakage inductance in the converter. Moreover a higher magnetic permeability implies a bigger core size (to avoid the core saturation) while the dimension of the current transformer has to be as small as possible for both space and cost reasons.
Among all possible choices a ferrite ring with 12.5 mm diameter has been selected. Starting from the preliminarily fixed turn ratio (N=0.2), we must determine the minimum primary turns needed to avoid the core saturation. With reference to figure 7b, by applying the Faraday's law and imposing the maximum flux Bmax equals to Bsat/2, we have:

$$V_1 = N_{TP}\frac{d\varphi}{dt} \cong N_{TP} \cdot A_e \cdot \frac{\Delta B}{\Delta t} \quad \Rightarrow \quad N_{TP} = 2\frac{V_1 \cdot T_{on\max}}{A_e \cdot B_{sat}}$$

Where B_{sat} is the saturation flux of the core. Both primary turn number and primary inductance for some common toroidal core have been calculated and summarized in the table below.

Table 3: Primary Turn Number and Primary Inductance for Some Common Toroidal Core

Material	A_l value [nH]	Bsat @ 25 °C [mT]	Bsat @ 100 °C [mT]	N_P	L_{TP} [H]
N67	1070	480	370	1.85 2	4.28
N30	2200	350	225	2.53 3	19.8
T38	5100	350	220	2.53 3	49.5

For the consideration previously made, the relatively high primary inductance of T38 does not make its selection as a suitable choice, furthermore between N67 and N30, this last one, giving the best trade off, has been selected. To deeply explain this choice, we must observe that the magnetization inductance cannot be neglected and it also strongly contribute in determining the real transformer transfer rate. This can be explained looking at the figure below where the proportional driving schematic and its equivalent circuit is reported.

Figure 8: ESBT Current Transformer Driver and Equivalent Circuit

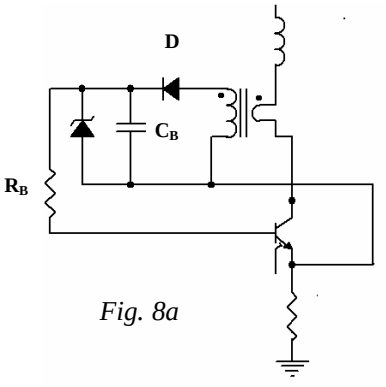


Fig. 8a

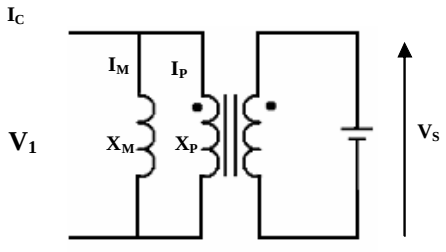


Fig. 8b

In figure 8b the driving circuit as been modeled with the equivalent schematic diagram of the transformer with its secondary closed with a voltage generator. In fact, looking at figure 8a we must note that during on time, the base of ESBT can be seen as a forward biased diode, to this we have to add the voltage drop on both diode D and resistor RB in series with the base of the ESBT to complete the secondary side load model. With these premises in a first order of analysis, the secondary side can be simply modeled as a voltage source given by:

$$V_S = V_{BEon} + V_D + V_{RB} \cong 2.5V$$

At primary side both primary inductance and magnetization inductance have been reported. Considering that only the IP fraction of the total collector current will be transferred to the secondary, the magnetization current has to be firstly as low as possible, secondly, its value must been taken into account for the proper calculation of transformer turn ratio. The magnetization voltage drop (that is the voltage at the primary of the current transformer) can be now easily calculate:

$$V_1 = V_S \frac{N_{1T}}{N_{2T}} = 2.5 \cdot \frac{1}{5} = 0.5 \quad [V]$$

The magnetization current for the two cores under analysis will be:

For N30: $$I_{Mmax} = \frac{V_1 T_{ONmax}}{L_{TP}} = \frac{0.5 \cdot 10.66}{19.8} = 0.27$$

For N67: $$I_{Mmax} = \frac{V_1 T_{ONmax}}{L_{TP}} = \frac{0.5 \cdot 10.66}{4.28} = 1.24$$

Being the I_{Pmax}=0.9A in steady state, the N67 core with 2 turns at primary side must obviously be excluded, unless increasing the number of turns, but this would lead to fill all the available window area and consequently to the necessity of choosing a bigger core size.

Once fixed both core material and size, the turn ratio must be adjusted to get the desiderated I_C/I_B ratio according to the below equation:

$$N_{eff} = \frac{I_P}{I_B} = \frac{I_{Cmax} - I_{Mmax}}{I_C/5} = \frac{0.9 - 0.27}{0.18} = 3.5$$

Where I_{Mmax} is the magnetization current related to $I_{Cmax} = I_P$

From a bench verification it is convenient to choose $\frac{N_{2T}}{N_{1T}} = 4$, and than $N_{1T} = 3 \quad N_{2T} = 12$.

Considering the short length of wires at both primary and secondary side, the exact calculation of their section is not of primary importance, while considerations about their insulation are, since the voltage at primary side during turn-on can overstep 1500V.

For the demo board, wires with the following section have been used:

d_P=0.5mm (Primary winding) and d_S=0.25mm (Secondary winding).

At primary side it is suggested to use an insulated wire capable to sustain 3500V.

Once defined the current transformer we still need to determine the zener diode, the capacitor C and the resistor R_B. As already mentioned in chapter 8, the turn-on performance of the ESBT is related to the initial base peak current and its duration t_{peak} that can be given by:

$$t_{peak} = 3R_b C_b$$

A good choice for R_b is 0.56Ω. This value allows us to eliminate the ringing on the base current after the peak, and at the same time, it generates negligible power dissipation.

Being the minimum ON time 1.4µs, tpeak should be less than 0.7µs. In this particular case it has been fixed at 400ns. Hence C_b= 238nF (the nearest 220nF has been used).

I_{peak} must be limited in order to avoid an extra saturation of the device. This action is made by the zener diode DZ that clamps the voltage across the small capacitor C_b. The zener is designed according to the following formula:

$$V_Z = 2(I_{peak} R_b + 1) R_b C_b = 3.12V \quad \Rightarrow \quad 3.3V$$

For the diode D in figure 8a the BA159 has been selected.

10. PWM DRIVER

As already mentioned, we still need to correctly drive the gate of ESBT. A simple PWM driver can both drive the gate of ESBT and supervise the fly-back operations requested by the converter. The common UC3842 provides a cost effective current mode control.

As already mentioned in chapter 5, the UC3845 needs 15V for its correct biasing and this voltage reference is supplied by the auxiliary output of the transformer. Neglecting for the moment the start-up circuit, next step is to correctly design the network for the PWM driver terminals.

Calculation and considerations made on the following steps are related to the complete schematic diagram of the realized demo board reported in figure 9.

1. Primary side regulation.

It can be achieved in a simple way just fixing a voltage divider. The advantages of primary side regulation are essentially linked to its simplicity and low cost, by the way it cannot supply an accurate control on output voltage at load variation. It is generally chosen for low power SMPS. The voltage reference of the internal error amplifier is set in the UC3842 at 2.5V, consequently the values chosen for the network resistors are:

R_{12}=22kΩ R_{13}=3.9kΩ

2. Control loop compensation.

Being the solution adopted a current mode control in discontinuous mode, a simple loop with just one pole can be used for its simplicity. For this loop we have:

R_{10}=150kΩ C_5=100pF

3. Switching frequency and max duty cycle setting.

Since the target of our project is to have f=50kHz and δ_{MAX}=75%, from the datasheet of the UC3842 we can set:

R_{15}=2.2kΩ C_6=15nF

4. Current sensing and limiting.

Since the inverting input to the UC3842 current-sense comparator is internally clamped at 1V, we must ensure that the voltage drop on the sense resistor (R_{18}) does not exceed this value for the normal operation. Since I_{peak} = 0.9A, we can choose with a margin of about 30% an I_{max} =1.2A; consequently from Ohm's law:

R_{18}=0.82Ω

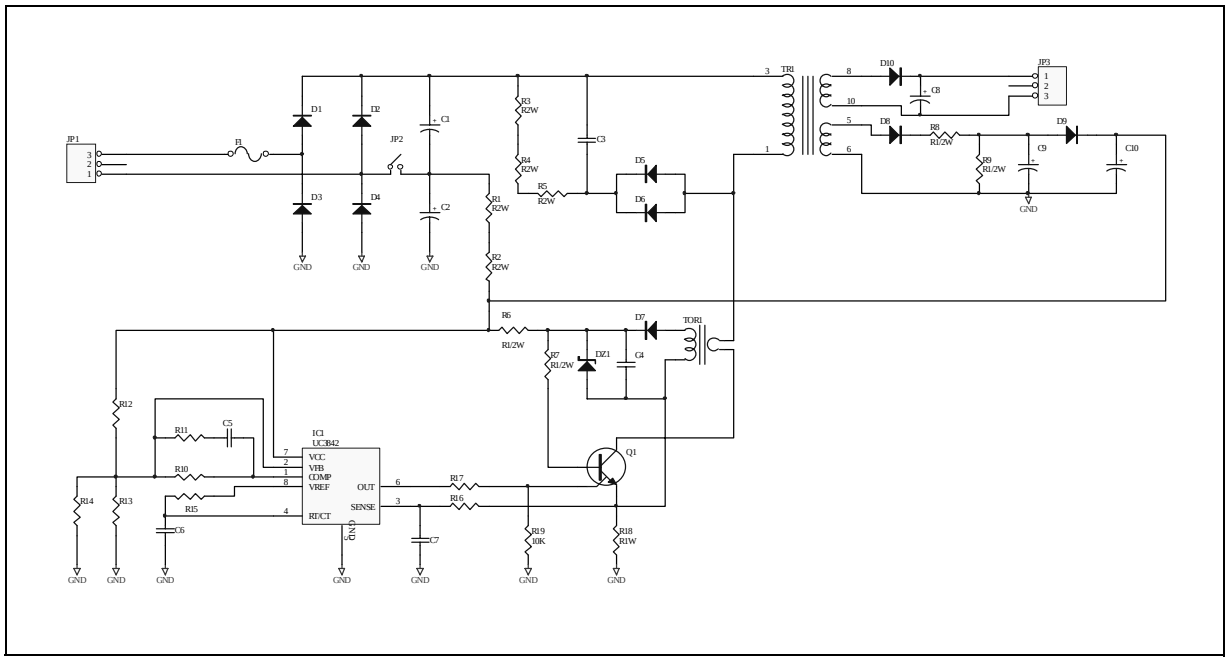
When sensing current in series with the power transistor, the current waveform will have a large spike at turn on due to the intrinsic capacitance. As shown in figure 9, a simple RC filter is adequate to suppress this spike. Typical values are:

R_{16}=1kΩ C_7=470pF

5. ESBT gate drive.

Series resistor R_{17} provides damping for a parasitic tank circuit. Resistor R_{19} shunts output leakage currents to ground when the under-voltage lockout is active.

Figure 9: Fly-back Schematic Diagram



11. START-UP NETWORK

To let the circuit start as soon as the line voltage is applied it is necessary to pre-charge both C_{10} and C_4 base capacitances. A resistor connected to the mid point of the input filter capacitor divider directly makes the pre-charge. Of course an active start-up circuit, avoiding dissipation during steady-state behavior, can improve the overall efficiency of the converter at expenses of increased circuit complexity and cost.

The power supply must start at V_{dcmin}=250V. The total current required by all components connected to Vcc at start-up determines (R_1+R_2) value. The UC3842 has a start-up threshold of 16V, therefore the total turn-on current is:

$$I_{tot} = I_{UC3842-start-up} + I_{R12+R13} + I_{R6} = 0.5mA + \frac{16V}{25.9k\Omega} + \frac{16V}{56k\Omega} = 1.4mA$$

$$(R_1 + R_2)_{min} = \frac{V_{dcmin}}{2 \cdot I_{TOT}} = 78k\Omega$$

R_6 has been supposed equal to 56kΩ , whose value is enough to pre-charge the base capacitor C_4, anyway it is important to check a posteriori that the time constant established by R_6 and C_4 is negligible with respect to that imposed by (R_1+R_2) and C_{10}.

C_4 must be able to supply UC3842 till the steady-state behavior of the converter is established. This time, from bench verification is 15ms maximum. Being under-voltage threshold of UC3842 8.5V, the voltage across C_4 must always be over 8.5V during the start-up period. Therefore:

$$C_{10min} = \frac{\left(I_{UC3842-quiescent} + I_{R12+R13} + I_{R6}\right) \cdot t_{start-up}}{16 - 8.5} \cong \frac{18mA \cdot 15ms}{7.5} = 36\mu F$$

The next closed commercial value for C_{10} = 47µF has been chosen.

Therefore:

$$R_6 \cdot C_4 << (R_1 + R_2)_{min} \cdot C_{10} \quad \Rightarrow \quad 12.3ms << 3.6s$$

This completely verifies our assumption.

12. EXPERIMENTAL RESULTS

Theoretical assumptions made so far have been validated with the realization of a demo board, whose schematic has been reported in figure 9. A complete characterization of this board has been carried out and the most meaningful waveforms at full load condition are below reported.

Figure 10: Steady State

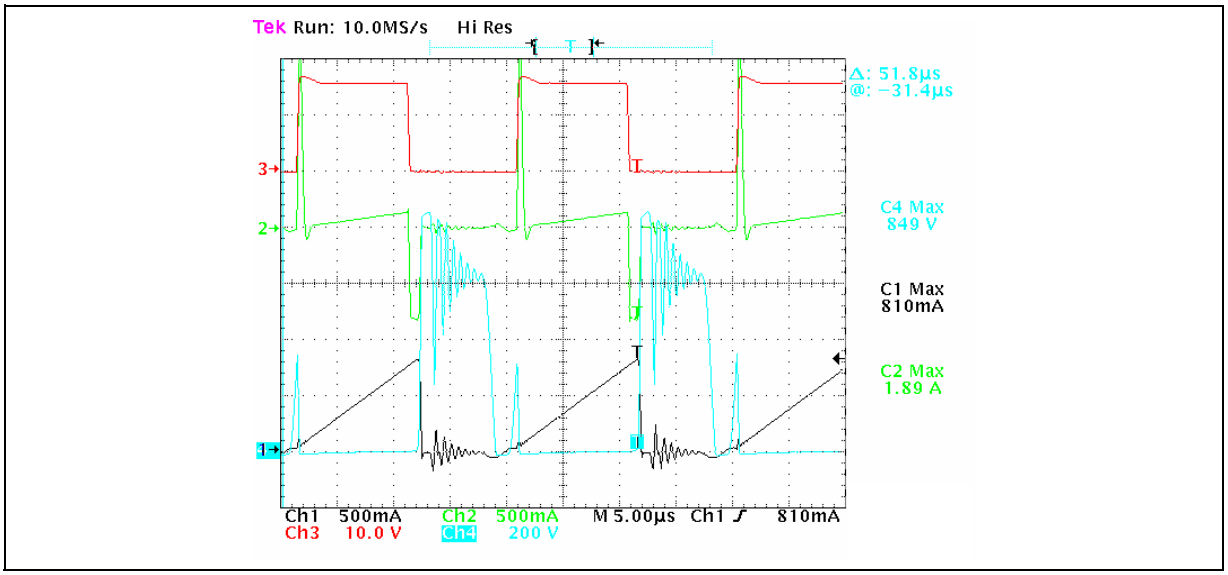


Figure 11: Turn-on Behavior

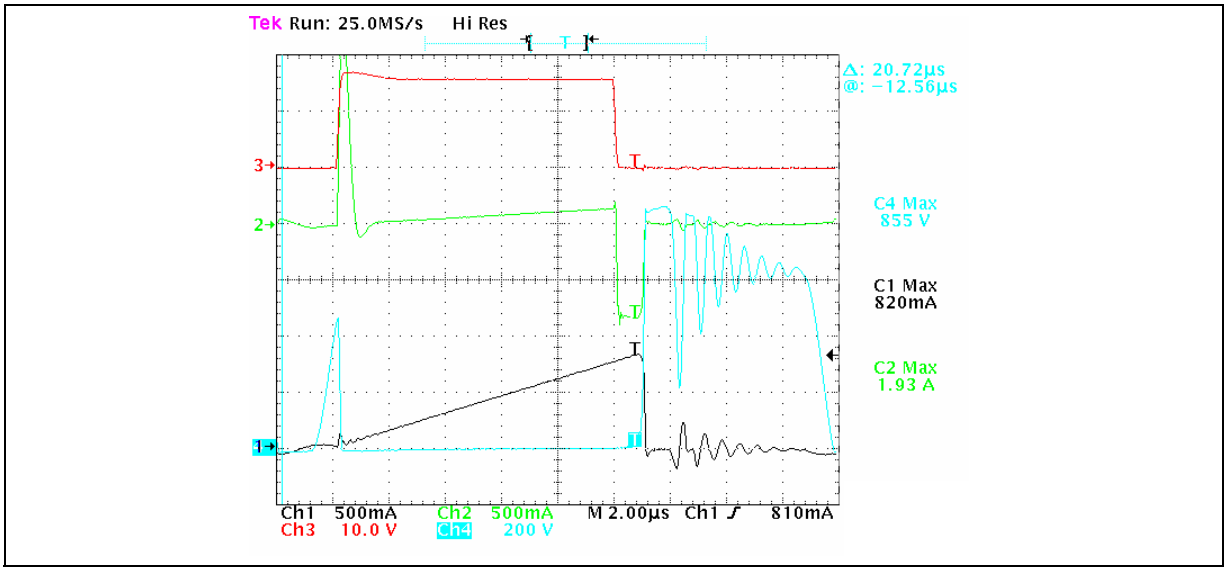


Figure 12: Turn-off Behavior

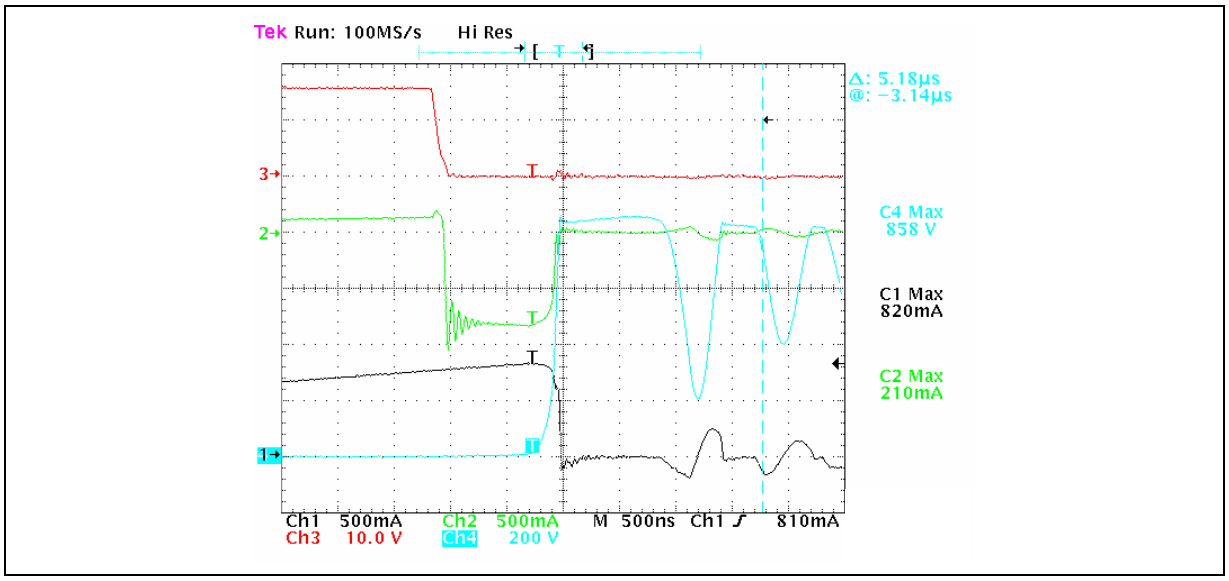
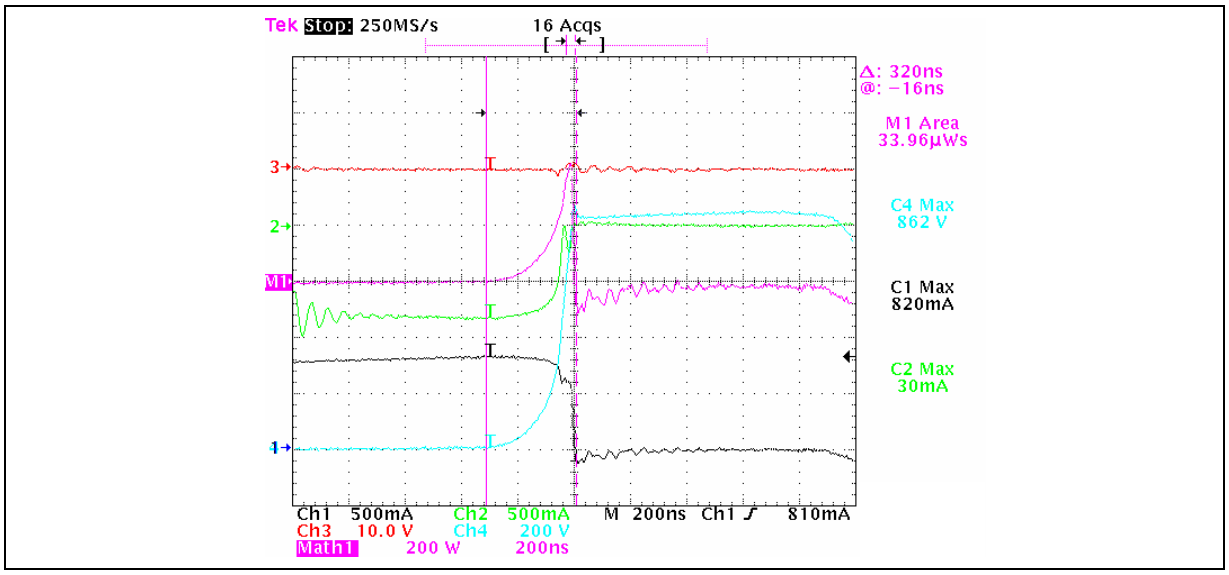


Figure 13: Turn-off Losses



Waveforms in figures 10, 11, 12 describe the function of the converter at maximum load with minimum rectified input voltage (V_{IN} = 250V), with zoomed view at turn-on and turn-off operation. Figure 13 gives also the losses at turn-off.

The following figures reproduce the same waveforms at maximum input voltage (V_{IN} = 750V).

Figure 14: Steady State

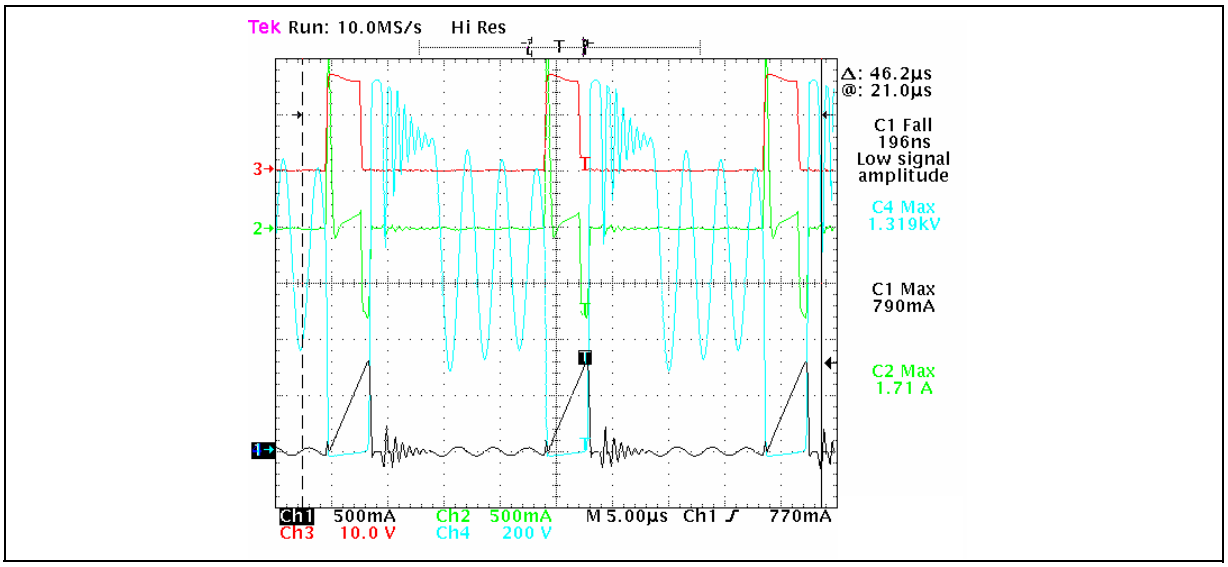


Figure 15: Turn-on Behavior

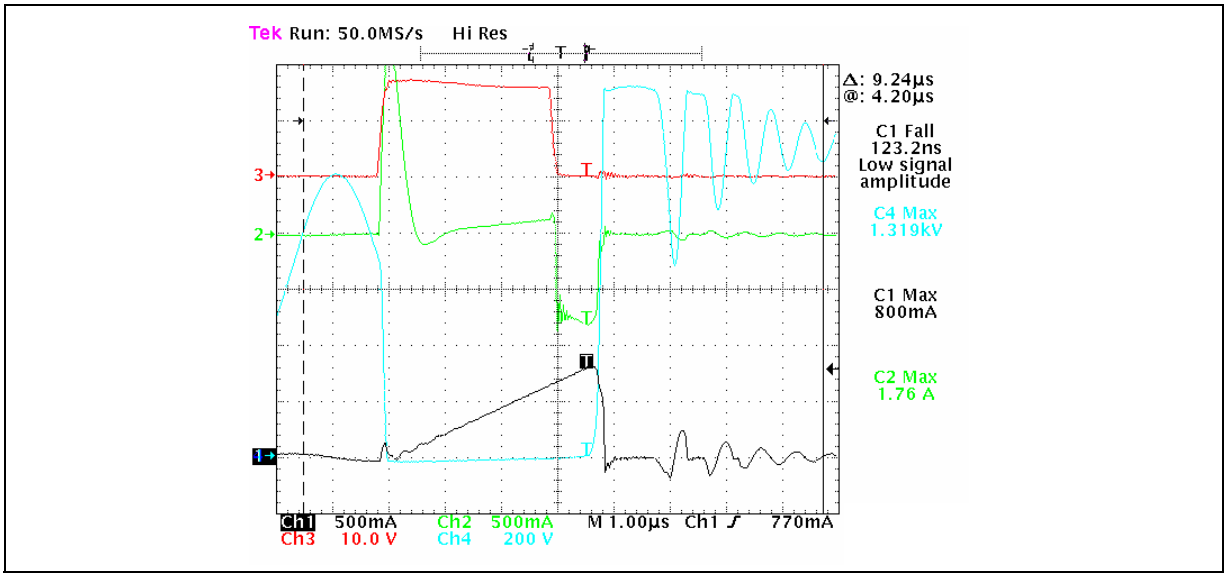


Figure 16: Turn-off Behavior

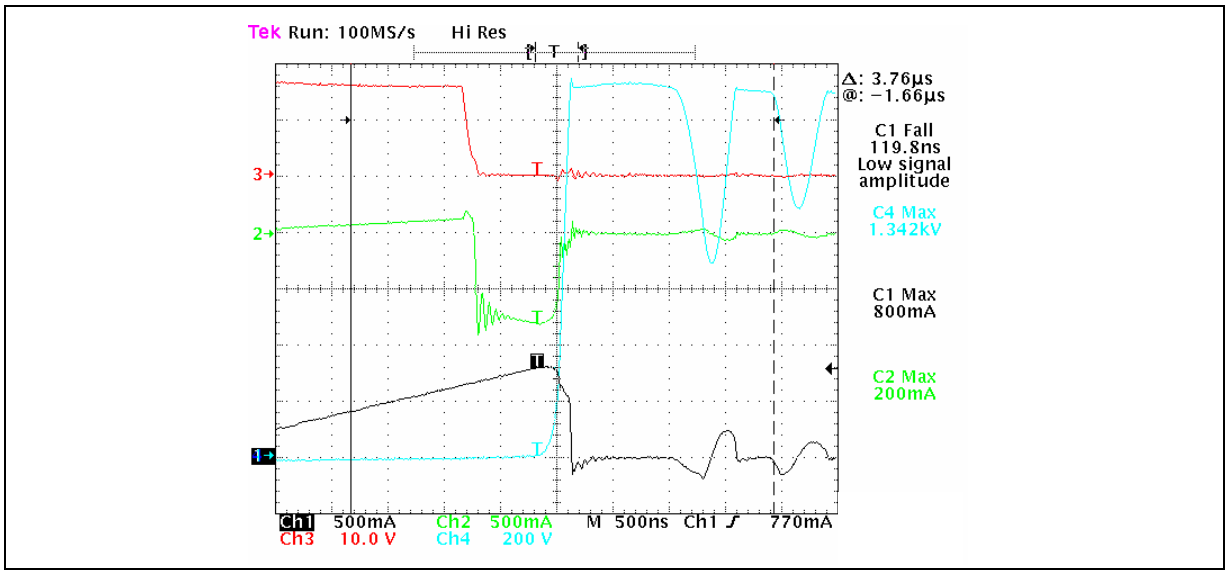
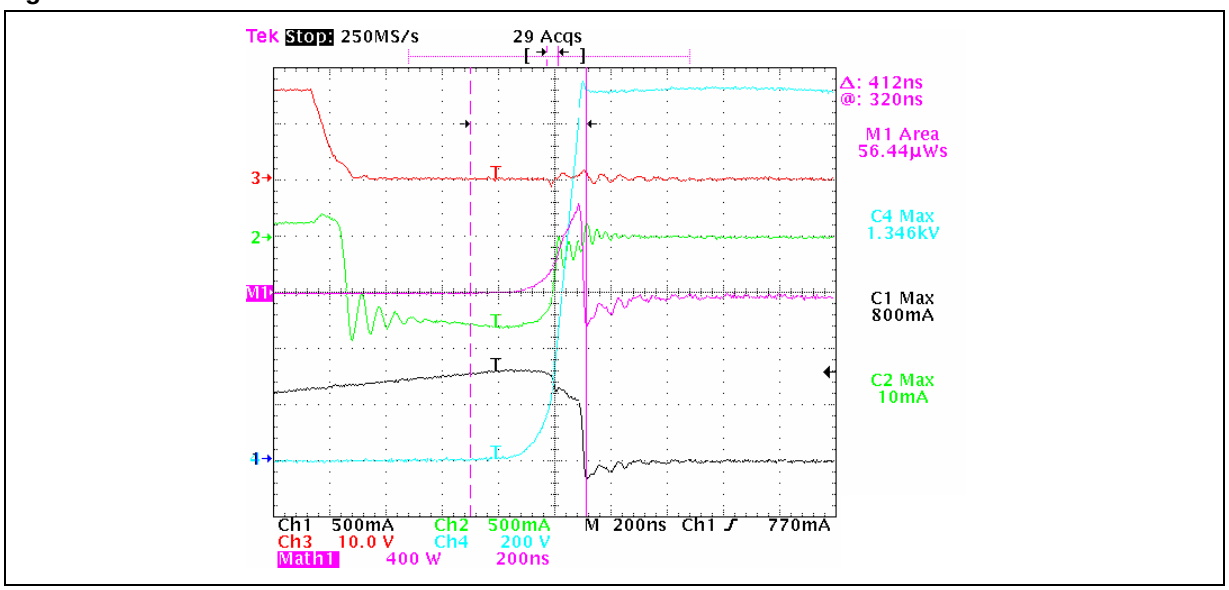


Figure 17: Turn-off Losses



In the following figures while reporting again the steady state waveforms at both minimum and maximum input voltages, the voltage drop on the secondary side of the current transformer has been added (curves labeled 3 in the waveforms reported in figures 18 and 19)

Figure 18: Steady State at Minimum Voltage

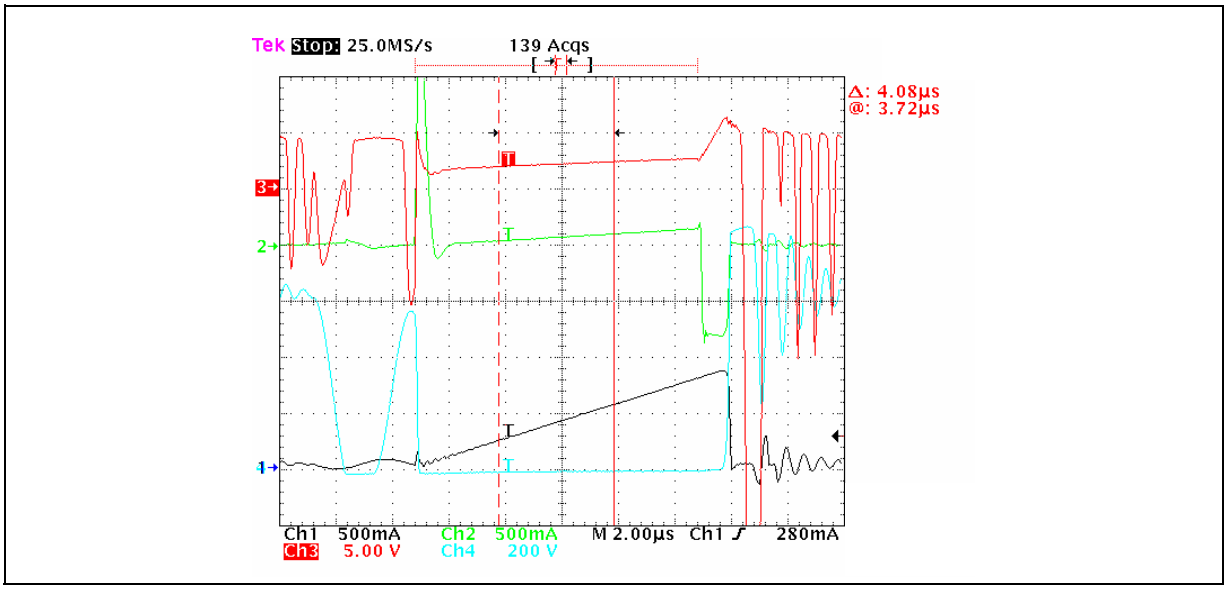
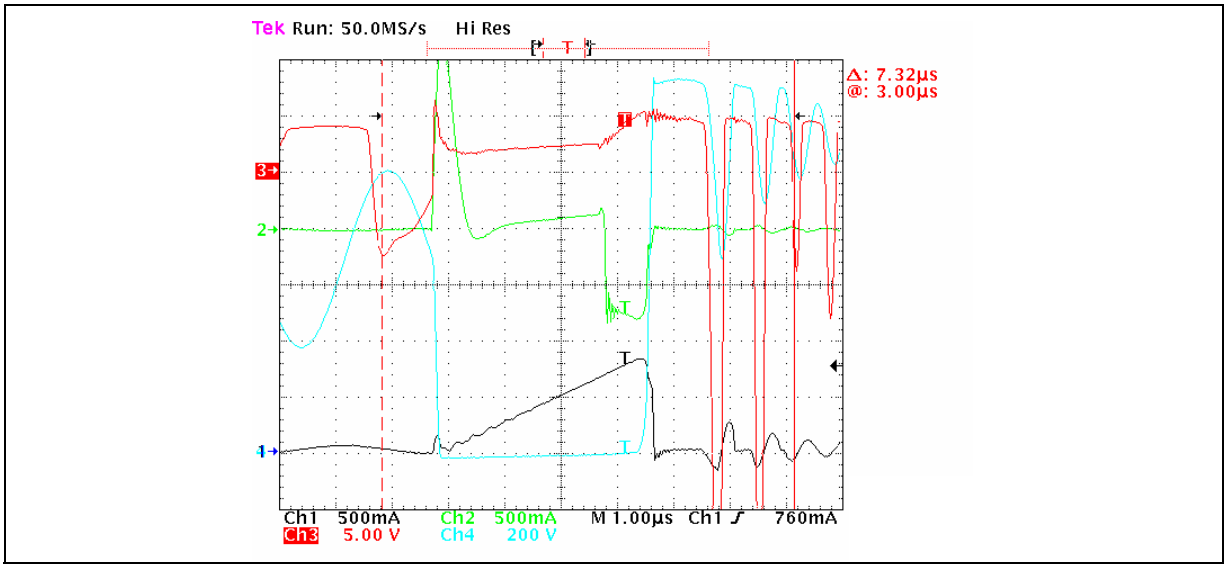


Figure 19: Steady State at Maximum Voltage



As clearly visible in the above figures, this voltage during on state is fixed at 2.5V (confirming theoretical calculation) and the core will be completely demagnetized after turn-off.

13. PCB LAYOUT AND LIST OF MATERIALS

The printed circuit board is reported in figure 20, while the relevant bill of material is listed in table 4.

Figure 20: PCB Layout

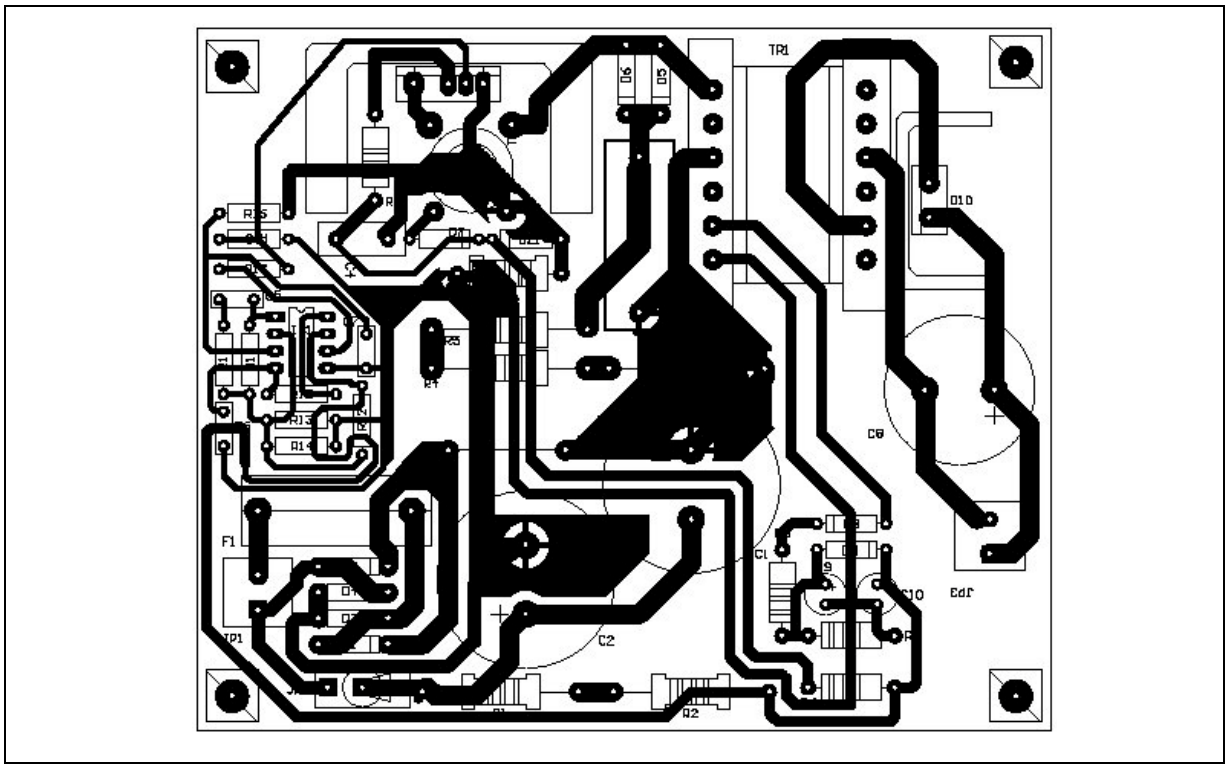


Table 4: Bill of Materials

R1	39k -2W
R2	33k -2W
R3	56k -2W
R4	56k -2W
R5	56k -2W
R6	56k -0.5W
R7	0.56 -0.5W
R8	0
R9	1k 0.5W
R10	150k
R11	0
R12	22k -0.25W 1%
R13	3.9k -0.25W 1%
R14	
R15	2.2k -0.25W
R16	1k -0.25W
R17	22 -0.25W
R18	0.82 -1W
R19	10k -0.25W
C1	220 F-400V
C2	220 F-400V
C3	6.8nF-2000V
C4	220nF-100V
C5	100pF
C6	15nF
C7	470pF
C8	2200 F-50V
C9	47 F-25V
C10	47 F-25V
D1	1N4007
D2	1N4007
D3	1N4007
D4	1N4007
D5	BY259
D6	BY259
D7	BA159
D8	1N4148
D9	1N4148
D10	STBYW81P200
DZ1	3.3V-0.8W
TR1	TDK SRW2924ED-E02V015
IC1	UC3842A