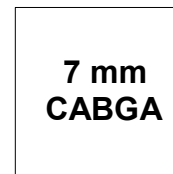
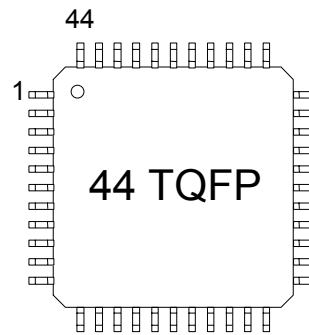


## FEATURES

- Complete E1, T1, or J1 line interface unit (LIU)
- Supports both long-haul and short-haul trunks
- Internal software-selectable receive-side termination for 75Ω/100Ω/120Ω
- 3.3V power supply
- 32-bit or 128-bit crystal-less jitter attenuator requires only a 2.048MHz master clock for both E1 and T1 with option to use 1.544MHz for T1
- Generates the appropriate line build-outs, with and without return loss, for E1 and DSX-1 and CSU line build-outs for T1
- AMI, HDB3, and B8ZS, encoding/decoding
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output synthesized to recovered clock
- Programmable monitor mode for receiver
- Loopbacks and PRBS pattern generation/detection with output for received errors
- Generates/detects in-band loop codes, 1 to 16 bits including CSU loop codes
- 8-bit parallel or serial interface with optional hardware mode
- Muxed and nonmuxed parallel bus supports Intel or Motorola
- Detects/generates blue (AIS) alarms
- NRZ/bipolar interface for TX/RX data I/O
- Transmit open-circuit detection
- Receive Carrier Loss (RCL) indication (G.775)
- High-Z State for TTIP and TRING
- 50mA (rms) current limiter

## PIN DESCRIPTION



## ORDERING INFORMATION

|           |             |                  |
|-----------|-------------|------------------|
| DS21348TN | 44-Pin TQFP | (-40°C to +85°C) |
| DS21348T  | 44-Pin TQFP | (0° C to +70°C)  |
| DS21348GN | 7mm CABGA   | (-40°C to +85°C) |
| DS21348G  | 7mm CABGA   | (0° C to +70°C)  |
| DS21Q348N | (Quad) BGA  | (-40°C to +85°C) |
| DS21Q348  | (Quad) BGA  | (0° C to +70° C) |

## DESCRIPTION

The DS21348 is a complete selectable E1 or T1 LIU for short-haul and long-haul applications. Throughout the data sheet, J1 is represented wherever T1 exists. Receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0dB to 12 dB or 0dB to 43dB for E1 applications and 0dB to 30dB or 0dB to 36dB for T1 applications. The device can generate the necessary G.703 E1 waveshapes in 75Ω or 120Ω applications and DSX-1 line build outs or CSU line build outs of 0dB, -7.5dB, -15dB, and -22.5dB for T1 applications. The crystal-less onboard jitter attenuator requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications). The jitter attenuator FIFO is selectable to either 32 bits or 128 bits in depth and can be placed in either the transmit or receive data paths. An X 2.048MHz output clock synthesized to RCLK is available for use as a backplane system clock (where n = 1, 2, 4, or 8). The DS21348 has diagnostic capabilities such as loopbacks and PRBS pattern generation/detection. 16-bit loop-up and loop-down codes can be generated and detected. The device can be controlled via an 8-bit parallel muxed or nonmuxed port, serial port, or used in hardware mode. The device fully meets all of the latest E1 and T1 specifications including ANSI T1.403-1999, ANSI T1.408, AT&T TR 62411, ITU G.703, G.704, G.706, G.736, G.775, G.823, I.431, O.151, O.161, ETSI ETS 300 166, JTG.703, JTI.431, JJ-20.1, TBR12, TBR13, and CTR4.

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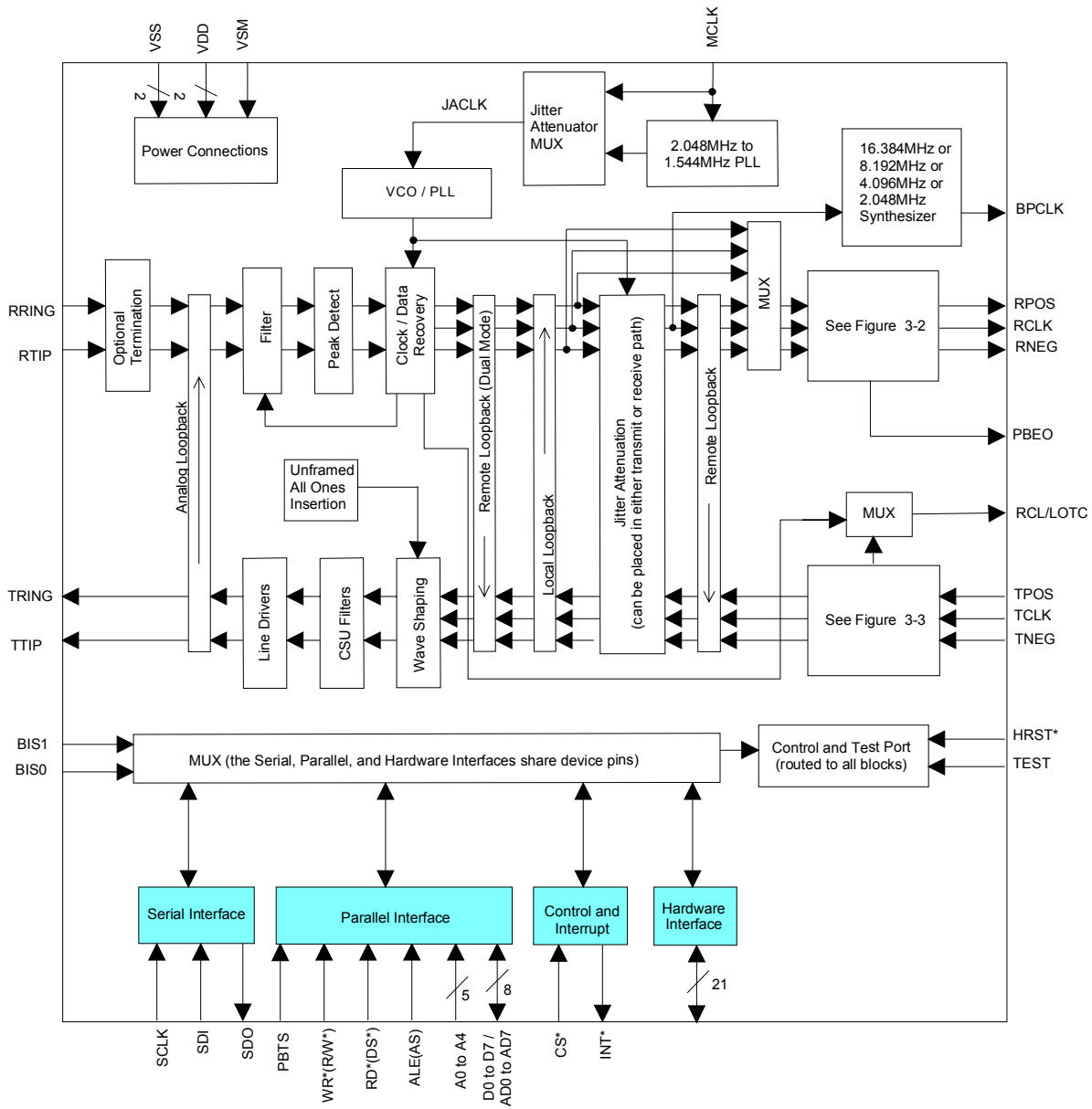
### 3. INTRODUCTION

The analog AMI/HDB3 waveform off of the E1 line or the AMI/B8ZS waveform off of the T1 line is transformer coupled into the RTIP and RRING pins of the DS21348. The user has the option to use internal termination, software selectable for 75Ω/100Ω/120Ω applications, or external termination. The device recovers clock and data from the analog signal and passes it through the jitter attenuation MUX outputting the received line clock at RCLK and bipolar or NRZ data at RPOS and RNEG. The DS21348 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The receive circuitry is also configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOS and TNEG is sent via the jitter attenuation mux to the waveshaping circuitry and line driver. The DS21348 will drive the E1 or T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long haul (CSU) or short haul (DSX-1) lines for T1.

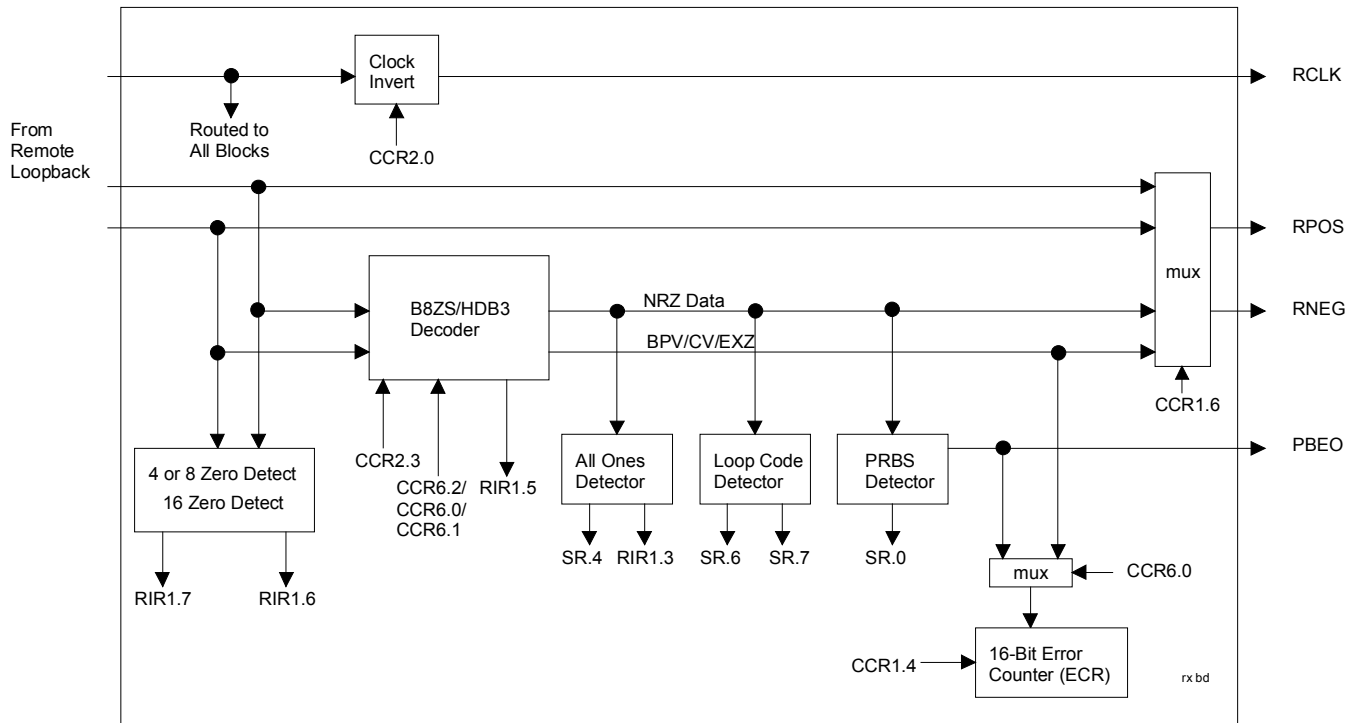
#### 3.1 DOCUMENT REVISION HISTORY

- 1) Datasheet for 3.3V only, 011801.
- 2) Added supply current measurements; added thermal characteristics of quad package, 092101.

# DS21348 BLOCK DIAGRAM Figure 3-1

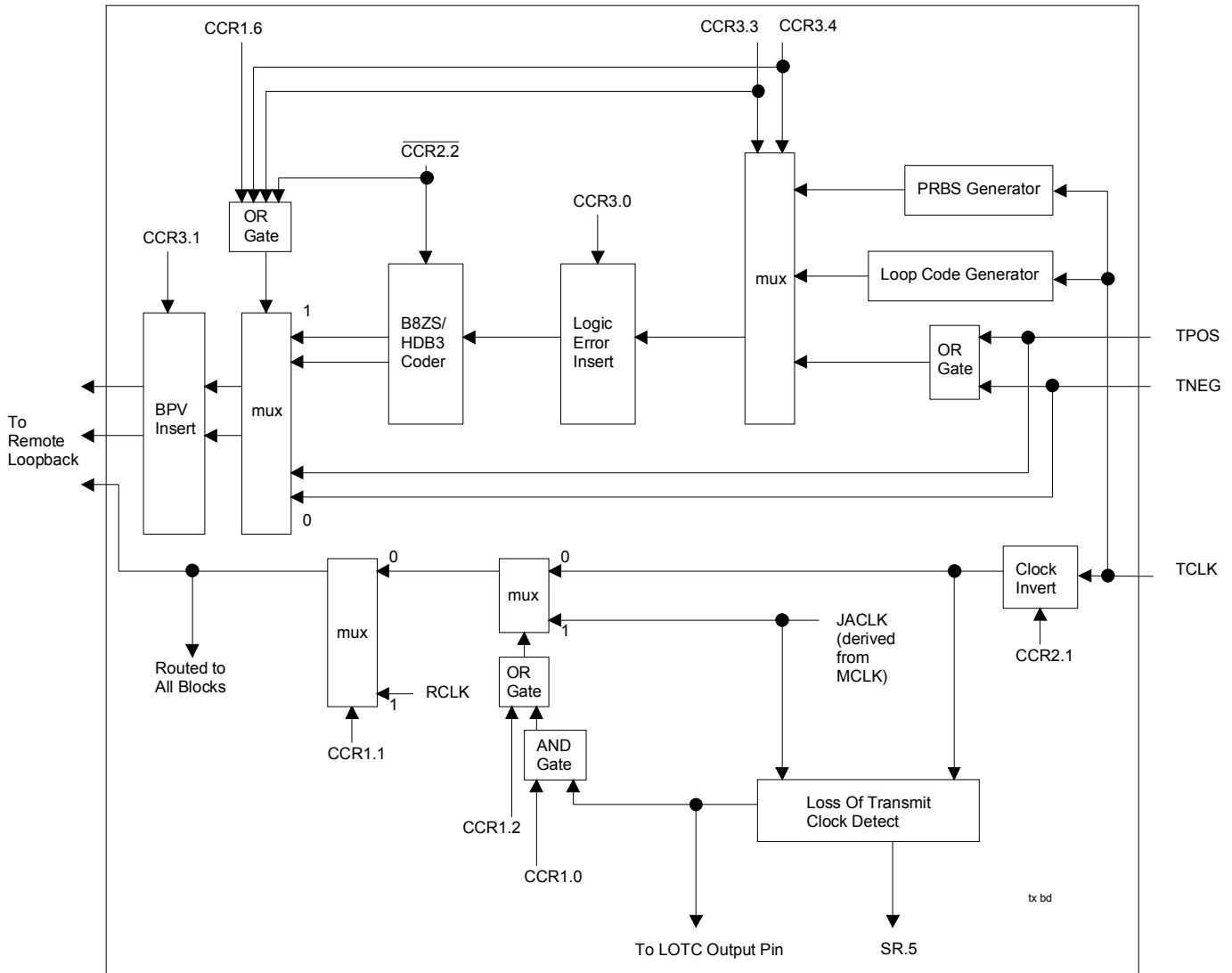


RECEIVE LOGIC Figure 3-2





**TRANSMIT LOGIC** Figure 3-3



**4. PIN DESCRIPTION**

The DS21348 can be controlled in a parallel port mode, a serial port mode, or a hardware mode (Table 4-1, 4-2, and 4-3). The parallel and serial port modes are described in Section 3, and the Hardware Mode is described below.

**BUS INTERFACE SELECTION** Table 4-1

| BIS1 | BIS0 | PBTS | MODE              |
|------|------|------|-------------------|
| 0    | 0    | 0    | Muxed Intel       |
| 0    | 0    | 1    | Muxed Motorola    |
| 0    | 1    | 0    | Nonmuxed Intel    |
| 0    | 1    | 1    | Nonmuxed Motorola |
| 1    | 0    | -    | Serial Port       |
| 1    | 1    | -    | Hardware          |

**PIN ASSIGNMENT IN PARALLEL PORT MODE** Table 4-2a

| DS21348T<br>PIN # | DS21348G<br>PIN# | I/O | Parallel<br>Port Mode |
|-------------------|------------------|-----|-----------------------|
| 1                 | C3               | I   | CS*                   |
| 2                 | C2               | I   | RD*(DS*)              |
| 3                 | B1               | I   | WR*(R/W*)             |
| 4                 | D2               | I   | ALE(AS)               |
| 5                 | C1               | I   | NA                    |
| 6                 | D3               | I   | NA                    |
| 7                 | D1               | I/O | A4                    |
| 8                 | E1               | I   | A3                    |
| 9                 | F2               | I   | A2                    |
| 10                | F1               | I   | A1                    |
| 11                | G1               | I   | A0                    |
| 12                | E3               | I/O | D7/AD7                |
| 13                | F3               | I/O | D6/AD6                |
| 14                | G2               | I/O | D5/AD5                |
| 15                | F4               | I/O | D4/AD4                |
| 16                | G3               | I/O | D3/AD3                |
| 17                | E4               | I/O | D2/AD2                |
| 18                | G4               | I/O | D1/AD1                |
| 19                | F5               | I/O | D0/AD0                |
| 20                | G5               | I   | VSM                   |
| 21                | F6               | -   | V <sub>DD</sub>       |
| 22                | G6               | -   | V <sub>SS</sub>       |
| 23                | E5               | I/O | INT*                  |
| 24                | E6               | O   | PBEO                  |
| 25                | F7               | O   | RCL/LOTCL             |
| 26                | D6               | I   | TEST                  |
| 27                | D5               | I   | RTIP                  |
| 28                | D7               | I   | RRING                 |
| 29                | C6               | I   | HRST*                 |
| 30                | C7               | I   | MCLK                  |
| 31                | B6               | O   | BPCLK                 |
| 32                | B7               | I   | BIS0                  |
| 33                | A7               | I   | BIS1                  |
| 34                | C5               | O   | TTIP                  |
| 35                | B5               | -   | V <sub>SS</sub>       |
| 36                | A6               | -   | V <sub>DD</sub>       |
| 37                | B4               | O   | TRING                 |
| 38                | C4               | O   | RPOS                  |
| 39                | A4               | O   | RNEG                  |
| 40                | B3               | O   | RCLK                  |
| 41                | A3               | I   | TPOS                  |
| 42                | B2               | I   | TNEG                  |
| 43                | A2               | I   | TCLK                  |
| 44                | A1               | I   | PBTS                  |

**PIN DESCRIPTIONS IN PARALLEL PORT MODE** (Sorted by Pin Name,  
DS21348T Pin Numbering) Table 4-2b

| ACRONYM                    | PIN            | I/O | DESCRIPTION   |
|----------------------------|----------------|-----|---|
| A0 to A4                   | 11<br>to<br>7  | I   | <b>Address Bus.</b> In nonmultiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the address bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), these pins are not used and should be tied low.   |
| ALE(AS)                    | 4              | I   | <b>Address Latch Enable (Address Strobe).</b> When using the parallel port (BIS1 = 0) in multiplexed bus mode (BIS0 = 0), serves to demultiplex the bus on a positive-going edge. In nonmultiplexed bus mode (BIS0 = 1), should be tied low.  |
| BIS0/BIS1                  | 32/33          | I   | <b>Bus Interface Select Bits 0 &amp; 1.</b> Used to select bus interface option. See Table 4-1 for details.   |
| BPCLK                      | 31             | O   | <b>Back Plane Clock.</b> A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384MHz output.   |
| CS*                        | 1              | I   | <b>Chip Select.</b> Must be low to read or write to the device. CS* is an active low signal.  |
| D0 / AD0<br>to<br>D7 / AD7 | 19<br>to<br>12 | I/O | <b>Data Bus/Address/Data Bus.</b> In nonmultiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the data bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), serves as an 8-bit multiplexed address/data bus.   |
| HRST*                      | 29             | I   | <b>Hardware Reset.</b> Bringing HRST* low will reset the DS21348 setting all control bits to their default state of all zeros.  |
| INT*                       | 23             | O   | <b>Interrupt [INT*] Pin 23.</b> Flags host controller during conditions and change of conditions defined in the Status Register. Active low, open drain output.   |
| MCLK                       | 30             | I   | <b>Master Clock.</b> A 2.048MHz ( $\pm 50$ ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544 MHz clock source is optional. See Note 2.   |
| NA                         | -              | I   | <b>Not Assigned.</b> Should be tied low.  |
| PBEO                       | 24             | O   | <b>PRBS Bit Error Output.</b> The receiver will constantly search for a $2^{15}-1$ or a $2^{20}-1$ PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1. |
| PBTS                       | 44             | I   | <b>Parallel Bus Type Select.</b> When using the parallel port (BIS1 = 0), set high to select Motorola bus timing, set low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If PBTS = 1 and BIS1 = 0, then these pins assume the Motorola function listed in parenthesis (). In serial port mode, this pin should be tied low.   |

| ACRONYM               | PIN       | I/O | DESCRIPTION  |
|-----------------------|-----------|-----|--|
| <b>RCLK</b>           | 40        | O   | <b>Receive Clock.</b> Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.  |
| RD*<br>(DS*)          | 2         | I   | <b>Read Input (Data Strobe).</b> RD* and DS* are active low signals. DS active low when in nonmultiplexed, Motorola mode. See the <i>Bus Timing Diagrams</i> in Section 12.  |
| RCL/<br>LOTC          | 25        | O   | <b>Receive Carrier Loss/Loss of Transmit Clock.</b> An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for 5 $\mu$ sec $\pm$ 2 $\mu$ sec (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.   |
| <b>RNEG</b>           | 39        | O   | <b>Receive Negative Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 8.4 for details. |
| RPOS                  | 38        | O   | <b>Receive Positive Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See Section 8.4 for details.     |
| RTIP/<br>RRING        | 27/<br>28 | I   | <b>Receive Tip and Ring.</b> Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 7 for details.  |
| TCLK                  | 43        | I   | <b>Transmit Clock.</b> A 2.048MHz or 1.544MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 3-3.  |
| TEST                  | 26        | I   | <b>3-State Control.</b> Set high to 3-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.   |
| TNEG                  | 42        | I   | <b>Transmit Negative Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TPOS                  | 41        | I   | <b>Transmit Positive Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TTIP/<br>TRING        | 34/<br>37 | O   | <b>Transmit Tip and Ring [TTIP &amp; TRING].</b> Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 7 for details.  |
| <b>V<sub>DD</sub></b> | 21/<br>36 | -   | <b>Positive Supply.</b> 5.0V $\pm$ 5%  |
| VSM                   | 20        | I   | <b>Voltage Supply Mode.</b> Should be tied high for 5V operation.  |
| V <sub>SS</sub>       | 22/<br>35 | -   | <b>Signal Ground.</b>  |

| ACRONYM       | PIN | I/O | DESCRIPTION  |
|---------------|-----|-----|--|
| WR*<br>(R/W*) | 3   | I   | <b>Write Input (Read/Write).</b> WR* is an active low signal. See the Bus Timing Diagrams in section 12. |

### PIN ASSIGNMENT IN SERIAL PORT MODE Table 4-3a

| DS21348T<br>PIN # | DS21348G<br>PIN# | I/O | Serial<br>Port Mode |
|-------------------|------------------|-----|---------------------|
| 1                 | C3               | I   | CS*                 |
| 2                 | C2               | I   | NA                  |
| 3                 | B1               | I   | NA                  |
| 4                 | D2               | I   | NA                  |
| 5                 | C1               | I   | SCLK                |
| 6                 | D3               | I   | SDI                 |
| 7                 | D1               | I/O | SDO                 |
| 8                 | E1               | I   | ICES                |
| 9                 | F2               | I   | OCES                |
| 10                | F1               | I   | NA                  |
| 11                | G1               | I   | NA                  |
| 12                | E3               | I/O | NA                  |
| 13                | F3               | I/O | NA                  |
| 14                | G2               | I/O | NA                  |
| 15                | F4               | I/O | NA                  |
| 16                | G3               | I/O | NA                  |
| 17                | E4               | I/O | NA                  |
| 18                | G4               | I/O | NA                  |
| 19                | F5               | I/O | NA                  |
| 20                | G5               | I   | VSM                 |
| 21                | F6               | -   | VDD                 |
| 22                | G6               | -   | VSS                 |
| 23                | E5               | I/O | INT*                |
| 24                | E6               | O   | PBEO                |
| 25                | F7               | O   | RCL/LOTCL           |
| 26                | D6               | I   | TEST                |
| 27                | D5               | I   | RTIP                |
| 28                | D7               | I   | RRING               |
| 29                | C6               | I   | HRST*               |
| 30                | C7               | I   | MCLK                |
| 31                | B6               | O   | BPCLK               |
| 32                | B7               | I   | BIS0                |
| 33                | A7               | I   | BIS1                |
| 34                | C5               | O   | TTIP                |
| 35                | B5               | -   | V <sub>SS</sub>     |
| 36                | A6               | -   | V <sub>DD</sub>     |
| 37                | B4               | O   | TRING               |
| 38                | C4               | O   | RPOS                |
| 39                | A4               | O   | RNEG                |

| DS21348T<br>PIN # | DS21348G<br>PIN# | I/O | Serial<br>Port Mode |
|-------------------|------------------|-----|---------------------|
| 40                | B3               | O   | RCLK                |
| 41                | A3               | I   | TPOS                |
| 42                | B2               | I   | TNEG                |
| 43                | A2               | I   | TCLK                |
| 44                | A1               | I   | NA                  |

**PIN DESCRIPTIONS IN SERIAL PORT MODE** (Sorted by Pin Name, DS21348T Pin Numbering) Table 4-3b

| ACRONYM       | PIN       | I/O | DESCRIPTION   |
|---------------|-----------|-----|---|
| BIS0/<br>BIS1 | 32/<br>33 | I   | <b>Bus Interface Select Bits 0 &amp; 1.</b> Used to select bus interface option. See Table 4-1 for details.   |
| BPCLK         | 31        | O   | <b>Back Plane Clock.</b> A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384 MHz output.  |
| CS*           | 1         | I   | <b>Chip Select.</b> Must be low to read or write to the device. CS* is an active low signal.  |
| HRST*         | 29        | I   | <b>Hardware Reset.</b> Bringing HRST* low will reset the DS21348 setting all control bits to their default state of all zeros.  |
| ICES          | 8         | I   | <b>Input Clock Edge Select.</b> Selects whether the serial port data input (SDI) is sampled on rising (ICES =0) or falling edge (ICES = 1) of SCLK.   |
| INT*          | 23        | O   | <b>Interrupt [INT*] Pin 23.</b> Flags host controller during conditions and change of conditions defined in the Status Register. Active low, open drain output.   |
| MCLK          | 30        | I   | <b>Master Clock.</b> A 2.048MHz ( $\pm 50$ ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544 MHz clock source is optional. See Note 2.   |
| NA            | -         | I   | <b>Not Assigned.</b> Should be tied low.  |
| OCES          | 9         | I   | <b>Output Clock Edge Select.</b> Selects whether the serial port data output (SDO) is valid on the rising (OCES = 1) or falling edge (OCES = 0) of SCLK.  |
| PBEO          | 24        | O   | <b>PRBS Bit Error Output.</b> The receiver will constantly search for a $2^{15}-1$ or a $2^{20}-1$ PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1. |
| RCLK          | 40        | O   | <b>Receive Clock.</b> Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.   |

| ACRONYM         | PIN       | I/O | DESCRIPTION  |
|-----------------|-----------|-----|--|
| RCL/<br>LOTC    | 25        | O   | <b>Receive Carrier Loss/Loss of Transmit Clock.</b> An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for $5 \mu\text{sec} \pm 2 \mu\text{sec}$ (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.   |
| RNEG            | 39        | O   | <b>Receive Negative Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details. |
| RPOS            | 38        | O   | <b>Receive Positive Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details.     |
| RTIP/<br>RRING  | 27/<br>28 | I   | <b>Receive Tip and Ring.</b> Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 7 for details.  |
| SCLK            | 5         | I   | <b>Serial Clock.</b> Serial bus clock input.   |
| SDI             | 6         | I   | <b>Serial Data Input.</b> Sampled on rising edge (ICES = 0) or the falling edge (ICES = 1) of SCLK.  |
| SDO             | 7         | O   | <b>Serial Data Output.</b> Valid on the falling edge (OCES = 0) or the rising edge (OCES = 1) of SCLK.   |
| TCLK            | 43        | I   | <b>Transmit Clock.</b> A 2.048MHz or 1.544MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 3-3.  |
| TEST            | 26        | I   | <b>3-State Control.</b> Set high to 3-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.   |
| TNEG            | 42        | I   | <b>Transmit Negative Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TPOS            | 41        | I   | <b>Transmit Positive Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TTIP/<br>TRING  | 34/<br>37 | O   | <b>Transmit Tip and Ring [TTIP &amp; TRING].</b> Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 7 for details.  |
| V <sub>DD</sub> | 21/<br>36 | -   | <b>Positive Supply.</b> 5.0V $\pm$ 5%  |
| VSM             | 20        | I   | <b>Voltage Supply Mode.</b> Should be tied high for 5V operation.  |
| V <sub>SS</sub> | 22/<br>35 | -   | <b>Signal Ground.</b>  |

**PIN ASSIGNMENT IN HARDWARE MODE Table 4-4a**

| DS21348T<br>PIN # | DS21348G<br>PIN# | I/O | Hardware<br>Mode |
|-------------------|------------------|-----|------------------|
| 1                 | C3               | I   | EGL              |
| 2                 | C2               | I   | ETS              |
| 3                 | B1               | I   | NRZE             |
| 4                 | D2               | I   | SCLKE            |
| 5                 | C1               | I   | L2               |
| 6                 | D3               | I   | L1               |
| 7                 | D1               | I/O | L0               |
| 8                 | E1               | I   | DJA              |
| 9                 | F2               | I   | JAMUX            |
| 10                | F1               | I   | JAS              |
| 11                | G1               | I   | HBE              |
| 12                | E3               | I/O | CES              |
| 13                | F3               | I/O | TPD              |
| 14                | G2               | I/O | TX0              |
| 15                | F4               | I/O | TX1              |
| 16                | G3               | I/O | LOOP0            |
| 17                | E4               | I/O | LOOP1            |
| 18                | G4               | I/O | MM0              |
| 19                | F5               | I/O | MM1              |
| 20                | G5               | I   | VSM              |
| 21                | F6               | -   | VDD              |
| 22                | G6               | -   | VSS              |
| 23                | E5               | I/O | RT1              |
| 24                | E6               | O   | PBEO             |
| 25                | F7               | O   | RCL              |
| 26                | D6               | I   | TEST             |
| 27                | D5               | I   | RTIP             |
| 28                | D7               | I   | RRING            |
| 29                | C6               | I   | HRST*            |
| 30                | C7               | I   | MCLK             |
| 31                | B6               | O   | BPCLK            |
| 32                | B7               | I   | BIS0             |
| 33                | A7               | I   | BIS1             |
| 34                | C5               | O   | TTIP             |
| 35                | B5               | -   | V <sub>SS</sub>  |
| 36                | A6               | -   | V <sub>DD</sub>  |
| 37                | B4               | O   | TRING            |
| 38                | C4               | O   | RPOS             |
| 39                | A4               | O   | RNEG             |
| 40                | B3               | O   | RCLK             |
| 41                | A3               | I   | TPOS             |
| 42                | B2               | I   | TNEG             |
| 43                | A2               | I   | TCLK             |
| 44                | A1               | I   | RT0              |



**PIN DESCRIPTIONS IN HARDWARE MODE** (Sorted by Pin Name, DS21348T Pin Numbering) Table 4-4b

| ACRONYM         | PIN           | I/O | DESCRIPTION   |
|-----------------|---------------|-----|---|
| BIS0/<br>BIS1   | 32/<br>33     | I   | <b>Bus Interface Select Bits 0 &amp; 1.</b> Used to select bus interface option. See Table 4-1 for details.   |
| BPCLK           | 31            | O   | <b>Back Plane Clock.</b> A 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384MHz output.   |
| CES             | 12            | I   | <b>Receive &amp; Transmit Clock Edge Select.</b> Selects which RCLK edge to update RPOS and RNEG and which TCLK edge to sample TPOS and TNEG. CES combines TCES (CCR2.1) and RCES (CCR2.0).<br>0 = update RNEG/RPOS on rising edge of RCLK; sample TPOS/TNEG on falling edge of TCLK<br>1 = update RNEG/RPOS on falling edge of RCLK; sample TPOS/TNEG on rising edge of TCLK |
| DJA             | 8             | I   | <b>Disable Jitter Attenuator.</b><br>0 = jitter attenuator enabled<br>1 = jitter attenuator disabled  |
| EGL             | 1             | I   | <b>Receive Equalizer Gain Limit.</b> This bit controls the sensitivity of the receive equalizer. See Table 4-7.   |
| ETS             | 2             | I   | <b>E1/T1 Select.</b><br>0 = E1<br>1 = T1  |
| HBE             | 11            | I   | <b>Receive &amp; Transmit HDB3/B8ZS Enable.</b> HBE combines RHBE (CCR2.3) and THBE (CCR2.2).<br>0 = enable HDB3 (E1)/B8ZS (T1)<br>1 = disable HDB3 (E1)/B8ZS (T1)  |
| HRST*           | 29            | I   | <b>Hardware Reset.</b> Bringing HRST* low will reset the DS21348 setting all control bits to their default state of all zeros.  |
| JAMUX           | 9             | I   | <b>Jitter Attenuator MUX.</b> Controls the source for JACLK. See Figure 3-1 and Table 4-10.<br>0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK)<br>1 = JACLK sourced from internal PLL (2.048MHz at MCLK)   |
| JAS             | 10            | I   | <b>Jitter Attenuator Select.</b><br>0 = place the jitter attenuator on the receive side<br>1 = place the jitter attenuator on the transmit side   |
| L0/L1/L2        | 7/<br>6/<br>5 | I   | <b>Transmit LIU Waveshape Select Bits 0 &amp; 1 [H/W Mode].</b> These inputs determine the waveshape of the transmitter. See Table 9-1 and Table 9-2.   |
| LOOP0/<br>LOOP1 | 16/<br>17     | I   | <b>Loopback Select Bits 0 &amp; 1 [H/W Mode].</b> These inputs determine the active loopback mode (if any). See Table 4-5.  |

| ACRONYM        | PIN       | I/O | DESCRIPTION   |
|----------------|-----------|-----|---|
| MCLK           | 30        | I   | <b>Master Clock.</b> A 2.048MHz ( $\pm 50$ ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544MHz clock source is optional.<br>See Note 2.   |
| MM0/<br>MM1    | 18/<br>19 | I   | <b>Monitor Mode Select Bits 0 &amp; 1 [H/W Mode].</b> These inputs determine if the receive equalizer is in a monitor mode.<br>See Table 4-8.   |
| NA             | -         | I   | <b>Not Assigned.</b> Should be tied low.  |
| NRZE           | 3         | I   | <b>NRZ Enable [H/W Mode].</b><br>0 = Bipolar data at RPOS/RNEG and TPOS/TNEG<br>1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive going pulse when device receives a BPV, CV, or EXZ.  |
| PBEO           | 24        | O   | <b>PRBS Bit Error Output.</b> The receiver will constantly search for a $2^{15}-1$ or a $2^{20}-1$ PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1. |
| RCLK           | 40        | O   | <b>Receive Clock.</b> Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.   |
| RCL            | 25        | O   | <b>Receive Carrier Loss.</b> An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for $5 \mu\text{sec} \pm 2 \mu\text{sec}$ (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.   |
| RNEG           | 39        | O   | <b>Receive Negative Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details.  |
| RPOS           | 38        | O   | <b>Receive Positive Data.</b> Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details.  |
| RT0/<br>RT1    | 44/<br>23 | I   | <b>Receive LIU Termination Select Bits 0 &amp; 1 [H/W Mode].</b> These inputs determine the receive termination. See Table 4-9.   |
| RTIP/<br>RRING | 27/<br>28 | I   | <b>Receive Tip and Ring.</b> Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 7 for details.   |

| ACRONYM         | PIN       | I/O | DESCRIPTION  |
|-----------------|-----------|-----|--|
| SCLKE           | 4         | I   | <b>Receive &amp; Transmit Synchronization Clock Enable.</b> SCLKE combines RSCLKE (CCR5.3) and TSCLKE (CCR5.2).<br>0 = disable 2.048 MHz synchronization transmit and receive mode<br>1 = enable 2.048 MHz synchronization transmit and receive mode |
| TCLK            | 43        | I   | <b>Transmit Clock.</b> A 2.048MHz or 1.544MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 3-3.  |
| TEST            | 26        | I   | <b>3-State Control.</b> Set high to 3-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.   |
| TNEG            | 42        | I   | <b>Transmit Negative Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TPD             | 13        | I   | <b>Transmit Power-Down.</b><br>0 = normal transmitter operation<br>1 = powers down the transmitter and 3-states the TTIP and TRING pins  |
| TPOS            | 41        | I   | <b>Transmit Positive Data.</b> Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.  |
| TTIP/<br>TRING  | 34/<br>37 | O   | <b>Transmit Tip and Ring [TTIP &amp; TRING].</b> Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 7 for details.  |
| TX0/<br>TX1     | 14/<br>15 | I   | <b>Transmit Data Source Select Bits 0 &amp; 1 [H/W Mode].</b> These inputs determine the source of the transmit data. See Table 4-6.   |
| V <sub>DD</sub> | 21/<br>36 | -   | <b>Positive Supply.</b> 5.0V ±5%   |
| VSM             | 20        | I   | <b>Voltage Supply Mode.</b> Should be tied high for 5V operation.  |
| V <sub>SS</sub> | 22/<br>35 | -   | <b>Signal Ground.</b>  |

**NOTES:**

- 1) G.703 requires an accuracy of ±50ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of ±32ppm for T1 interfaces.
- 2) \* Denotes active low.

**LOOP BACK CONTROL IN HARDWARE MODE** Table 4-5

| LOOPBACK         | SYMBOL | CONTROL BIT | LOOP1 | LOOP0 |
|------------------|--------|-------------|-------|-------|
| Remote Loop Back | RLB    | CCR6.6      | 1     | 1     |
| Local Loop Back  | LLB    | CCR6.7      | 1     | 0     |
| Analog Loop Back | ALB    | CCR6.4      | 0     | 1     |
| No Loop Back     | -      | -           | 0     | 0     |

**TRANSMIT DATA CONTROL IN HARDWARE MODE** Table 4-6

| TRANSMIT DATA                       | SYMBOL | CONTROL BIT | TX1 | TX0 |
|-------------------------------------|--------|-------------|-----|-----|
| Transmit Unframed All Ones          | TUA1   | CCR3.7      | 1   | 1   |
| Transmit Alternating Ones and Zeros | TAOZ   | CCR3.5      | 1   | 0   |
| Transmit PRBS                       | TPRBSE | CCR3.4      | 0   | 1   |
| TPOS and TNEG                       | -      | -           | 0   | 0   |

**RECEIVE SENSITIVITY SETTINGS** Table 4-7

| EGL<br>(CCR4.4) | ETS<br>(CCR1.7) | RECEIVE SENSITIVITY        |
|-----------------|-----------------|----------------------------|
| 0               | 0 (E1)          | -12 dB (short haul)        |
| 1               | 0 (E1)          | -43 dB (long haul)         |
| 1               | 1 (T1)          | -30 dB (limited long haul) |
| 0               | 1 (T1)          | -36 dB (long haul)         |

**MONITOR GAIN SETTINGS** Table 4-8

| MM1<br>(CCR5.5) | MM0<br>(CCR5.4) | INTERNAL LINEAR GAIN<br>BOOST (dB) |
|-----------------|-----------------|------------------------------------|
| 0               | 0               | Normal operation (no boost)        |
| 0               | 1               | 20                                 |
| 1               | 0               | 26                                 |
| 1               | 1               | 32                                 |

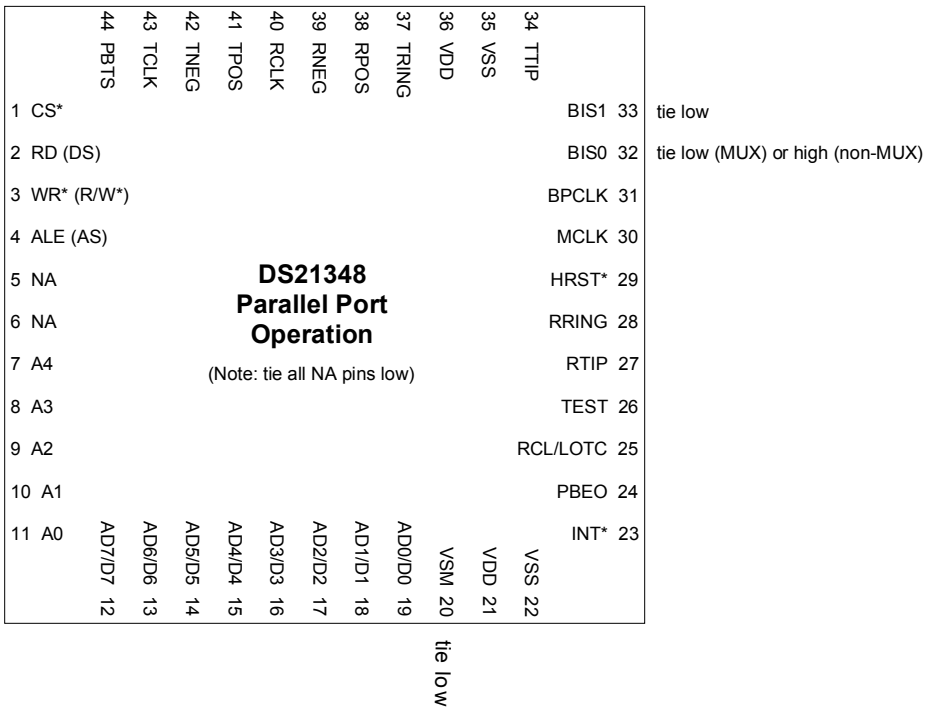
**INTERNAL RX TERMINATION SELECT** Table 4-9

| RT1<br>(CCR5.1) | RT0<br>(CCR5.0) | INTERNAL RECEIVE<br>TERMINATION CONFIGURATION |
|-----------------|-----------------|---|
| 0               | 0               | Internal receive-side termination disabled    |
| 0               | 1               | Internal receive-side 120Ω enabled            |
| 1               | 0               | Internal receive-side 100Ω enabled            |
| 1               | 1               | Internal receive-side 75Ω enabled             |

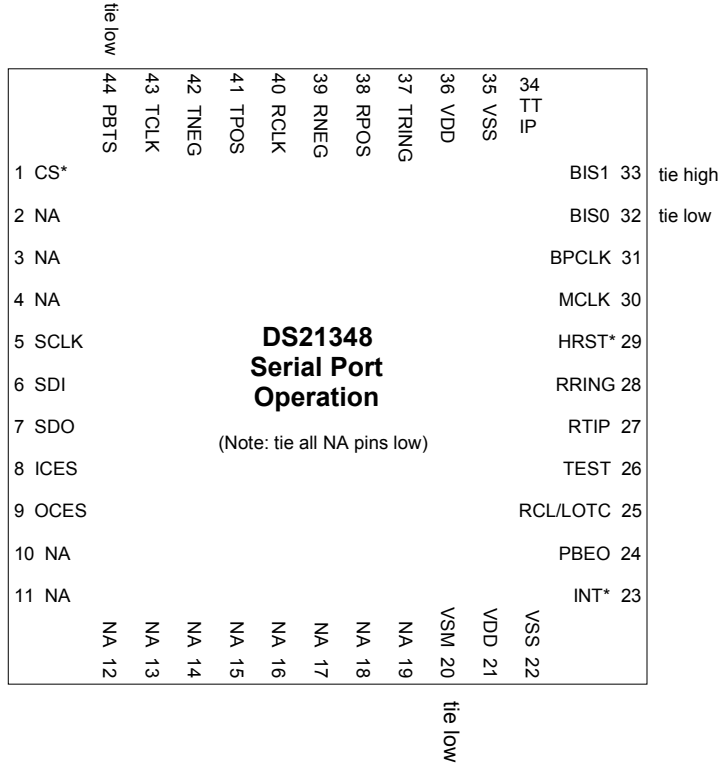
**MCLK SELECTION** Table 4-10

| MCLK     | JAMUX<br>(CCR1.3) | ETS<br>(CCR1.7) |
|----------|-------------------|-----------------|
| 2.048MHz | 0                 | 0               |
| 2.048MHz | 1                 | 1               |
| 1.544MHz | 0                 | 1               |

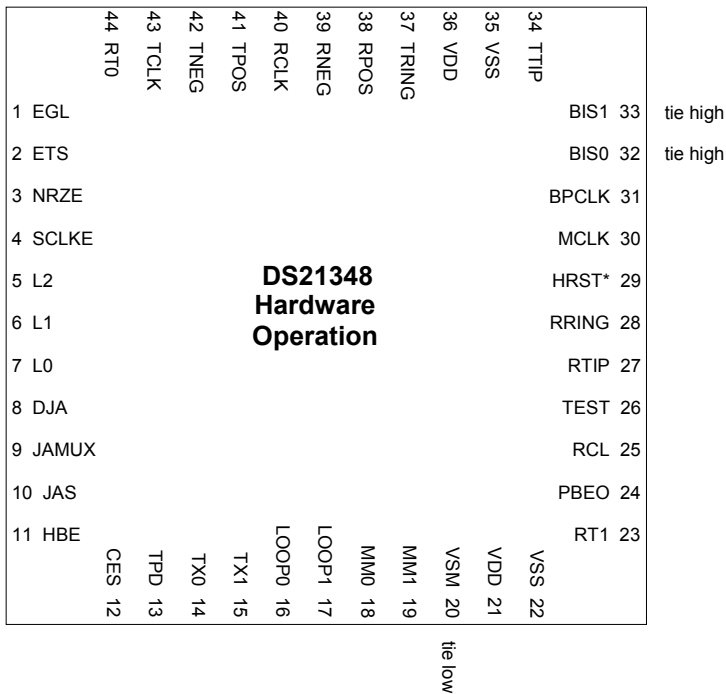
## PARALLEL PORT MODE PINOUT (BIS1 = 0, BIS0 = 1 or 0) Figure 4-1



## SERIAL PORT MODE PINOUT (BIS1 = 1, BIS0 = 0) Figure 4-2



## HARDWARE MODE PINOUT (BIS1 = 1, BIS0 = 1) Figure 4-3



## 5. HARDWARE MODE

In hardware mode (BIS1 = 1, BIS0 = 1), pins 1-19, 23, 25, 31, and 44 are redefined to be used for initializing the DS21348. BPCLK (pin 31) defaults to a 16.384MHz output when in hardware mode. The RCL/LOTC (pin 25) is designated to RCL when in hardware mode. JABDS (CCR4.2) defaults to logic 0. The RHBE (CCR2.3) and THBE (CCR2.2) control bits are combined and controlled by HBE at pin 11 while the RSCLKE (CCR5.3) and TSCLKE (CCR5.2) bits are combined and controlled by SCLKE at pin 4. TCES (CCR2.1) and RCES (CCR2.0) are combined and controlled by CES at pin 12. The transmitter functions are combined and controlled by TX1 (pin 15) and TX0 (pin 14). The loopback functions are controlled by LOOP1 (pin 17) and LOOP0 (pin 16). All other control bits default to the logic 0 setting.

## 5.1 Register Map

Table 5-1 REGISTER MAP

| ACRONYM | REGISTER NAME                           | R/W | PARALLEL PORT MODE | SERIAL PORT MODE<br>See Notes 2 - 5<br>(msb) (lsb) |
|---------|---|-----|--------------------|--|
| CCR1    | Common Control Register 1               | R/W | 00h                | B000 000A  |
| CCR2    | Common Control Register 2               | R/W | 01h                | B000 001A  |
| CCR3    | Common Control Register 3               | R/W | 02h                | B000 010A  |
| CCR4    | Common Control Register 4               | R/W | 03h                | B000 011A  |
| CCR5    | Common Control Register 5               | R/W | 04h                | B000 100A  |
| CCR6    | Common Control Register 6               | R/W | 05h                | B000 101A  |
| SR      | Status Register                         | R   | 06h                | B000 110A  |
| IMR     | Interrupt Mask Register                 | R/W | 07h                | B000 111A  |
| RIR1    | Receive Information Register 1          | R   | 08h                | B001 000A  |
| RIR2    | Receive Information Register 2          | R   | 09h                | B001 001A  |
| IBCC    | In-Band Code Control Register           | R/W | 0Ah                | B001 010A  |
| TCD1    | Transmit Code Definition Register 1     | R/W | 0Bh                | B001 011A  |
| TCD2    | Transmit Code Definition Register 2     | R/W | 0Ch                | B001 100A  |
| RUPCD1  | Receive Up Code Definition Register 1   | R/W | 0Dh                | B001 101A  |
| RUPCD2  | Receive Up Code Definition Register 2   | R/W | 0Eh                | B001 110A  |
| RDNCD1  | Receive Down Code Definition Register 1 | R/W | 0Fh                | B001 111A  |
| RDNCD2  | Receive Down Code Definition Register 2 | R/W | 10h                | B010 000A  |
| ECR1    | Error Count Register 1                  | R   | 11h                | B010 001A  |
| ECR2    | Error Count Register 2                  | R   | 12h                | B010 010A  |
| TEST1   | Test 1                                  | R/W | 13h                | B010 011A  |
| TEST2   | Test 2                                  | R/W | 14h                | B010 100A  |
| TEST2   | Test 3                                  | R/W | 15h                | B010 101A  |
| -       | -                                       | -   | Note 1             | -  |

### NOTES:

- 1) Register addresses 16h to 1Fh do not exist.
- 2) In the Serial Port Mode, the LSB is on the right hand side.
- 3) In the Serial Port Mode, data is read and written LSB first.
- 4) In the Serial Port Mode, the A bit (the LSB) determines whether the access is a read (A = 1) or a write (A = 0).
- 5) In the Serial Port Mode, the B bit (the MSB) determines whether the access is a burst access (B = 1) or a single register access (B = 0).

## 5.2 Parallel Port Operation

When using the parallel interface on the DS21348 (BIS1 = 0) the user has the option for either multiplexed bus operation (BIS1 = 0, BIS0 = 0) or non-multiplexed bus operation (BIS1 = 0, BIS0 = 1). The DS21348 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in Section 12 for more details.

## 5.3 Serial Port Operation

Setting BIS1 = 1 and BIS0 = 0 enables the serial bus interface on the DS21348. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 12 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 5-1, Figure 5-2, Figure 5-3, and Figure 5-4 for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 5 bits identify the register address. Bit 7 is reserved and must be set to 0 for proper operation.

The last bit (MSB) of the address/command byte is the burst mode bit. When the burst bit is enabled (B = 0) and a READ operation is performed, addresses 0 through 15h are read sequentially, starting at address 0h. And when the burst bit is enabled and a WRITE operation is performed, addresses 0 through 16h are written sequentially, starting at address 0h. Burst operation is stopped once address 15h is read. See Figure 5-5 and Figure 5-6 for more details.

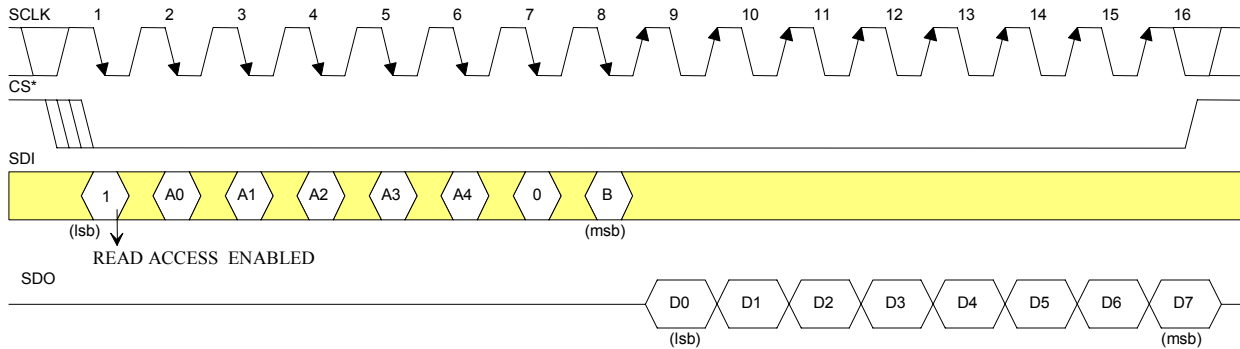
All data transfers are initiated by driving the CS\* input low. When Input Clock-Edge Select (ICES) is low, input data is latched on the rising edge of SCLK and when ICES is high, input data is latched on the falling edge of SCLK. When Output Clock-Edge Select (OCES) is low, data is output on the falling edge of SCLK and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the CS\* input transitions high. Port control logic is disabled and SDO is 3-stated when CS\* is high.



## SERIAL PORT OPERATION FOR READ ACCESS (R=1) MODE 1 Figure 5-1

ICES = 1 (sample SDI on the falling edge of SCLK)

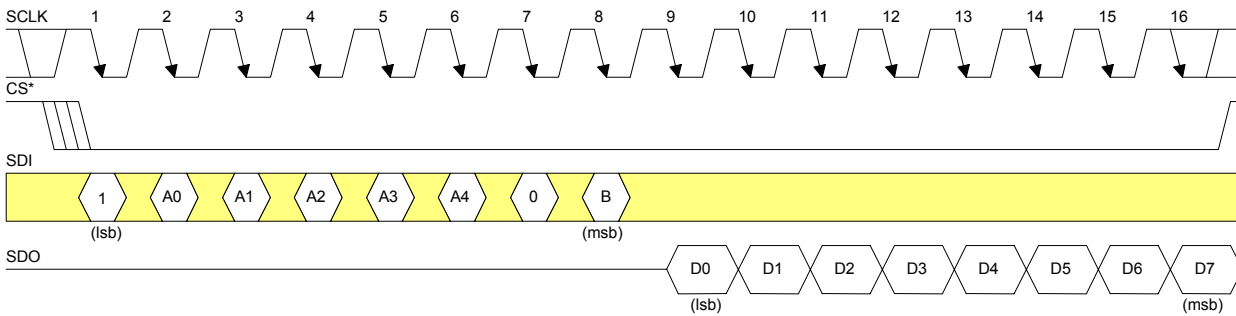
OCES = 1 (update SDO on rising edge of SCLK)



## SERIAL PORT OPERATION FOR READ ACCESS MODE 2 Figure 5-2

ICES = 1 (sample SDI on the falling edge of SCLK)

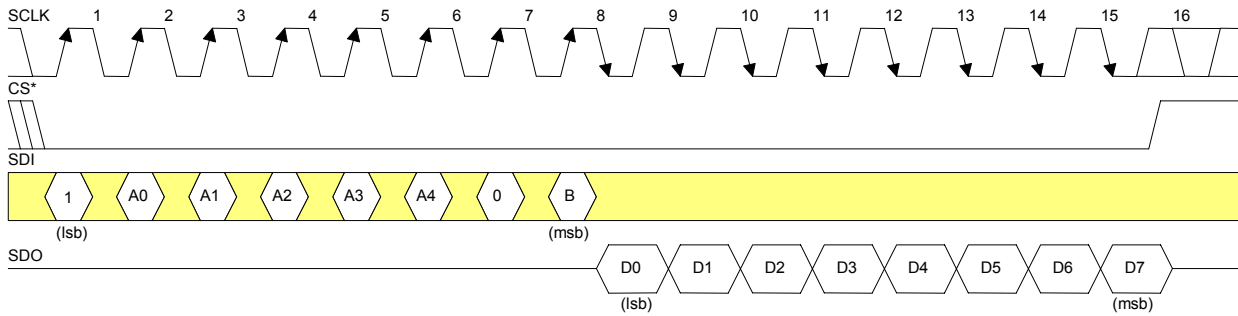
OCES = 0 (update SDO on falling edge of SCLK)



### SERIAL PORT OPERATION FOR READ ACCESS MODE 3 Figure 5-3

ICES = 0 (sample SDI on the rising edge of SCLK)

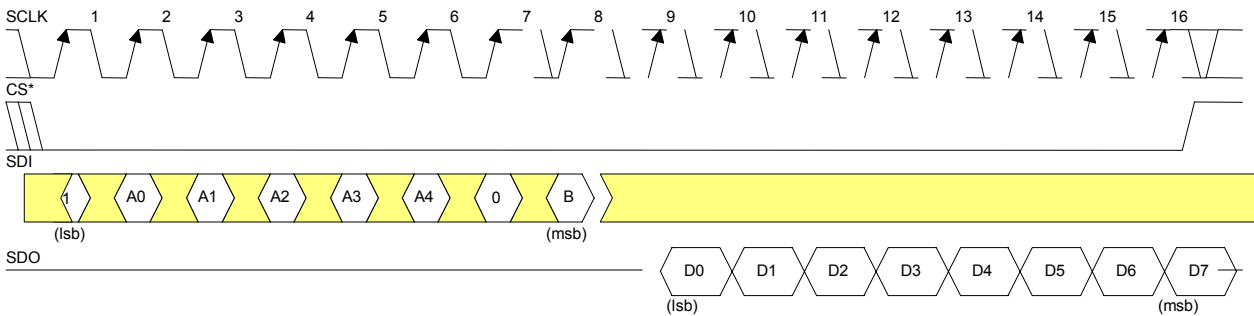
OCES = 0 (update SDO on falling edge of SCLK)



### SERIAL PORT OPERATION FOR READ ACCESS MODE 4 Figure 5-4

ICES = 0 (sample SDI on the rising edge of SCLK)

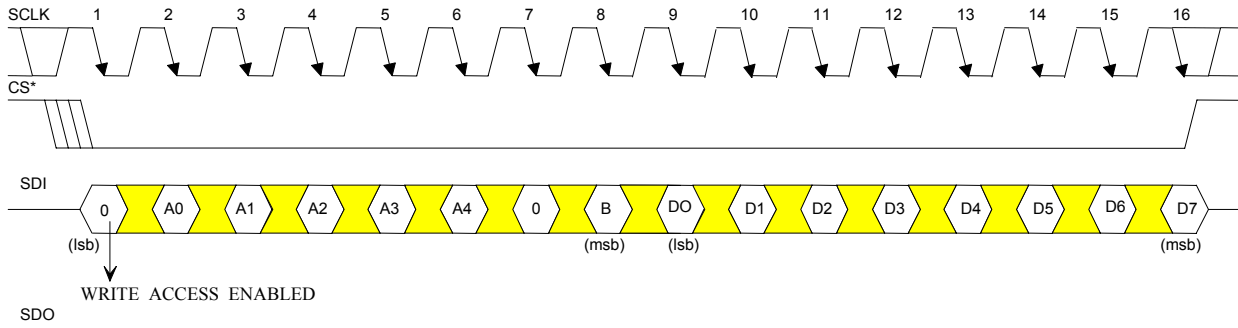
OCES = 1 (update SDO on rising edge of SCLK)



D0

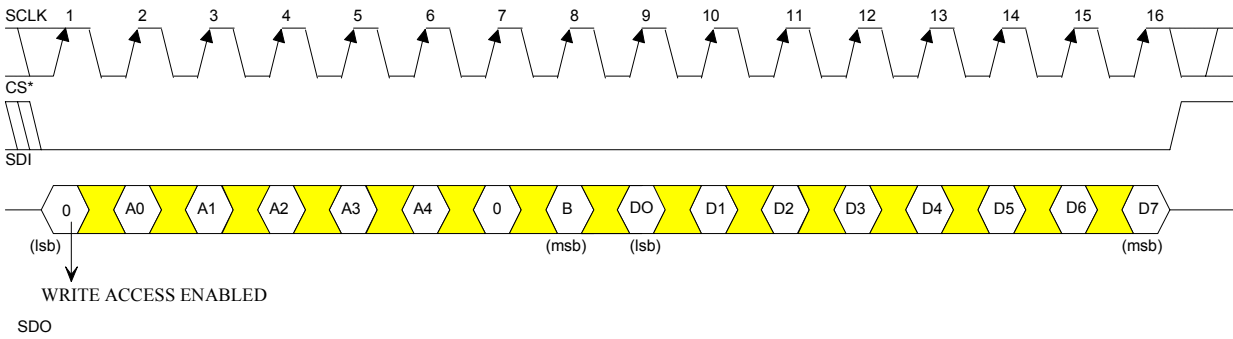
## SERIAL PORT OPERATION FOR WRITE ACCESS (R=0) MODES 1 & 2 Figure 5-5

ICES = 1 (sample SDI on the falling edge of SCLK)



## SERIAL PORT OPERATION FOR WRITE ACCESS (R=0) MODES 3 & 4 Figure 5-6

ICES = 0 (sample SDI on the rising edge of SCLK)



## 6. CONTROL REGISTERS

### CCR1 (00H): COMMON CONTROL REGISTER 1

| (MSB) |      |      |      |       |      |      | (LSB)  |
|-------|------|------|------|-------|------|------|--------|
| ETS   | NRZE | RCLA | ECUE | JAMUX | TTOJ | TTOR | LOTCCM |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| ETS    | CCR1.7   | <b>E1/T1 Select.</b><br>0 = E1<br>1 = T1  |
| NRZE   | CCR1.6   | <b>NRZ Enable.</b><br>0 = Bipolar data at RPOS/RNEG and TPOS/TNEG<br>1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive going pulse when device receives a BPV, CV, or EXZ.   |
| RCLA   | CCR1.5   | <b>Receive Carrier Loss Alternate Criteria.</b><br>0 = RCL declared upon 255 (E1) or 192 (T1) consecutive zeros<br>1 = RCL declared upon 2048 (E1) or 1544 (T1) consecutive zeros   |
| ECUE   | CCR1.4   | <b>Error Counter Update Enable.</b> A 0 to 1 transition forces the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of two clocks cycles (976ns for E1 and 1296ns for T1) before reading the error count registers to allow for a proper update. See Section 6 for details. |
| JAMUX  | CCR1.3   | <b>Jitter Attenuator MUX.</b> Controls the source for JACLK. See .<br>0 = JACLK sourced from MCLK (2.048MHz or 1.544MHz at MCLK)<br>1 = JACLK sourced from internal PLL (2.048MHz at MCLK)  |
| TTOJ   | CCR1.2   | <b>TCLK to JACLK.</b> Internally connects TCLK to JACLK. See .<br>0 = disabled<br>1 = enabled   |
| TTOR   | CCR1.1   | <b>TCLK to RCLK.</b> Internally connects TCLK to RCLK. See .<br>0 = disabled<br>1 = enabled   |
| LOTCCM | CCR1.0   | <b>Loss Of Transmit Clock Mux Control.</b> Determines whether the transmit logic should switch to JACLK if the TCLK input should fail to transition. See .<br>0 = do not switch to JACLK if TCLK stops<br>1 = switch to JACLK if TCLK stops   |

**MCLK SELECTION Table 6-1**

| MCLK     | JAMUX<br>(CCR1.3) | ETS<br>(CCR1.7) |
|----------|-------------------|-----------------|
| 2.048MHz | 0                 | 0               |
| 2.048MHz | 1                 | 1               |
| 1.544MHz | 0                 | 1               |

**CCR2 (01H): COMMON CONTROL REGISTER 2**

| (MSB) |     |      |      |      |      |      | (LSB) |
|-------|-----|------|------|------|------|------|-------|
| P25S  | n/a | SCLD | CLDS | RHBE | THBE | TCES | RCES  |

| SYMBOL | POSITION | DESCRIPTION  |
|--------|----------|--|
| P25S   | CCR2.7   | <b>Pin 25 Select.</b> Forced to logic 0 in hardware mode.<br>0 = toggles high during a Receive Carrier Loss condition<br>1 = toggles high if TCLK does not transition for at least 5 $\mu$ s   |
| -      | CCR2.6   | <b>Not Assigned. Should be set to zero when written to.</b>  |
| SCLD   | CCR2.5   | <b>Short Circuit Limit Disable (ETS = 0).</b> Controls the 50 mA (rms) current limiter.<br>0 = enable 50 mA current limiter<br><b>1 = disable 50 mA current limiter</b>  |
| CLDS   | CCR2.4   | <b>Custom Line Driver Select.</b> Setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and CCR4.5 = CCR4.6 = CCR4.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and CCR4.5 = CCR4.6 = CCR4.7 $\neq$ 0, then the device will force TTIP and TRING outputs to become open drain drivers instead of their normal push-pull operation. <b>This bit should be set to zero for normal operation of the device.</b> Contact the factory for more details on how to use this bit. |
| RHBE   | CCR2.3   | <b>Receive HDB3/B8ZS Enable.</b><br>0 = enable HDB3 (E1)/B8ZS (T1)<br>1 = disable HDB3 (E1)/B8ZS (T1)  |
| THBE   | CCR2.2   | <b>Transmit HDB3/B8ZS Enable.</b><br>0 = enable HDB3 (E1)/B8ZS (T1)<br>1 = disable HDB3 (E1)/B8ZS (T1)   |
| TCES   | CCR2.1   | <b>Transmit Clock Edge Select.</b> Selects which TCLK edge to sample TPOS and TNEG.<br>0 = sample TPOS and TNEG on falling edge of TCLK<br>1 = sample TPOS and TNEG on rising edge of TCLK   |
| RCES   | CCR2.0   | <b>Receive Clock Edge Select.</b> Selects which RCLK edge to update RPOS and RNEG.<br>0 = update RPOS and RNEG on rising edge of RCLK<br>1 = update RPOS and RNEG on falling edge of RCLK  |

**CCR3 (02H): COMMON CONTROL REGISTER 3**

| (MSB) |       |      |        |      |       |      | (LSB) |
|-------|-------|------|--------|------|-------|------|-------|
| TUA1  | ATUA1 | TAOZ | TPRBSE | TLCE | LIRST | IBPV | IBE   |

| SYMBOL | POSITION | DESCRIPTION  |
|--------|----------|--|
| TUA1   | CCR3.7   | <b>Transmit Unframed All Ones.</b> The polarity of this bit is set such that the device will transmit an all ones pattern on power-up or device reset. This bit must be set to a one to allow the device to transmit data. The transmission of this data pattern is always timed off of the JACLK (See Figure 3-1).<br>0 = transmit all ones at TTIP and TRING<br>1 = transmit data normally |
| ATUA1  | CCR3.6   | <b>Automatic Transmit Unframed All Ones.</b> Automatically transmit an unframed all ones pattern at TTIP and TRING during a receive carrier loss (RCL) condition or receive all ones condition.<br>0 = disabled<br>1 = enabled   |
| TAOZ   | CCR3.5   | <b>Transmit Alternate Ones and Zeros.</b> Transmit a ...101010... pattern at TTIP and TRING. The transmission of this data pattern is always timed off of TCLK (See Figure 3-1).<br>0 = disabled<br>1 = enabled  |
| TPRBSE | CCR3.4   | <b>Transmit PRBS Enable.</b> Transmit a $2^{15} - 1$ (E1) or a $2^{20} - 1$ (T1) PRBS at TTIP and TRING.<br>0 = disabled<br>1 = enabled  |
| TLCE   | CCR3.3   | <b>Transmit Loop Code Enable.</b> Enables the transmit side to transmit the loop up code in the Transmit Code Definition registers (TCD1 and TCD2). See Section 6 for details.<br>0 = disabled<br><b>1 = enabled</b>   |
| LIRST  | CCR3.2   | <b>Line Interface Reset.</b> Setting this bit from a zero to a one will initiate an internal reset that resets the clock recovery state machine and re-centers the jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.   |
| IBPV   | CCR3.1   | <b>Insert BPV.</b> A 0 to 1 transition on this bit will cause a single BiPolar Violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted. See .                       |
| IBE    | CCR3.0   | <b>Insert Bit Error.</b> A 0 to 1 transition on this bit will cause a single logic error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted. See Figure 3-3.   |

## 6.1 Device Power-Up and Reset

The DS21348 will reset itself upon power-up setting all writeable registers to 00h and clear the status and information registers. CCR3.7 (TUA1) = 0 results in the LIU transmitting unframed all ones. After the power supplies have settled following power-up, initialize all control registers to the desired settings, then toggle the LIRST bit (CCR3.2). At anytime, the DS21348 can be reset to the default settings by bringing HRST\* (pin 29) low (level triggered) or by powering down and powering up again.

### CCR4 (03H): COMMON CONTROL REGISTER 4

| (MSB) |    |    |     | (LSB) |       |     |     |
|-------|----|----|-----|-------|-------|-----|-----|
| L2    | L1 | L0 | EGL | JAS   | JABDS | DJA | TPD |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| L2     | CCR4.7   | <b>Line Build Out Select Bit 2.</b> Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.                                  |
| L1     | CCR4.6   | <b>Line Build Out Select Bit 1.</b> Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.                                  |
| L0     | CCR4.5   | <b>Line Build Out Select Bit 0.</b> Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.                                  |
| EGL    | CCR4.4   | <b>Receive Equalizer Gain Limit.</b> This bit controls the sensitivity of the receive equalizer. See Table 6-2.                                 |
| JAS    | CCR4.3   | <b>Jitter Attenuator Select.</b><br>0 = place the jitter attenuator on the receive side<br>1 = place the jitter attenuator on the transmit side |
| JABDS  | CCR4.2   | <b>Jitter Attenuator Buffer Depth Select.</b><br>0 = 128 bits<br>1 = 32 bits (use for delay sensitive applications)                             |
| DJA    | CCR4.1   | <b>Disable Jitter Attenuator.</b><br>0 = jitter attenuator enabled<br>1 = jitter attenuator disabled  |
| TPD    | CCR4.0   | <b>Transmit Power-Down.</b><br>0 = normal transmitter operation<br>1 = powers down the transmitter and 3-states the TTIP and TRING pins         |

### RECEIVE SENSITIVITY SETTINGS Table 6-2

| EGL<br>(CCR4.4) | ETS<br>(CCR1.7) | RECEIVE SENSITIVITY       |
|-----------------|-----------------|---------------------------|
| 0               | 0 (E1)          | -12dB (short haul)        |
| 1               | 0 (E1)          | -43dB (long haul)         |
| 1               | 1 (T1)          | -30dB (limited long haul) |
| 0               | 1 (T1)          | -36dB (long haul)         |

**CCR5 (04H): COMMON CONTROL REGISTER 5****(MSB)****(LSB)**

|       |       |     |     |        |        |     |     |
|-------|-------|-----|-----|--------|--------|-----|-----|
| BPCS1 | BPCS0 | MM1 | MM0 | RSCLKE | TSCLKE | RT1 | RT0 |
|-------|-------|-----|-----|--------|--------|-----|-----|

| SYMBOL | POSITION | DESCRIPTION  |
|--------|----------|--|
| BPCS1  | CCR5.7   | <b>Back Plane Clock Select 1.</b> See Table 6-3 for details.   |
| BPCS0  | CCR5.6   | <b>Back Plane Clock Select 0.</b> See Table 6-3 for details.   |
| MM1    | CCR5.5   | <b>Monitor Mode 1.</b> See Table 6-4.  |
| MM0    | CCR5.4   | <b>Monitor Mode 0.</b> See Table 6-4.  |
| RSCLKE | CCR5.3   | <b>Receive Synchronization Clock Enable.</b><br>0 = disable 2.048MHz synchronization receive mode<br>1 = enable 2.048MHz synchronization receive mode      |
| TSCLKE | CCR5.2   | <b>Transmit Synchronization Clock Enable.</b><br>0 = disable 2.048MHz transmit synchronization clock<br>1 = enable 2.048MHz transmit synchronization clock |
| RT1    | CCR5.1   | <b>Receive Termination 1.</b> See Table 6-5 for details.   |
| RT0    | CCR5.0   | <b>Receive Termination 0.</b> See Table 6-5 for details.   |

**BACK PLANE CLOCK SELECT Table 6-3**

| BPCS1<br>(CCR5.7) | BPCS0<br>(CCR5.6) | BPCLK FREQUENCY |
|-------------------|-------------------|-----------------|
| 0                 | 0                 | 16.384MHz       |
| 0                 | 1                 | 8.192MHz        |
| 1                 | 0                 | 4.096MHz        |
| 1                 | 1                 | 2.048 MHz       |

**MONITOR GAIN SETTINGS Table 6-4**

| MM1<br>(CCR5.5) | MM0<br>(CCR5.4) | INTERNAL LINEAR<br>GAIN BOOST (dB) |
|-----------------|-----------------|------------------------------------|
| 0               | 0               | Normal operation (no boost)        |
| 0               | 1               | 20                                 |
| 1               | 0               | 26                                 |
| 1               | 1               | 32                                 |



**INTERNAL RX TERMINATION SELECT Table 6-5**

| RT1<br>(CCR5.1) | RT0<br>(CCR5.0) | INTERNAL RECEIVE<br>TERMINATION CONFIGURATION |
|-----------------|-----------------|---|
| 0               | 0               | Internal receive-side termination disabled    |
| 0               | 1               | Internal receive-side 120Ω enabled            |
| 1               | 0               | Internal receive-side 100Ω enabled            |
| 1               | 1               | Internal receive-side 75Ω enabled             |

**CCR6 (05H): COMMON CONTROL REGISTER 6**

| (MSB) |     |       |     |      |       | (LSB) |       |
|-------|-----|-------|-----|------|-------|-------|-------|
| LLB   | RLB | ARLBE | ALB | RJAB | ECSR2 | ECSR1 | ECSR0 |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| LLB    | CCR6.7   | <b>Local Loopback.</b> In Local Loopback (LLB), transmit data will be looped back to the receive path passing through the jitter attenuator if it is enabled. Data in the transmit path will act as normal. See for details.<br><b>0 = loopback disabled</b><br>1 = loopback enabled  |
| RLB    | CCR6.6   | <b>Remote Loopback.</b> In Remote Loopback (RLB), data output from the clock/data recovery circuitry will be looped back to the transmit path passing through the jitter attenuator if it is enabled. Data in the receive path will act as normal while data presented at TPOS and TNEG will be ignored. See for details.<br><b>0 = loopback disabled</b><br>1 = loopback enabled   |
| ARLBE  | CCR6.5   | <b>Automatic Remote Loopback Enable &amp; Reset.</b> When this bit is set high, the device will automatically go into remote loopback when it detects loop up code programmed into the Receive Loop Up Code Definition Registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds and it will also set the RIR2.1 status bit. Once in a RLB state, it will remain in this state until it has detected the loop code programmed into the Receive Loop Down Code Definition Registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds at which point it will force the device out of RLB and clear RIR2.1. The automatic RLB circuitry can be reset by toggling this bit from a 1 to a 0. The action of the automatic remote loopback circuitry is logically OR'ed with the RLB (CCR6.6) control bit (i.e. either one can cause a RLB to occur). |
| ALB    | CCR6.4   | <b>Analog Loopback.</b> In Analog Loopback (ALB), signals at TTIP and TRING will be internally connected to RTIP and RRING. The incoming signals, from the line, at RTIP and RRING will be ignored. The signals at TTIP and TRING will be transmitted as normal. See for more details.<br><b>0 = loopback disabled</b><br>1 = loopback enabled  |
| RJAB   | CCR6.3   | <b>RCLK Jitter Attenuator Bypass.</b> This control bit allows the   |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
|        |          | receive recovered clock and data to bypass the jitter attenuation while still allowing the BPCLK output to use the jitter attenuator. See for details.<br>0 = disabled<br>1 = enabled |
| ECRS2  | CCR6.2   | <b>Error Count Register Select 2.</b> See Section 8.4 for details.  |
| ECRS1  | CCR6.1   | <b>Error Count Register Select 1.</b> See Section 8.4 for details.  |
| ECRS0  | CCR6.0   | <b>Error Count Register Select 0.</b> See Section 8.4 for details.  |

## 7. STATUS REGISTERS

There are three registers that contain information on the current real time status of the device, Status Register (SR) and Receive Information Registers 1 and 2 (RIR1/RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a one. Some of the bits in SR, RIR1, and RIR2 are latched bits and some are real time bits. The register descriptions below list which status bits are latched and which are real time bits. For latched status bits, when an event or an alarm occurs the bit is set to a one and will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. Two of the latched status bits (RUA1 and RCL) will remain set after reading if the alarm is still present.

The user will always precede a read of any of the three status registers with a write. The byte written to the register will inform the DS21348 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers with a one in the bit positions to be read and a zero in the other bit positions. When a one is written to a bit location, that location will be updated with the latest information. When a zero is written to a bit position, that bit position will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously with respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21348 with higher-order software languages.

The bits in the SR register have the unique ability to initiate a hardware interrupt via the INT\* output pin. Each of the alarms and events in the SR can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register (IMR). The interrupts caused by the RCL, RUA1, and LOTC bits in SR act differently than the interrupts caused by the other status bits in SR. The RCL, RUA1 and LOTC bits will force the INT\* pin low whenever they change state (i.e., go active or inactive). The INT\* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present. The other status bits in SR can force the INT\* pin low when they are set. The INT\* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

**RECEIVED ALARM CRITERIA Table 7-1**

| ALARM            | E1/T1 | SET CRITERIA  | CLEAR CRITERIA  |
|------------------|-------|---|---|
| RUA1             | E1    | Less than 2 zeros in two frames (512 bits)                    | More than 2 zeros in two frames (512 bits)  |
| RUA1             | T1    | Over a 3ms window, five or fewer zeros are received           | Over a 3ms window, six or more zeros are received   |
| RCL <sup>1</sup> | E1    | 255 (or 2048) <sup>2</sup> consecutive zeros received (G.775) | In 255 bit times, at least 32 ones are received   |
| RCL <sup>1</sup> | T1    | 192 (or 1544) <sup>2</sup> consecutive zeros are received     | 14 or more ones out of 112 possible bit positions are received starting with the first one received |

**NOTES:**

- 1) Receive carrier loss (RCL) is also known as loss of signal (LOS) or Red Alarm in T1.
- 2) See CCR1.5 for details.

**SR (06H): STATUS REGISTER**

| (MSB) |     |      |      |     |      | (LSB) |       |
|-------|-----|------|------|-----|------|-------|-------|
| LUP   | LDN | LOTC | RUA1 | RCL | TCLE | TOCD  | PRBSD |

| SYMBOL               | POSITION | DESCRIPTION  |
|----------------------|----------|--|
| LUP<br>(latched)     | SR.7     | <b>Loop Up Code Detected.</b> Set when the loop up code defined in registers RUPCD1 and RUPCD2 is being received. See Section 6 for details.     |
| LDN<br>(latched)     | SR.6     | <b>Loop Down Code Detected.</b> Set when the loop down code defined in registers RDNCD1 and RDNCD2 is being received. See Section 6 for details. |
| LOTC<br>(real time)  | SR.5     | <b>Loss of Transmit Clock.</b> Set when the TCLK pin has not transitioned for 5μsec (±2μsec). Will force the LOTC pin high.                      |
| RUA1<br>(latched)    | SR.4     | <b>Receive Unframed All Ones.</b> Set when an unframed all ones code is received at RRING and RTIP. See Table 7-1 for details.                   |
| RCL<br>(latched)     | SR.3     | <b>Receive Carrier Loss.</b> Set when a receive carrier loss condition exists at RRING and RTIP. See Table 7-1 for details.                      |
| TCLE<br>(real time)  | SR.2     | <b>Transmit Current Limit Exceeded.</b> Set when the 50 mA (rms) current limiter is activated whether the current limiter is enabled or not.     |
| TOCD<br>(real time)  | SR.1     | <b>Transmit Open Circuit Detect.</b> Set when the device detects that the TTIP and TRING outputs are open circuited.                             |
| PRBSD<br>(real time) | SR.0     | <b>PRBS Detect.</b> Set when the receive-side detects a $2^{15} - 1$ (E1) or a $2^{20} - 1$ (T1) Pseudo Random Bit Sequence (PRBS).              |

**IMR (07H): INTERRUPT MASK REGISTER****(MSB)****(LSB)**

|     |     |      |      |     |      |      |       |
|-----|-----|------|------|-----|------|------|-------|
| LUP | LDN | LOTC | RUA1 | RCL | TCLE | TOCD | PRBSD |
|-----|-----|------|------|-----|------|------|-------|

| SYMBOL | POSITION | DESCRIPTION  |
|--------|----------|--|
| LUP    | IMR.7    | <b>Loop Up Code Detected.</b><br>0 = interrupt masked<br>1 = interrupt enabled             |
| LDN    | IMR.6    | <b>Loop Down Code Detected.</b><br>0 = interrupt masked<br>1 = interrupt enabled           |
| LOTC   | IMR.5    | <b>Loss of Transmit Clock.</b><br>0 = interrupt masked<br>1 = interrupt enabled            |
| RUA1   | IMR.4    | <b>Receive Unframed All Ones.</b><br>0 = interrupt masked<br>1 = interrupt enabled         |
| RCL    | IMR.3    | <b>Receive Carrier Loss.</b><br>0 = interrupt masked<br>1 = interrupt enabled              |
| TCLE   | IMR.2    | <b>Transmit Current Limiter Exceeded.</b><br>0 = interrupt masked<br>1 = interrupt enabled |
| TOCD   | IMR.1    | <b>Transmit Open Circuit Detect.</b><br>0 = interrupt masked<br>1 = interrupt enabled      |
| PRBSD  | IMR.0    | <b>PRBS Detection.</b><br>0 = interrupt masked<br>1 = interrupt enabled                    |

**RIR1 (08H): RECEIVE INFORMATION REGISTER 1**

| (MSB) |      |     |      |       |      | (LSB) |     |
|-------|------|-----|------|-------|------|-------|-----|
| ZD    | 16ZD | HBD | RCLC | RUA1C | JALT | n/a   | n/a |

| SYMBOL             | POSITION | DESCRIPTION  |
|--------------------|----------|--|
| ZD<br>(latched)    | RIR1.7   | <b>Zero Detect.</b> Set when a string of at least four (ETS = 0) or eight (ETS = 1) consecutive zeros (regardless of the length of the string) have been received. Will be cleared when read.  |
| 16ZD<br>(latched)  | RIR1.6   | <b>Sixteen Zero Detect.</b> Set when at least 16 consecutive zeros (regardless of the length of the string) have been received. Will be cleared when read.   |
| HBD<br>(latched)   | RIR1.5   | <b>HDB3/B8ZS Word Detect.</b> Set when an HDB3 (ETS = 0) or B8ZS (ETS = 1) code word is detected independent of whether the receive HDB3/B8ZS mode (CCR4.6) is enabled. Will be cleared when read. Useful for automatically setting the line coding. |
| RCLC<br>(latched)  | RIR1.4   | <b>Receive Carrier Loss Clear.</b> Set when the RCL alarm has met the clear criteria defined in Table 7-1. Will be cleared when read.  |
| RUA1C<br>(latched) | RIR1.3   | <b>Receive Unframed All Ones Clear.</b> Set when the unframed all ones signal is no longer detected. Will be cleared when read. See Table 7-1.   |
| JALT<br>(latched)  | RIR1.2   | <b>Jitter Attenuator Limit Trip.</b> Set when the jitter attenuator FIFO reaches to within 4 bits of its useful limit. Will be cleared when read. Useful for debugging jitter attenuation operation.   |
| N/A                | RIR1.1   | <b>Not Assigned.</b> Could be any value when read.   |
| N/A                | RIR1.0   | <b>Not Assigned.</b> Could be any value when read.   |

**RIR2 (09H): RECEIVE INFORMATION REGISTER 2****(MSB)****(LSB)**

|     |     |     |     |     |     |      |     |
|-----|-----|-----|-----|-----|-----|------|-----|
| RL3 | RL2 | RL1 | RL0 | N/A | N/A | ARLB | SEC |
|-----|-----|-----|-----|-----|-----|------|-----|

| SYMBOL              | POSITION | DESCRIPTION   |
|---------------------|----------|---|
| RL3<br>(real time)  | RIR2.7   | <b>Receive Level Bit 3.</b> See Table 7-2.  |
| RL2<br>(real time)  | RIR2.6   | <b>Receive Level Bit 2.</b> See Table 7-2.  |
| RL1<br>(real time)  | RIR2.5   | <b>Receive Level Bit 1.</b> See Table 7-2.  |
| RL0<br>(real time)  | RIR2.4   | <b>Receive Level Bit 0.</b> See Table 7-2.  |
| N/A                 | RIR2.3   | <b>Not Assigned.</b> Could be any value when read.  |
| N/A                 | RIR2.2   | <b>Not Assigned.</b> Could be any value when read.  |
| ARLB<br>(real time) | RIR2.1   | <b>Automatic Remote LoopBack Detected.</b> This bit will be set to a one when the automatic Remote Loopback (RLB) circuitry has detected the presence of a loop up code for 5 seconds. It will remain set until the automatic RLB circuitry has detected the loop down code for 5 seconds. See Section 6 for more details. This bit will be forced low when the automatic RLB circuitry is disabled (CCR6.5 = 0). |
| SEC<br>(latched)    | RIR2.0   | <b>One-Second Timer.</b> This bit will be set to a one on one-second boundaries as timed by the device based on the RCLK. It will be cleared when read.   |

**RECEIVE LEVEL INDICATION Table 7-2**

| RL3 | RL2 | RL1 | RL0 | Receive Level (dB) |
|-----|-----|-----|-----|--------------------|
| 0   | 0   | 0   | 0   | Greater than -2.5  |
| 0   | 0   | 0   | 1   | -2.5 to -5.0       |
| 0   | 0   | 1   | 0   | -5.0 to -7.5       |
| 0   | 0   | 1   | 1   | -7.5 to -10.0      |
| 0   | 1   | 0   | 0   | -10.0 to -12.5     |
| 0   | 1   | 0   | 1   | -12.5 to -15.0     |
| 0   | 1   | 1   | 0   | -15.0 to -17.5     |
| 0   | 1   | 1   | 1   | -20.0 to -22.5     |
| 1   | 0   | 0   | 0   | -22.5 to -25.0     |
| 1   | 0   | 0   | 1   | -25.0 to -27.5     |
| 1   | 0   | 1   | 0   | -27.5 to -30.0     |
| 1   | 0   | 1   | 1   | -30.0 to -32.5     |
| 1   | 1   | 0   | 0   | -32.5 to -35.0     |
| 1   | 1   | 0   | 1   | -35.0 to -37.5     |
| 1   | 1   | 1   | 0   | -37.5 to -40.0     |
| 1   | 1   | 1   | 1   | -40.0 to -42.5     |

## 8. DIAGNOSTICS

### 8.1 In-Band Loop Code Generation and Detection

The DS21348 has the ability to generate and detect a repeating bit pattern that is from one to eight or sixteen bits in length. To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition (TCD1 and TCD2) registers and select the proper length of the pattern by setting the TC0 and TC1 bits in the In-Band Code Control (IBCC) register. When generating a 1, 2, 4, 8, or 16 bit pattern both the transmit code registers (TCD1 and TCD2) must be filled with the proper code. Generation of a 1, 3, 5, or 7-bit pattern only requires TCD1 to be filled. Once this is accomplished, the pattern will be transmitted as long as the TLCE control bit (CCR3.3) is enabled. As an example, if the user wished to transmit the standard “loop up” code for Channel Service Units which is a repeating pattern of ...10000100001... then 80h would be loaded into TCD1 and the length would set using TC1 and TC0 in the IBCC register to 5 bits.

The DS21348 can detect two separate repeating patterns to allow for both a “loop up” code and a “loop down” code to be detected. The user will program the codes to be detected in the Receive Up Code Definition (RUPCD1 and RUPCD2) registers and the Receive Down Code Definition (RDNCD1 and RDNCD2) registers and the length of each pattern will be selected via the IBCC register. The DS21348 will detect repeating pattern codes with bit error rates as high as  $1 \times 10^{-2}$ . The code detector has a nominal integration period of 48ms, hence, after about 48ms of receiving either code, the proper status bit (LUP at SR.7 and LDN at SR.6) will be set to a one. Normally codes are sent for a period of 5 seconds. It is recommended that the software poll the DS21348 every 100ms to 1000ms until 5 seconds has elapsed to insure that the code is continuously present.

### IBCC (0AH): IN-BAND CODE CONTROL REGISTER

| (MSB) |     |      |      |      |      |      |      | (LSB) |
|-------|-----|------|------|------|------|------|------|-------|
| TC1   | TC0 | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |       |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| TC1    | IBCC.7   | <b>Transmit Code Length Definition Bit 1.</b> See Table 8-1     |
| TC0    | IBCC.6   | <b>Transmit Code Length Definition Bit 0.</b> See Table 8-1     |
| RUP2   | IBCC.5   | <b>Receive Up Code Length Definition Bit 2.</b> See Table 8-2   |
| RUP1   | IBCC.4   | <b>Receive Up Code Length Definition Bit 1.</b> See Table 8-2   |
| RUP0   | IBCC.3   | <b>Receive Up Code Length Definition Bit 0.</b> See Table 8-2   |
| RDN2   | IBCC.2   | <b>Receive Down Code Length Definition Bit 2.</b> See Table 8-2 |
| RDN1   | IBCC.1   | <b>Receive Down Code Length Definition Bit 1.</b> See Table 8-2 |
| RDN0   | IBCC.0   | <b>Receive Down Code Length Definition Bit 0.</b> See Table 8-2 |

**TRANSMIT CODE LENGTH Table 8-1**

| TC1 | TC0 | LENGTH SELECTED                     |
|-----|-----|-------------------------------------|
| 0   | 0   | 5 bits                              |
| 0   | 1   | 6 bits/3 bits                       |
| 1   | 0   | 7 bits                              |
| 1   | 1   | 16 bits/8 bits/4 bits/2 bits/1 bits |

**RECEIVE CODE LENGTH Table 8-2**

| RUP2/ RDN2 | RUP1/ RDN1 | RUP0/ RDN0 | LENGTH SELECTED |
|------------|------------|------------|-----------------|
| 0          | 0          | 0          | 1 bits          |
| 0          | 0          | 1          | 2 bits          |
| 0          | 1          | 0          | 3 bits          |
| 0          | 1          | 1          | 4 bits          |
| 1          | 0          | 0          | 5 bits          |
| 1          | 0          | 1          | 6 bits          |
| 1          | 1          | 0          | 7 bits          |
| 1          | 1          | 1          | 16 bits/8 bits  |

**TCD1 (0BH): TRANSMIT CODE DEFINITION REGISTER 1**

(MSB)

(LSB)

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|----|----|----|----|----|----|----|----|

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| C7     | TCD1.7   | <b>Transmit Code Definition Bit 7.</b> First bit of the repeating pattern.                          |
| C6     | TCD1.6   | <b>Transmit Code Definition Bit 6.</b>  |
| C5     | TCD1.5   | <b>Transmit Code Definition Bit 5.</b>  |
| C4     | TCD1.4   | <b>Transmit Code Definition Bit 4.</b>  |
| C3     | TCD1.3   | <b>Transmit Code Definition Bit 3.</b>  |
| C2     | TCD1.2   | <b>Transmit Code Definition Bit 2.</b> A Don't Care if a 5-bit length is selected.                  |
| C1     | TCD1.1   | <b>Transmit Code Definition Bit 1.</b> A Don't Care if a 5-bit or 6-bit length is selected.         |
| C0     | TCD1.0   | <b>Transmit Code Definition Bit 0.</b> A Don't Care if a 5-bit, 6-bit, or 7-bit length is selected. |



**TCD2 (0CH): TRANSMIT CODE DEFINITION REGISTER 2**

| (MSB) |     |     |     |     |     |    | (LSB) |
|-------|-----|-----|-----|-----|-----|----|-------|
| C15   | C14 | C13 | C12 | C11 | C10 | C9 | C8    |

| SYMBOL | POSITION | DESCRIPTION                            |
|--------|----------|--|
| C15    | TCD2.7   | <b>Transmit Code Definition Bit 15</b> |
| C14    | TCD2.6   | <b>Transmit Code Definition Bit 14</b> |
| C13    | TCD2.5   | <b>Transmit Code Definition Bit 13</b> |
| C12    | TCD2.4   | <b>Transmit Code Definition Bit 12</b> |
| C11    | TCD2.3   | <b>Transmit Code Definition Bit 11</b> |
| C10    | TCD2.2   | <b>Transmit Code Definition Bit 10</b> |
| C9     | TCD2.1   | <b>Transmit Code Definition Bit 9</b>  |
| C8     | TCD2.0   | <b>Transmit Code Definition Bit 8</b>  |

**RUPCD1 (0DH): RECEIVE UP CODE DEFINITION REGISTER 1**

| (MSB) |    |    |    |    |    |    | (LSB) |
|-------|----|----|----|----|----|----|-------|
| C7    | C6 | C5 | C4 | C3 | C2 | C1 | C0    |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| C7     | RUPCD1.7 | <b>Receive Up Code Definition Bit 7.</b> First bit of the repeating pattern.                  |
| C6     | RUPCD1.6 | <b>Receive Up Code Definition Bit 6.</b> A Don't Care if a 1-bit length is selected.          |
| C5     | RUPCD1.5 | <b>Receive Up Code Definition Bit 5.</b> A Don't Care if a 1-bit or 2-bit length is selected. |
| C4     | RUPCD1.4 | <b>Receive Up Code Definition Bit 4.</b> A Don't Care if a 1-bit to 3-bit length is selected. |
| C3     | RUPCD1.3 | <b>Receive Up Code Definition Bit 3.</b> A Don't Care if a 1-bit to 4-bit length is selected. |
| C2     | RUPCD1.2 | <b>Receive Up Code Definition Bit 2.</b> A Don't Care if a 1-bit to 5-bit length is selected. |
| C1     | RUPCD1.1 | <b>Receive Up Code Definition Bit 1.</b> A Don't Care if a 1-bit to 6-bit length is selected. |
| C0     | RUPCD1.0 | <b>Receive Up Code Definition Bit 0.</b> A Don't Care if a 1-bit to 7-bit length is selected. |

**RUPCD2 (0EH): RECEIVE UP CODE DEFINITION REGISTER 2**

| (MSB) |     |     |     |     |     |    | (LSB) |
|-------|-----|-----|-----|-----|-----|----|-------|
| C15   | C14 | C13 | C12 | C11 | C10 | C9 | C8    |

| SYMBOL | POSITION | DESCRIPTION                              |
|--------|----------|--|
| C15    | RUPCD2.7 | <b>Receive Up Code Definition Bit 15</b> |
| C14    | RUPCD2.6 | <b>Receive Up Code Definition Bit 14</b> |
| C13    | RUPCD2.5 | <b>Receive Up Code Definition Bit 13</b> |
| C12    | RUPCD2.4 | <b>Receive Up Code Definition Bit 12</b> |
| C11    | RUPCD2.3 | <b>Receive Up Code Definition Bit 11</b> |
| C10    | RUPCD2.2 | <b>Receive Up Code Definition Bit 10</b> |
| C9     | RUPCD2.1 | <b>Receive Up Code Definition Bit 9</b>  |
| C8     | RUPCD2.0 | <b>Receive Up Code Definition Bit 8</b>  |

**RDNCD1 (0FH): RECEIVE DOWN CODE DEFINITION REGISTER 1**

| (MSB) |    |    |    |    |    |    | (LSB) |
|-------|----|----|----|----|----|----|-------|
| C7    | C6 | C5 | C4 | C3 | C2 | C1 | C0    |

| SYMBOL | POSITION | DESCRIPTION   |
|--------|----------|---|
| C7     | RDNCD1.7 | <b>Receive Down Code Definition Bit 7.</b> First bit of the repeating pattern.                  |
| C6     | RDNCD1.6 | <b>Receive Down Code Definition Bit 6.</b> A Don't Care if a 1-bit length is selected.          |
| C5     | RDNCD1.5 | <b>Receive Down Code Definition Bit 5.</b> A Don't Care if a 1-bit or 2-bit length is selected. |
| C4     | RDNCD1.4 | <b>Receive Down Code Definition Bit 4.</b> A Don't Care if a 1-bit to 3-bit length is selected. |
| C3     | RDNCD1.3 | <b>Receive Down Code Definition Bit 3.</b> A Don't Care if a 1-bit to 4-bit length is selected. |
| C2     | RDNCD1.2 | <b>Receive Down Code Definition Bit 2.</b> A Don't Care if a 1-bit to 5-bit length is selected. |
| C1     | RDNCD1.1 | <b>Receive Down Code Definition Bit 1.</b> A Don't Care if a 1-bit to 6-bit length is selected. |
| C0     | RDNCD1.0 | <b>Receive Down Code Definition Bit 0.</b> A Don't Care if a 1-bit to 7-bit length is selected. |

**RDNCD2 (10H): RECEIVE DOWN CODE DEFINITION REGISTER 2**

| (MSB) |     |     |     |     |     | (LSB) |    |
|-------|-----|-----|-----|-----|-----|-------|----|
| C15   | C14 | C13 | C12 | C11 | C10 | C9    | C8 |

| SYMBOL | POSITION | DESCRIPTION                         |
|--------|----------|-------------------------------------|
| C15    | RDNCD2.7 | Receive Down Code Definition Bit 15 |
| C14    | RDNCD2.6 | Receive Down Code Definition Bit 14 |
| C13    | RDNCD2.5 | Receive Down Code Definition Bit 13 |
| C12    | RDNCD2.4 | Receive Down Code Definition Bit 12 |
| C11    | RDNCD2.3 | Receive Down Code Definition Bit 11 |
| C10    | RDNCD2.2 | Receive Down Code Definition Bit 10 |
| C9     | RDNCD2.1 | Receive Down Code Definition Bit 9  |
| C8     | RDNCD2.0 | Receive Down Code Definition Bit 8  |

## 8.2 Loopbacks

### 8.2.1 Remote Loopback (RLB)

When RLB (CCR6.6) is enabled, the DS21348 is placed into remote loopback. In this loopback, data from the clock/data recovery state machine will be looped back to the transmit path passing through the jitter attenuator if it is enabled. The data at the RPOS and RNEG pins will be valid while data presented at TPOS and TNEG will be ignored. See for details.

If the Automatic Remote Loop Back Enable (CCR6.5) is set to a one, the DS21348 will automatically go into remote loop back when it detects the loop up code programmed in the Receive Up Code Definition Registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds. When the DS21348 detects the loop down code programmed in the Receive Loop Down Code Definition registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds, the DS21348 will come out of remote loop back. The ARLB can also be disabled by setting ARLBE to a zero.

### 8.2.2 Local Loopback (LLB)

When LLB (CCR6.7) is set to a one, the DS21348 is placed into Local Loopback. In this loopback, data on the transmit-side will continue to be transmitted as normal. TCLK and TPOS/TNEG will pass through the jitter attenuator (if enabled) and be output at RCLK and RPOS/RNEG. Incoming data from the line at RTIP and RRING will be ignored. If Transmit Unframed All Ones (CCR3.7) is set to a one while in LLB, TTIP and TRING will transmit all ones while TCLK and TPOS/TNEG will be looped back to RCLK and RPOS/RNEG. See for more details.

### 8.2.3 Analog Loopback (LLB)

Setting ALB (CCR6.4) to a one puts the DS21348 in Analog Loopback. Signals at TTIP and TRING will be internally connected to RTIP and RRING. The incoming signals at RTIP and RRING will be ignored. The signals at TTIP and TRING will be transmitted as normal. See for more details.

### 8.2.4 Dual Loopback (DLB)

Setting both CCR6.7 and CCR6.6 to a one, LLB and RLB respectively, puts the DS21348 into Dual Loopback operation. The TCLK and TPOS/TNEG signals will be looped back through the jitter attenuator (if enabled) and output at RCLK and RPOS/RNEG. Clock and data recovered from RTIP and RRING will be looped back to the transmit-side and output at TTIP and TRING. This mode of operation is not available when implementing hardware operation. See for more details.

## 8.3 PRBS Generation and Detection

Setting TPRBSE (CCR3.4) = 1 enables the DS21348 to transmit a  $2^{15} - 1$  (E1) or a  $2^{20} - 1$  (T1) Pseudo Random Bit Sequence (PRBS) depending on the ETS bit setting in CCR1.7. The receive-side of the DS21348 will always search for these PRBS patterns independent of CCR3.4. The PRBS Bit Error Output (PBEO) will remain high until the receiver has synchronized to one of the two patterns (64 bits received without an error) at which time PBEO will go low and the PRBSD bit in the Status Register (SR) will be set. Once synchronized, any bit errors received will cause a positive going pulse at PBEO, synchronous with RCLK. This output can be used with external circuitry to keep track of bit error rates during the PRBS testing. Setting CCR6.0 (ECSR) = 1 will allow the PRBS errors to be accumulated in the 16-bit counter in registers ECR1 and ECR2. The PRBS synchronizer will remain in sync until it experiences 6 bit errors or more within a 64 bit span. Both PRBS patterns comply with the ITU-T O.151 specifications.

## 8.4 Error Counter

Error Count Register 1 (ECR1) is the most significant word and ECR2 is the least significant word of a user selectable 16-bit counter that records incoming errors including BiPolar Violations (BPV), Code Violations (CV), Excessive Zero violations (EXZ) and/or PRBS Errors. See Table 8-3 and Table 8-4 and Figure 3-2 for details.

### DEFINITION OF RECEIVED ERRORS Table 8-3

| ERROR | E1 OR T1 | DEFINITION OF RECEIVED ERRORS  |
|-------|----------|--|
| BPV   | E1/T1    | Two consecutive marks with the same polarity. Will ignore BPVs due to HDB3 and B8ZS zero suppression when CCR2.3 = 0. Typically used with AMI coding (CCR2.3 = 1). ITU-T O.161.                                      |
| CV    | E1       | When HDB3 is enabled (CCR2.3 = 0) and the receiver detects two consecutive BPVs with the same polarity. ITU-T O.161.   |
| EXZ   | E1       | When four or more consecutive zeros are detected.  |
| EXZ   | T1       | When receiving AMI coded signals (CCR2.3 = 1), detection of 16 or more zeros or a BPV. ANSI T1.403 1999.<br>When receiving B8ZS coded signals (CCR2.3 = 0), detection of 8 or more zeros or a BPV. ANSI T1.403 1999. |
| PRBS  | E1/T1    | A bit error in a received PRBS pattern. See section 8.3 for details. ITU-T O.151.  |

**FUNCTION OF ECRS BITS AND RNEG PIN Table 8-4**

| E1 or T1<br>(CCR1.7) | ECRS2<br>(CCR6.2) | ECRS1<br>(CCR6.1) | ECRS0<br>(CCR6.0) | RHBE<br>(CCR2.3) | FUNCTION OF ECR<br>COUNTERS/RNEG <sup>1</sup> |
|----------------------|-------------------|-------------------|-------------------|------------------|---|
| 0                    | 0                 | 0                 | 0                 | X                | CVs   |
| 0                    | 0                 | 0                 | 1                 | X                | BPVs (HDB3 code words not counted)            |
| 0                    | 0                 | 1                 | 0                 | X                | CVs + EXZs                                    |
| 0                    | 0                 | 1                 | 1                 | X                | BPVs + EXZs                                   |
| 1                    | 0                 | X                 | 0                 | 0                | BPVs (B8ZS code words not counted)            |
| 1                    | 0                 | X                 | 1                 | 0                | BPVs + 8 EXZs                                 |
| 1                    | 0                 | X                 | 0                 | 1                | BPVs  |
| 1                    | 0                 | X                 | 1                 | 1                | BPVs + 16 EXZs                                |
| X                    | 1                 | X                 | X                 | X                | PRBS Errors <sup>2</sup>                      |

**NOTES:**

1. RNEG outputs error data only when in NRZ mode (CCR1.6 = 1)
2. PRBS errors will always be output at PBE0 independent of ECR control bits and NRZ mode and will not be present at RNEG.

**8.4.1 Error Counter Update**

A transition of the ECUE (CCR1.4) control bit from 0 to 1 will update the ECR registers with the current values and reset the counters. ECUE must be set back to zero and another 0 to 1 transition must occur for subsequent reads/resets of the ECR registers. Note that the DS21348 can report errors at RNEG when in NRZ mode (CCR1.6 = 1) by outputting a pulse for each error occurrence. The counter saturates at 65,535 and will not rollover.

**ECR1 (11H): UPPER ERROR COUNT REGISTER 1****ECR2 (12H): LOWER ERROR COUNT REGISTER 2**

| (MSB) |     |     |     | (LSB) |     |    |    |      |
|-------|-----|-----|-----|-------|-----|----|----|------|
| E15   | E14 | E13 | E12 | E11   | E10 | E9 | E8 | ECR1 |
| E7    | E6  | E5  | E4  | E3    | E2  | E1 | E0 | ECR2 |

| SYMBOL | POSITION | DESCRIPTION                          |
|--------|----------|--------------------------------------|
| E15    | ECR1.7   | <b>MSB of the 16-bit error count</b> |
| E0     | ECR2.0   | <b>LSB of the 16-bit error count</b> |

**8.5 Error Insertion**

When IBPV (CCR3.1) is transitioned from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert a BPV. IBPV must be cleared and set again for another BPV error insertion. See for details on the insertion of the BPV into the datastream.

When IBE (CCR3.0) is transitioned from a zero to a one, the device will insert a logic error. IBE must be cleared and set again for another logic error insertion. See for details on the insertion of the logic error into the datastream.

## 9. ANALOG INTERFACE

### 9.1 Receiver

The DS21348 contains a digital clock recovery system. The DS21348 couples to the receive E1 or T1 twisted pair (or coaxial cable in 75Ω E1 applications) via a 1:1 transformer. See Table 9-3 for transformer details. Figure 9-1, Figure 9-2, and Figure 9-3 along with Table 9-1 and Table 9-2 show the receive termination requirements. The DS21348 has the option of using internal termination resistors.

The DS21348 is designed to be fully software-selectable for E1 and T1 without the need to change any external resistors for the receive-side. The receive-side will allow the user to configure the DS21348 for 75Ω, 100Ω, or 120Ω receive termination by setting the RT1 (CCR5.1) and RT0 (CCR5.0) bits. When using the internal termination feature, the Rr resistors should be 60Ω each. See Figure 9-1 for details. If external termination is required, RT1 and RT0 should be set to 0 and both Rr resistors in Figure 9-1 will need to be 37.5Ω, 50Ω, or 60Ω each depending on the line impedance.

The resultant E1 or T1 clock derived from the 2.048/1.544 PLL (JACLK in ) is internally multiplied by 16 via another internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding performance to meet jitter tolerance specifications shown in Figure 9-.

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. When no signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK will be derived from the JACLK source. See . If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. See the Receive AC Timing Characteristics in Section 12 for more details.

The receive-side circuitry also contains a clock synthesizer which outputs a user configurable clock (up to 16.384MHz) synthesized to RCLK at BPCLK (pin 31). See Table 6-3 for details on output clock frequencies at BPCLK. In hardware mode, BPCLK defaults to a 16.384MHz output.

The DS21348 has a bypass mode for the receive side clock and data. This allows the BPCLK to be derived from RCLK after the jitter attenuator while the clock and data presented at RCLK, RPOS, and RNEG go unaltered. This is intended for applications where the receive side jitter attenuation will be done after the LIU. Setting RJAB (CCR6.3) to a logic 1 will enable the bypass. Be sure that the jitter attenuator is in the receive path (CCR4.3 = 0). See for details.

The DS21348 will report the signal strength at RTIP and RRING in 2.5dB increments via RL3-RL0 located in the Receive Information Register 2. This feature is helpful when trouble shooting line performance problems. See Table 7-2 for details.

Monitor applications in both E1 and T1 require various flat gain settings for the receive-side circuitry. The DS21348 can be programmed to support these applications via the Monitor Mode control bits MM1 and MM0. When the monitor modes are enabled, the receiver will tolerate normal line loss up to -6dB. See Table 6-4 for details.

## 9.2 Transmitter

The DS21348 uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms created by the DS21348 meet the latest ETSI, ITU, ANSI, and AT&T specifications. The user will select which waveform is to be generated by setting the ETS bit (CCR1.7) for E1 or T1 operation, then programming the L2/L1/L0 bits in Common Control Register 4 for the appropriate application. See Table 9-1 and Table 9-2 for the proper L2/L1/L0 settings.

A 2.048MHz or 1.544MHz TTL clock is required at TCLK for transmitting data at TPOS and TNEG. ITU specification G.703 requires an accuracy of  $\pm 50$ ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of  $\pm 32$ ppm for T1 interfaces. The clock can be sourced internally by RCLK or JACLK. See CCR1.2, CCR1.1, CCR1.0, and for details. Due to the nature of the design of the transmitter in the DS21348, very little jitter (less than 0.005 UIpp broadband from 10Hz to 100kHz) is added to the jitter present on TCLK. Also, the waveforms created are independent of the duty cycle of TCLK. The transmitter in the DS21348 couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) via a 1:2 step-up transformer. In order for the device to create the proper waveforms, the transformer used must meet the specifications listed in Table 9-3.

The DS21348 has automatic short-circuit limiter which limits the source current to 50mA (rms) into a 1 $\Omega$  load. This feature can be disabled by setting the SCLD bit (CCR2.5) = 1. When the current limiter is activated, TCLE (SR.2) will be set even if short circuit limiter is disabled. The TPD bit (CCR4.0) will power-down the transmit line driver and 3-state the TTIP and TRING pins. The DS21348 can also detect when the TTIP or TRING outputs are open circuited. When an open circuit is detected, TOCD (SR.1) will be set.

## 9.3 Jitter Attenuator

The DS21348 contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit (CCR4.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in . The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (CCR4.3). Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit (CCR4.1). In order for the jitter attenuator to operate properly, a 2.048MHz or 1.544MHz clock must be applied at MCLK. ITU specification G.703 requires an accuracy of  $\pm 50$ ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of  $\pm 32$ ppm for T1 interfaces. There is an onboard PLL for the jitter attenuator, which will convert the 2.048MHz clock to a 1.544 MHz rate for T1 applications. Setting JAMUX (CCR1.3) to a logic 0 bypasses this PLL. Onboard circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a smooth jitter free clock which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128 bits) or 28 UIpp (buffer depth is 32 bits), then the DS21348 will divide the internal nominal 32.768MHz (E1) or 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register 1 (RIR1).



## 9.4 G.703 Synchronization Signal

The DS21348 is capable of receiving a 2.048MHz square-wave synchronization clock as specified in section 10 of ITU G.703. In order to use the DS21348 in this mode, set the Receive Synchronization Clock Enable (CCR5.3) = 1. The DS21348 can also transmit the 2.048MHz square-wave synchronization clock as specified in section 10 of G.703. In order to transmit the 2.048 MHz clock, set the Transmit Synchronization Clock Enable (CCR5.2) = 1.

### LINE BUILD OUT SELECT FOR E1 IN REGISTER CCR4 (ETS = 0) Table 9-1

| L2 | L1 | L0 | V <sub>DD</sub> | APPLICATION              | N   | RETURN LOSS | R <sub>t</sub> |
|----|----|----|-----------------|--------------------------|-----|-------------|----------------|
| 0  | 0  | 0  | 3.3V            | 75Ω normal               | 1:2 | NM          | 0Ω             |
| 0  | 0  | 1  | 3.3V            | 120Ω normal              | 1:2 | NM          | 0Ω             |
| 1  | 0  | 0  | 3.3V            | 75Ω w/ high return loss  | 1:2 | 21dB        | 6.2Ω           |
| 1  | 0  | 1  | 3.3V            | 120Ω w/ high return loss | 1:2 | 21dB        | 11.6Ω          |

**Note:** See Figure 9-1, Figure 9-2, and Figure 9-3.

### LINE BUILD OUT SELECT FOR T1 IN REGISTER CCR4 (ETS = 1) Table 9-2

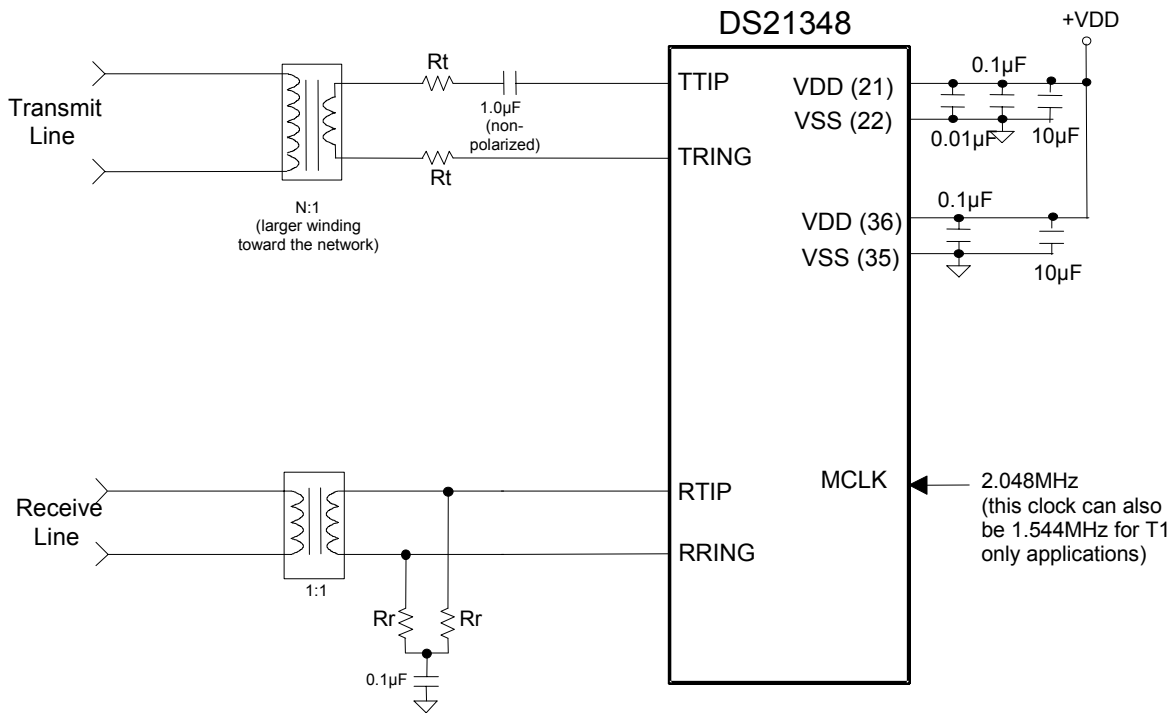
| L2 | L1 | L0 | V <sub>DD</sub> | APPLICATION                         | N   | RETURN LOSS | R <sub>t</sub> |
|----|----|----|-----------------|-------------------------------------|-----|-------------|----------------|
| 0  | 0  | 0  | 3.3V            | DSX-1 (0 to 133 feet) /<br>0 DB CSU | 1:2 | NM          | 0Ω             |
| 0  | 0  | 1  | 3.3V            | DSX-1 (133 to 266 feet)             | 1:2 | NM          | 0Ω             |
| 0  | 1  | 0  | 3.3V            | DSX-1 (266 to 399 feet)             | 1:2 | NM          | 0Ω             |
| 0  | 1  | 1  | 3.3V            | DSX-1 (399 to 533 feet)             | 1:2 | NM          | 0Ω             |
| 1  | 0  | 0  | 3.3V            | DSX-1 (533 to 655 feet)             | 1:2 | NM          | 0Ω             |
| 1  | 0  | 1  | 3.3V            | -7.5dB CSU                          | 1:2 | NM          | 0Ω             |
| 1  | 1  | 0  | 3.3V            | -15dB CSU                           | 1:2 | NM          | 0Ω             |
| 1  | 1  | 1  | 3.3V            | -22.5dB CSU                         | 1:2 | NM          | 0Ω             |

**Note:** See Figure 9-1, Figure 9-2, and Figure 9-3.

### TRANSFORMER SPECIFICATIONS FOR 3.3V OPERATION Table 9-3

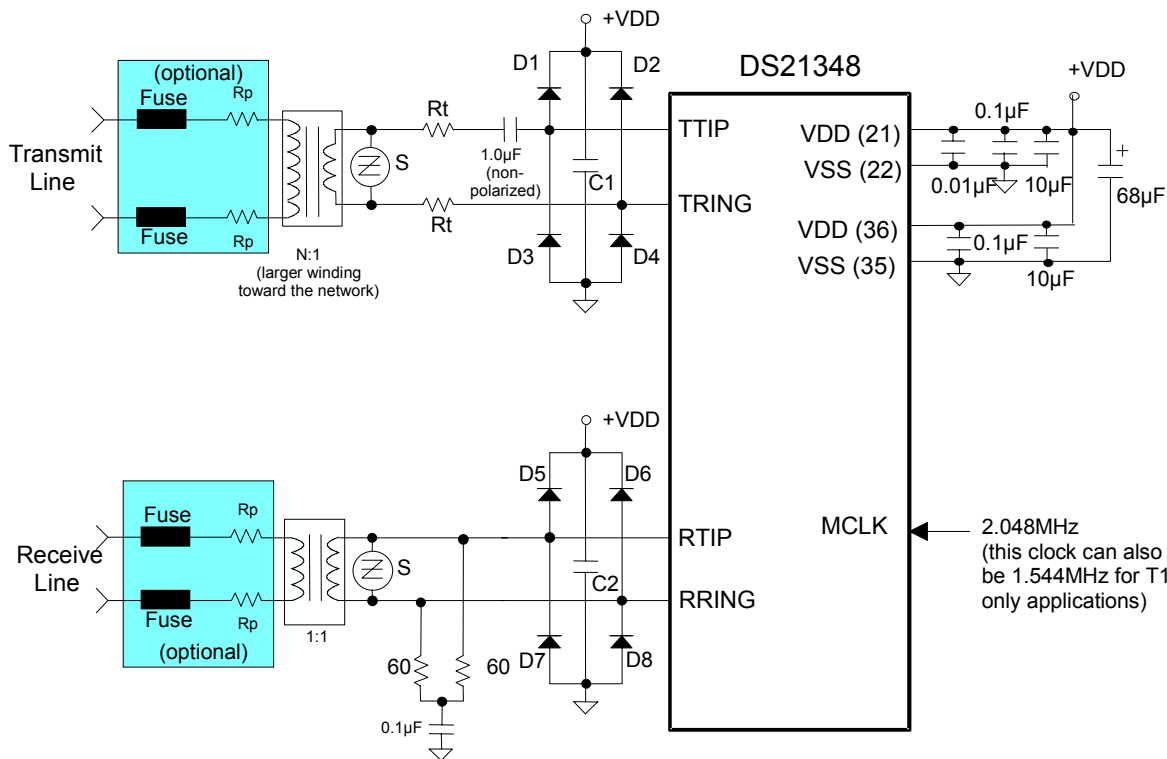
| SPECIFICATION  | RECOMMENDED VALUE                    |
|--|--------------------------------------|
| Turns Ratio 3.3V Applications  | 1:1 (receive) and 1:2 (transmit) ±2% |
| Primary Inductance   | 600μH minimum                        |
| Leakage Inductance   | 1.0μH maximum                        |
| Intertwining Capacitance   | 40pF maximum                         |
| Transmit Transformer DC Resistance<br>Primary (Device Side)<br>Secondary | 1.0Ω maximum<br>2.0Ω maximum         |
| Receive Transformer DC Resistance<br>Primary (Device Side)<br>Secondary  | 1.2Ω maximum<br>1.2Ω maximum         |



**BASIC INTERFACE** Figure 9-1**NOTES:**

- 1) All resistor values are  $\pm 1\%$ .
- 2) In E1 applications, the  $R_t$  resistors are used to increase the transmitter return loss (Table 9-1). No return loss is required for T1 applications.
- 3) The  $R_r$  resistors should be set to  $60\Omega$  each if the internal receive-side termination feature is enabled. When this feature is disabled,  $R_r = 37.5\Omega$  for  $75\Omega$  or  $60\Omega$  for  $120\Omega$  E1 systems, or  $50\Omega$  for  $100\Omega$  T1 lines.
- 4) See Table 9-1 and Table 9-2 for the appropriate transmit transformer turns ratio (N).

## Figure 9-2 PROTECTED INTERFACE USING INTERNAL RECEIVE TERMINATION

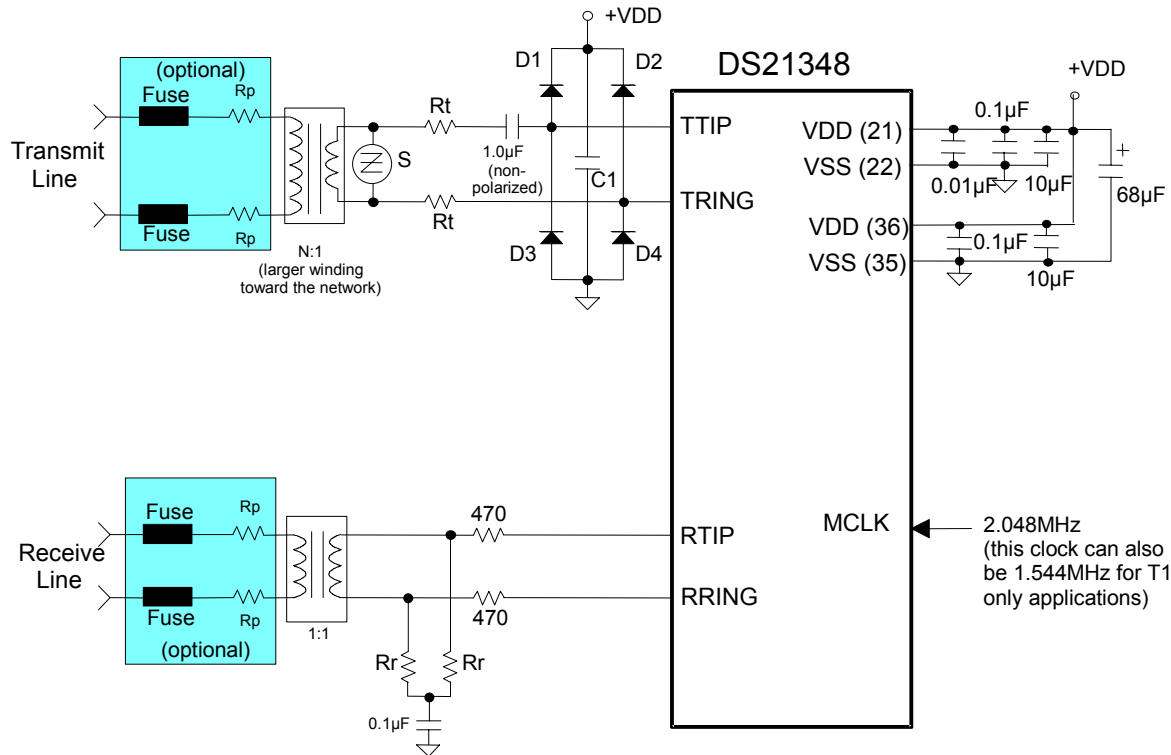


### NOTES:

1. All resistor values are  $\pm 1\%$ .
2.  $C1 = C2 = 0.1\mu\text{F}$ .
3. S is a 6V transient suppressor.
4. D1 to D8 are Schottky diodes.
5. The fuses are optional to prevent AC power line crosses from compromising the transformers.
6.  $R_p$  resistors exist to keep the Fuses from opening during a surge. If they are used, then the  $60\Omega$  receive termination resistance must be adjusted to match the line impedance.
7. The  $R_t$  resistors are used to increase the transmitter return loss (Table 9-1). No return loss is required for T1 applications.
8. The transmit transformer turns ratio (N) would be 1:2 for 3.3V operation.
9. The  $68\mu\text{F}$  is used to keep the local power plane potential within tolerance during a surge.

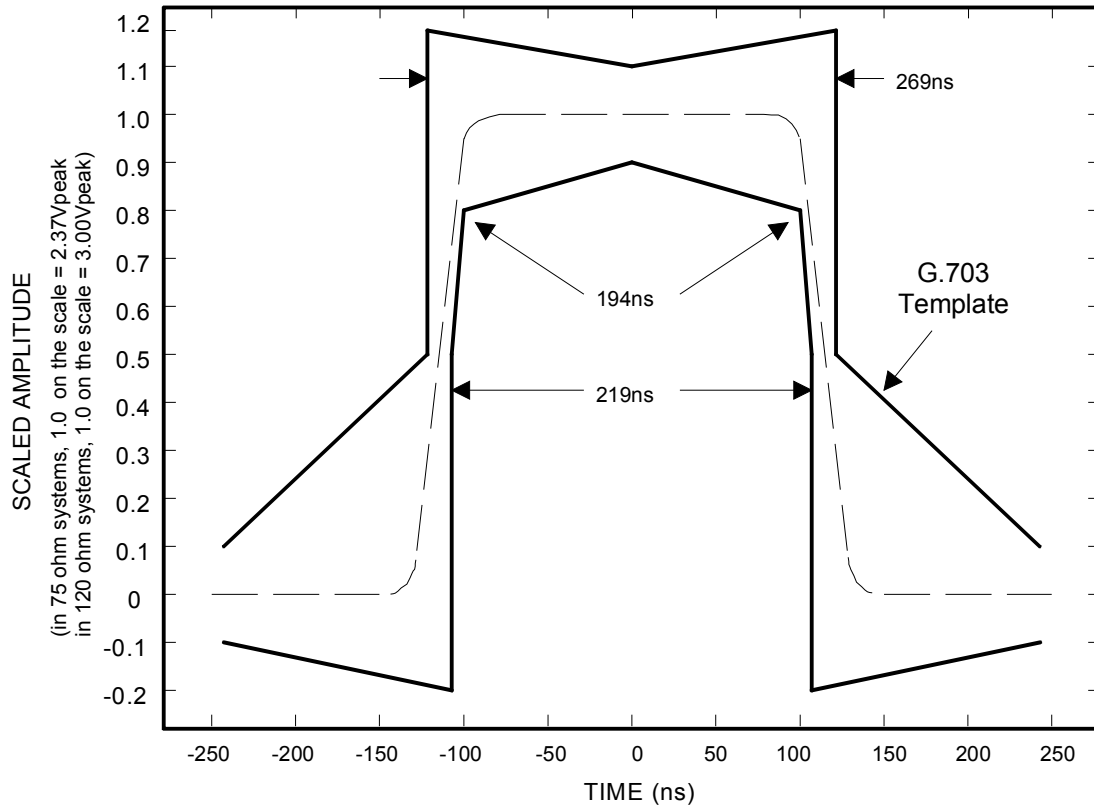
## PROTECTED INTERFACE USING EXTERNAL RECEIVE TERMINATION

Figure 9-3

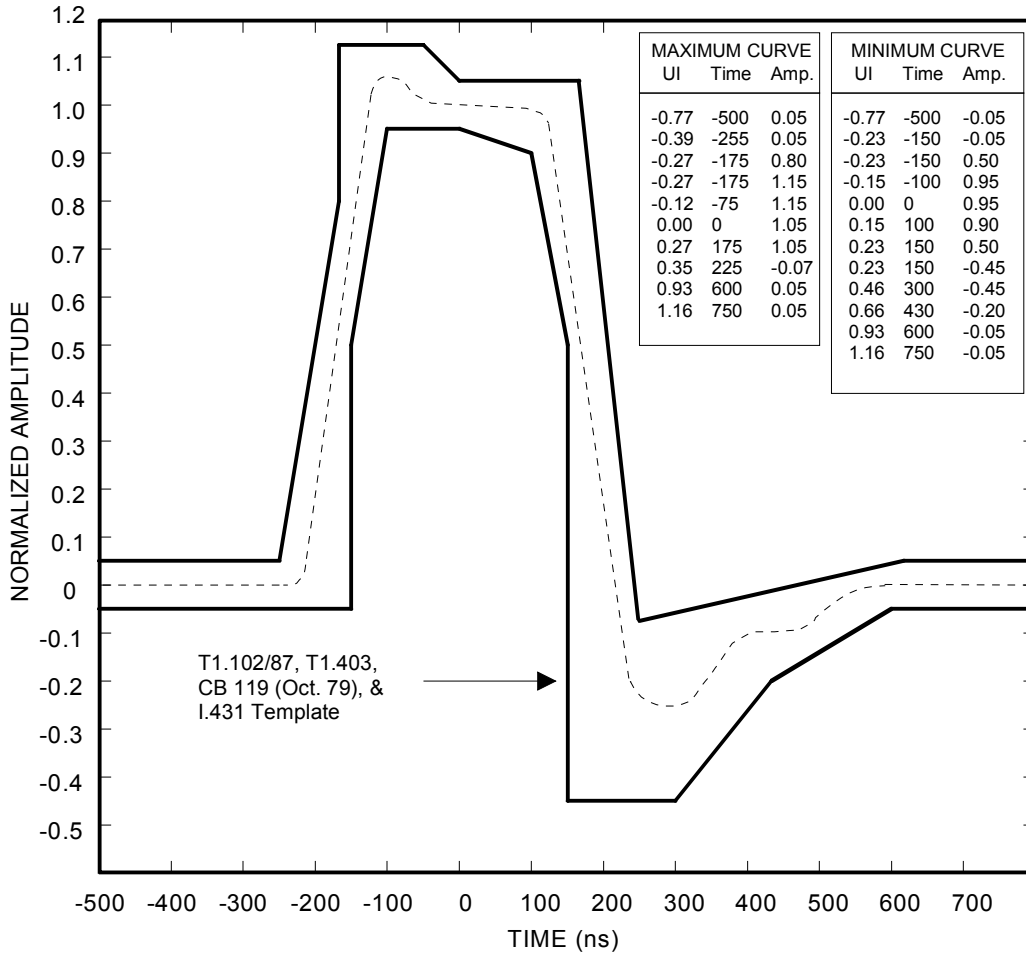


### NOTES:

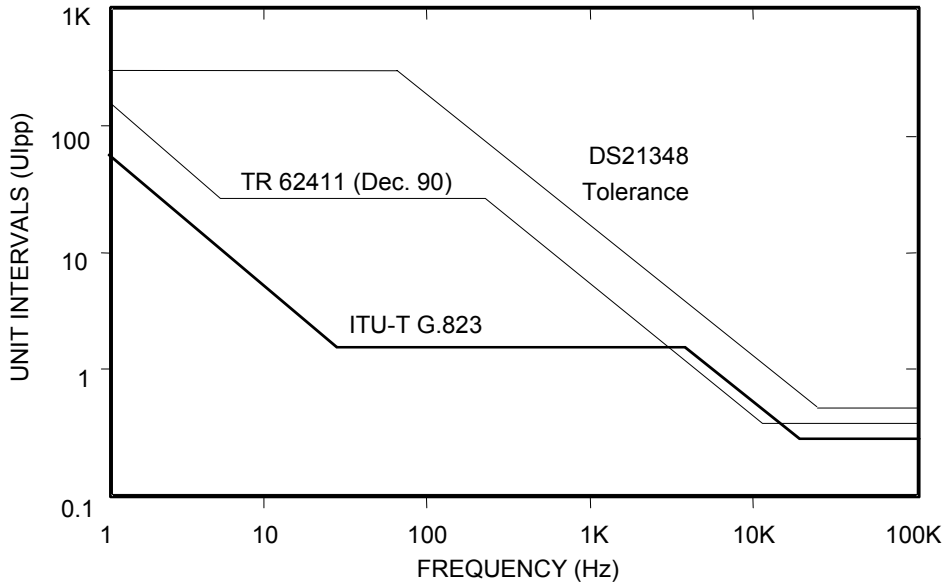
1. All resistor values are  $\pm 1\%$ .
2.  $C1 = 0.1 \mu\text{F}$ .
3. S is a 6V transient suppresser.
4. D1 to D4 are Schottky diodes.
5. The fuses are optional to prevent AC power line crosses from compromising the transformers.
6.  $R_p$  resistors exist to keep the Fuses from opening during a surge. If they are used, then  $R_r$  must be adjusted to match the line impedance.
7.  $R_r = 37.5 \Omega$  for 75  $\Omega$  or 60  $\Omega$  for 120  $\Omega$  E1 systems, or 50  $\Omega$  for 100  $\Omega$  T1 lines.
8. The  $R_t$  resistors are used to increase the transmitter return loss (Table 9-1). No return loss is required for T1 applications.
9. The transmit transformer turns ratio (N) would be 1:2 for 3.3V operation.
10. The 68  $\mu\text{F}$  is used to keep the local power plane potential within tolerance during a surge.

**E1 TRANSMIT PULSE TEMPLATE** Figure 9-4

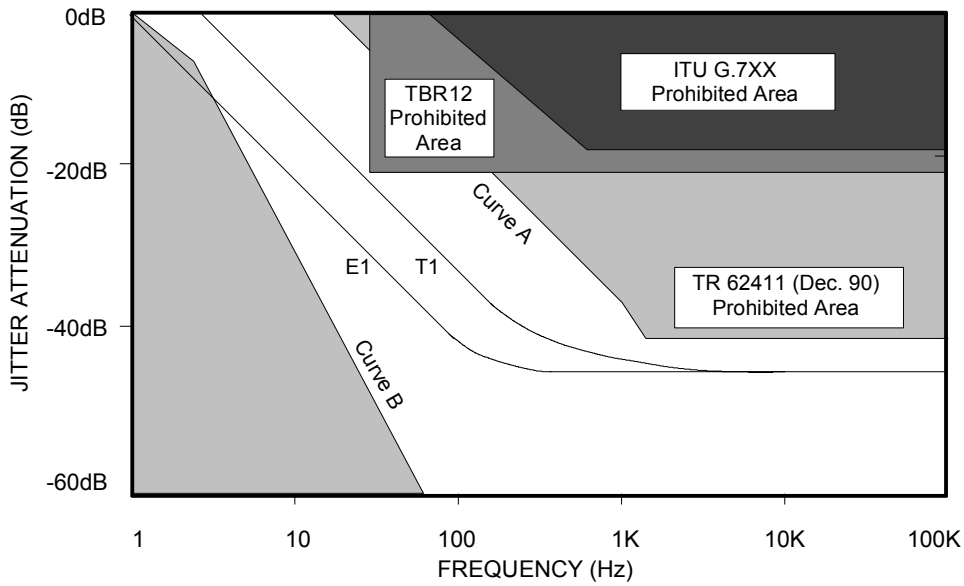
# T1 TRANSMIT PULSE TEMPLATE Figure 9-5



### JITTER TOLERANCE Figure 9-6



### JITTER ATTENUATION Figure 9-7



## 10. DS21Q348 QUAD LIU

The DS21Q348 is a quad version of the DS21348G utilizing CABGA on carrier packaging technology. The four LIUs are controlled via the parallel port mode. Serial and hardware modes are unavailable in this package.

**DS21Q348 PIN ASSIGNMENT Table 10-1**

| DS21Q348<br>PIN# | I/O | PARALLEL<br>PORT MODE      |
|------------------|-----|----------------------------|
| J1               | I   | Connect to V <sub>SS</sub> |
| K3               | I   | Connect to V <sub>SS</sub> |
| J2               | I   | RD*(DS*)                   |
| H1               | I   | WR*(R/W*)                  |
| K2               | I   | ALE(AS)                    |
| K1               | I/O | A4                         |
| L1               | I   | A3                         |
| H11              | I   | A2                         |
| H12              | I   | A1                         |
| G12              | I   | A0                         |
| J10              | I/O | D7/AD7                     |
| H10              | I/O | D6/AD6                     |
| G11              | I/O | D5/AD5                     |
| J9               | I/O | D4/AD4                     |
| E3               | I/O | D3/AD3                     |
| D4               | I/O | D2/AD2                     |
| F3               | I/O | D1/AD1                     |
| D5               | I/O | D0/AD0                     |
| G4               | I   | VSM                        |
| K9               | I/O | INT*                       |
| K7               | I   | TEST                       |
| L9               | I   | HRST*                      |
| J6               | I   | MCLK                       |
| L7               | I   | BIS0                       |
| M8               | I   | BIS1                       |
| M12              | I   | PBTS                       |
| J3               | I   | CS*1                       |
| D3               | I   | CS*2                       |
| D10              | I   | CS*3                       |
| K10              | I   | CS*4                       |
| K5               | O   | PBEO1                      |
| G3               | O   | PBEO2                      |
| E10              | O   | PBEO3                      |
| K8               | O   | PBEO4                      |
| L6               | O   | RCL/LOT1                   |
| D7               | O   | RCL/LOT2                   |
| F9               | O   | RCL/LOT3                   |

| <b>DS21Q348<br/>PIN#</b> | <b>I/O</b> | <b>PARALLEL<br/>PORT MODE</b> |
|--------------------------|------------|-------------------------------|
| J7                       | O          | RCL/LOT4                      |
| A1                       | I          | RTIP1                         |
| A4                       | I          | RTIP2                         |
| A7                       | I          | RTIP3                         |
| A10                      | I          | RTIP4                         |
| B2                       | I          | RRING1                        |
| B5                       | I          | RRING2                        |
| B8                       | I          | RRING3                        |
| B11                      | I          | RRING4                        |
| H4                       | O          | BPCLK1                        |
| D6                       | O          | BPCLK2                        |
| F10                      | O          | BPCLK3                        |
| L8                       | O          | BPCLK4                        |
| A2                       | O          | TTIP1                         |
| A5                       | O          | TTIP2                         |
| A8                       | O          | TTIP3                         |
| A11                      | O          | TTIP4                         |
| B3                       | O          | TRING1                        |
| B6                       | O          | TRING2                        |
| B9                       | O          | TRING3                        |
| B12                      | O          | TRING4                        |
| K4                       | O          | RPOS1                         |
| E1                       | O          | RPOS2                         |
| D11                      | O          | RPOS3                         |
| K11                      | O          | RPOS4                         |
| G2                       | O          | RNEG1                         |
| E2                       | O          | RNEG2                         |
| F11                      | O          | RNEG3                         |
| M10                      | O          | RNEG4                         |
| H3                       | O          | RCLK1                         |
| F1                       | O          | RCLK2                         |
| E11                      | O          | RCLK3                         |
| L11                      | O          | RCLK4                         |
| G1                       | I          | TPOS1                         |
| F2                       | I          | TPOS2                         |
| E12                      | I          | TPOS3                         |
| M11                      | I          | TPOS4                         |
| H2                       | I          | TNEG1                         |
| M1                       | I          | TNEG2                         |
| D12                      | I          | TNEG3                         |
| K12                      | I          | TNEG4                         |
| M2                       | I          | TCLK1                         |
| L2                       | I          | TCLK2                         |
| F12                      | I          | TCLK3                         |
| L12                      | I          | TCLK4                         |



| <b>DS21Q348<br/>PIN#</b> | <b>I/O</b> | <b>PARALLEL<br/>PORT MODE</b> |
|--------------------------|------------|-------------------------------|
| J5                       | -          | V <sub>DD1</sub>              |
| D2                       | -          | V <sub>DD2</sub>              |
| G9                       | -          | V <sub>DD3</sub>              |
| M9                       | -          | V <sub>DD4</sub>              |
| L5                       | -          | V <sub>DD1</sub>              |
| E4                       | -          | V <sub>DD2</sub>              |
| D8                       | -          | V <sub>DD3</sub>              |
| J8                       | -          | V <sub>DD4</sub>              |
| J4                       | -          | V <sub>SS1</sub>              |
| D1                       | -          | V <sub>SS2</sub>              |
| E9                       | -          | V <sub>SS3</sub>              |
| L10                      | -          | V <sub>SS4</sub>              |
| M4                       | -          | V <sub>SS1</sub>              |
| F4                       | -          | V <sub>SS2</sub>              |
| D9                       | -          | V <sub>SS3</sub>              |
| H9                       | -          | V <sub>SS4</sub>              |

**BGA 12 x 12 PIN LAYOUT** Figure 10-1

|          | 1                     | 2            | 3                     | 4          | 5          | 6             | 7             | 8          | 9             | 10         | 11         | 12         |
|----------|-----------------------|--------------|-----------------------|------------|------------|---------------|---------------|------------|---------------|------------|------------|------------|
| <b>A</b> | RTIP<br>1             | TTIP<br>1    | NC                    | RTIP<br>2  | TTIP<br>2  | NC            | RTIP<br>3     | TTIP<br>3  | NC            | RTIP<br>4  | TTIP<br>4  | NC         |
| <b>B</b> | NC                    | RRING<br>1   | TRING<br>1            | NC         | RRING<br>2 | TRING<br>2    | NC            | RRING<br>3 | TRING<br>3    | NC         | RRING<br>4 | TRING<br>4 |
| <b>C</b> | NC                    | NC           | NC                    | NC         | NC         | NC            | NC            | NC         | NC            | NC         | NC         | NC         |
| <b>D</b> | VSS<br>2              | VDD<br>2     | CS*<br>2              | D2/<br>AD2 | D0/<br>AD0 | BPCLK<br>2    | RCL/<br>LOTC2 | VDD<br>3   | VSS<br>3      | CS*<br>3   | RPOS<br>3  | TNEG<br>3  |
| <b>E</b> | RPOS<br>2             | RNEG<br>2    | D3/<br>AD3            | VDD<br>2   | NC         | NC            | NC            | NC         | VSS<br>3      | PEBO<br>3  | RCLK<br>3  | TPOS<br>3  |
| <b>F</b> | RCLK<br>2             | TPOS<br>2    | D1/<br>AD1            | VSS<br>2   | NC         | NC            | NC            | NC         | RCL/<br>LOTC3 | BPCLK<br>3 | RNEG<br>3  | TCLK<br>3  |
| <b>G</b> | TPOS<br>1             | RNEG<br>1    | PEBO<br>2             | VSM        | NC         | NC            | NC            | NC         | VDD<br>3      | NC         | D5/<br>AD5 | A0         |
| <b>H</b> | WR*<br>(R/W*)         | TNEG<br>1    | RCLK<br>1             | BPCLK<br>1 | NC         | NC            | NC            | NC         | VSS<br>4      | D6/<br>AD6 | A2         | A1         |
| <b>J</b> | <b>See<br/>Note 2</b> | RD*<br>(DS*) | CS*<br>1              | VSS<br>1   | VDD<br>1   | MCLK          | RCL/<br>LOTC4 | VDD<br>4   | D4/<br>AD4    | D7/<br>AD7 | NC         | NC         |
| <b>K</b> | A4                    | ALE<br>(AS)  | <b>See<br/>Note 2</b> | RPOS<br>1  | PEBO<br>1  | NC            | TEST          | PEBO<br>4  | INT*          | CS*<br>4   | RPOS<br>4  | TNEG<br>4  |
| <b>L</b> | A3                    | TCLK<br>2    | NC                    | NC         | VDD<br>1   | RCL/<br>LOTC1 | BIS0          | BPCLK<br>4 | HRST*         | VSS<br>4   | RCLK<br>4  | TCLK<br>4  |
| <b>M</b> | TNEG<br>2             | TCLK<br>1    | NC                    | VSS<br>1   | NC         | NC            | NC            | BIS1       | VDD<br>4      | RNEG<br>4  | TPOS<br>4  | PBTS       |

**NOTES:**

- 1) Shaded areas are signals common to all four devices
- 2) Connect to V<sub>SS</sub>.

## 11. DC CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS\*

|   |                              |
|---|------------------------------|
| Voltage Range on Any Pin Relative to Ground | -1.0V to +6.0V               |
| Operating Temperature Range for DS21348TN   | -40°C to +85°C               |
| Storage Temperature Range                   | See J-STD-020A specification |

\* This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

### RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

| PARAMETER                 | SYMBOL   | MIN   | TYP | MAX   | UNITS | NOTES |
|---------------------------|----------|-------|-----|-------|-------|-------|
| Logic 1                   | $V_{IH}$ | 2.0   |     | 5.5   | V     |       |
| Logic 0                   | $V_{IL}$ | -0.3  |     | +0.8  | V     |       |
| Supply for 3.3V Operation | $V_{DD}$ | 3.135 | 3.3 | 3.465 | V     | 1     |

### CAPACITANCE ( $T_A = +25^\circ\text{C}$ )

| PARAMETER          | SYMBOL    | MIN | TYP | MAX | UNITS | NOTES |
|--------------------|-----------|-----|-----|-----|-------|-------|
| Input Capacitance  | $C_{IN}$  |     | 5   |     | pF    |       |
| Output Capacitance | $C_{OUT}$ |     | 7   |     | pF    |       |

### DC CHARACTERISTICS (-40°C to +85°C; $V_{DD} = 3.3V \pm 5\%$ )

| PARAMETER             | SYMBOL   | MIN  | TYP | MAX  | UNITS         | NOTES |
|-----------------------|----------|------|-----|------|---------------|-------|
| Input Leakage         | $I_{IL}$ | -1.0 |     | +1.0 | $\mu\text{A}$ | 3     |
| Output Leakage        | $I_{LO}$ |      |     | 1.0  | $\mu\text{A}$ | 4     |
| Output Current (2.4V) | $I_{OH}$ | -1.0 |     |      | mA            |       |
| Output Current (0.4V) | $I_{OL}$ | +4.0 |     |      | mA            |       |
| Supply Current        | $I_{DD}$ | -    | 66  | 100  | mA            | 2, 5  |

### NOTES:

1. Applies to  $V_{DD}$ .
2.  $TCLK = MCLK = 2.048\text{MHz}$ .
3.  $0.0V < V_{IN} < V_{DD}$ .
4. Applied to INT\* when 3-stated.
5. Power dissipation with TTIP and TRING driving a  $30\Omega$  load, for an all one's data density.

**THERMAL CHARACTERISTICS OF DS21Q48 BGA PACKAGE**

| PARAMETER                               | MIN   | TYP      | MAX    | NOTES |
|---|-------|----------|--------|-------|
| Ambient Temperature                     | -40°C | -        | +85°C  | 1     |
| Junction Temperature                    | -     | -        | +125°C |       |
| Theta-JA ( $\theta_{JA}$ ) in Still Air | -     | +24°C/W  | -      | 2     |
| Theta-JC ( $\theta_{JC}$ ) in Still Air | -     | +4.1°C/W | -      | 3     |

**NOTES:**

- 1) The package is mounted on a four-layer JEDEC-standard test board.
- 2) Theta-JA ( $\theta_{JA}$ ) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC-standard test board.
- 3) While Theta-JC ( $\theta_{JC}$ ) is commonly used as the thermal parameter that provides a correlation between the junction temperature ( $T_j$ ) and the average temperature on top center of four of the chip-scale BGA packages ( $T_C$ ), the proper term is Psi-JT. It is defined by:

$$(T_j - T_C) / \text{overall package power}$$

The method of measurement of the thermal parameters is defined in EIA/JEDEC-standard document EIA-JESD51-2.

**THETA-JA ( $\theta_{JA}$ ) VERSUS AIRFLOW**

| FORCED AIR (m/s) | THETA-JA ( $\theta_{JA}$ ) |
|------------------|----------------------------|
| 0                | 24°C/W                     |
| 1                | 21°C/W                     |
| 2.5              | 19°C/W                     |

## 12. AC CHARACTERISTICS

### AC CHARACTERISTICS—MULTIPLEXED PARALLEL PORT

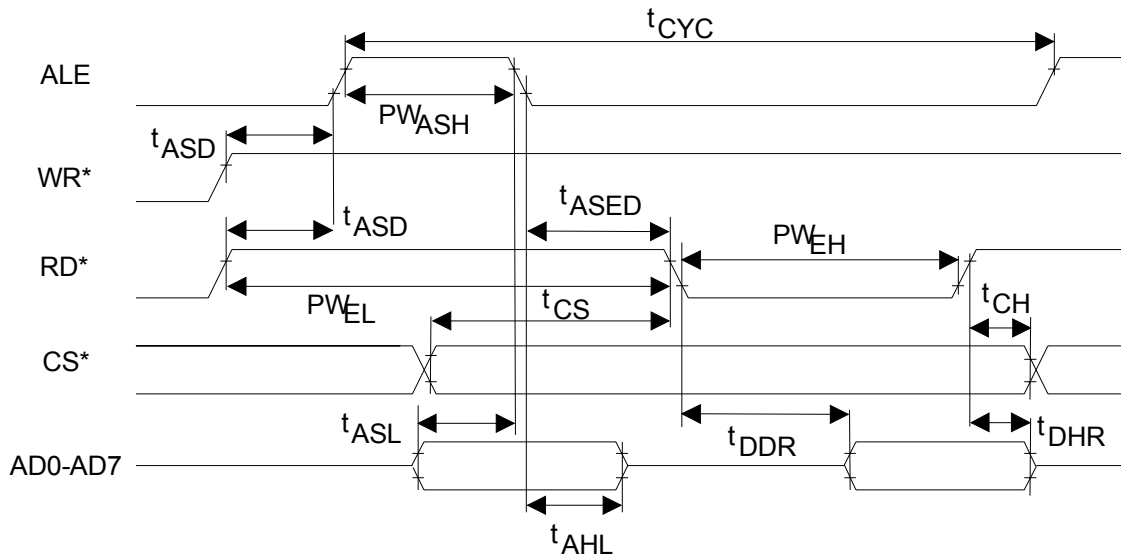
(BIS1 = 0, BIS0 = 0)

(-40°C to +85°C;  $V_{DD} = 3.3V \pm 5\%$ ;-40°C to +85°C;  $V_{DD} = 5.0V \pm 5\%$ )

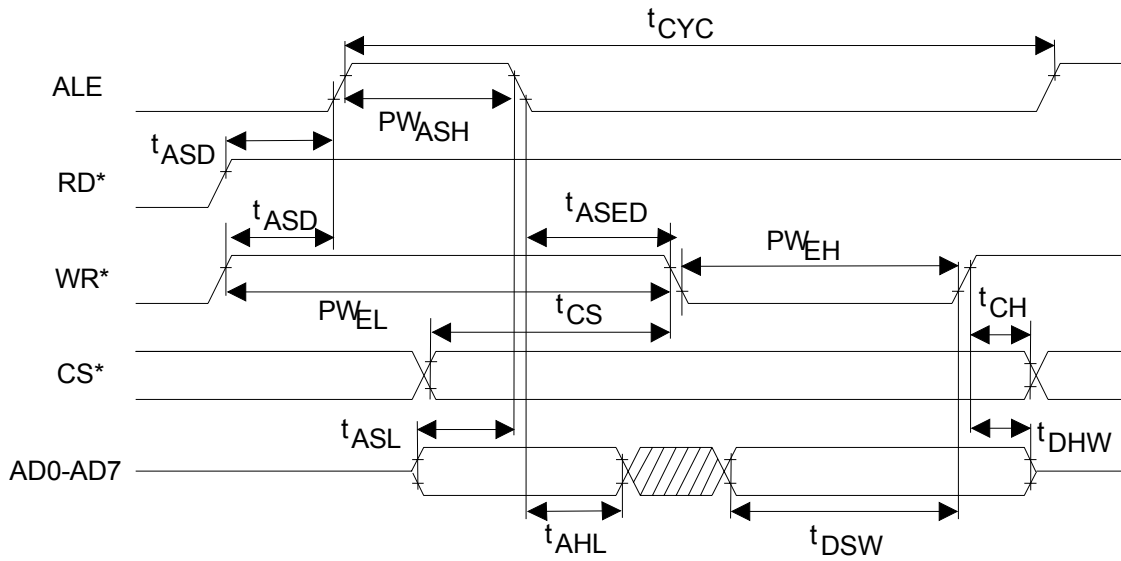
| PARAMETER                                   | SYMBOL     | MIN | TYP | MAX | UNITS | NOTES |
|---|------------|-----|-----|-----|-------|-------|
| Cycle Time                                  | $t_{CYC}$  | 200 |     |     | ns    |       |
| Pulse Width, DS Low or RD* High             | $PW_{EL}$  | 100 |     |     | ns    |       |
| Pulse Width, DS High or RD* Low             | $PW_{EH}$  | 100 |     |     | ns    |       |
| Input Rise/Fall Times                       | $t_R, t_F$ |     |     | 20  | ns    |       |
| R/W* Hold Time                              | $t_{RWH}$  | 10  |     |     | ns    |       |
| R/W* Setup Time Before DS High              | $t_{RWS}$  | 50  |     |     | ns    |       |
| CS* Setup Time Before DS, WR* or RD* Active | $t_{CS}$   | 20  |     |     | ns    |       |
| CS* Hold Time                               | $t_{CH}$   | 0   |     |     | ns    |       |
| Read Data Hold Time                         | $t_{DHR}$  | 10  |     | 50  | ns    |       |
| Write Data Hold Time                        | $t_{DHW}$  | 0   |     |     | ns    |       |
| Muxed Address Valid to AS or ALE Fall       | $t_{ASL}$  | 15  |     |     | ns    |       |
| Muxed Address Hold Time                     | $t_{AHL}$  | 10  |     |     | ns    |       |
| Delay Time DS, WR* or RD* to AS or ALE Rise | $t_{ASD}$  | 20  |     |     | ns    |       |
| Pulse Width AS or ALE High                  | $PW_{ASH}$ | 30  |     |     | ns    |       |
| Delay Time, AS or ALE to DS, WR* or RD*     | $t_{ASED}$ | 10  |     |     | ns    |       |
| Output Data Delay Time from DS or RD*       | $t_{DDR}$  | 20  |     | 80  | ns    |       |
| Data Setup Time                             | $t_{DSW}$  | 50  |     |     | ns    |       |

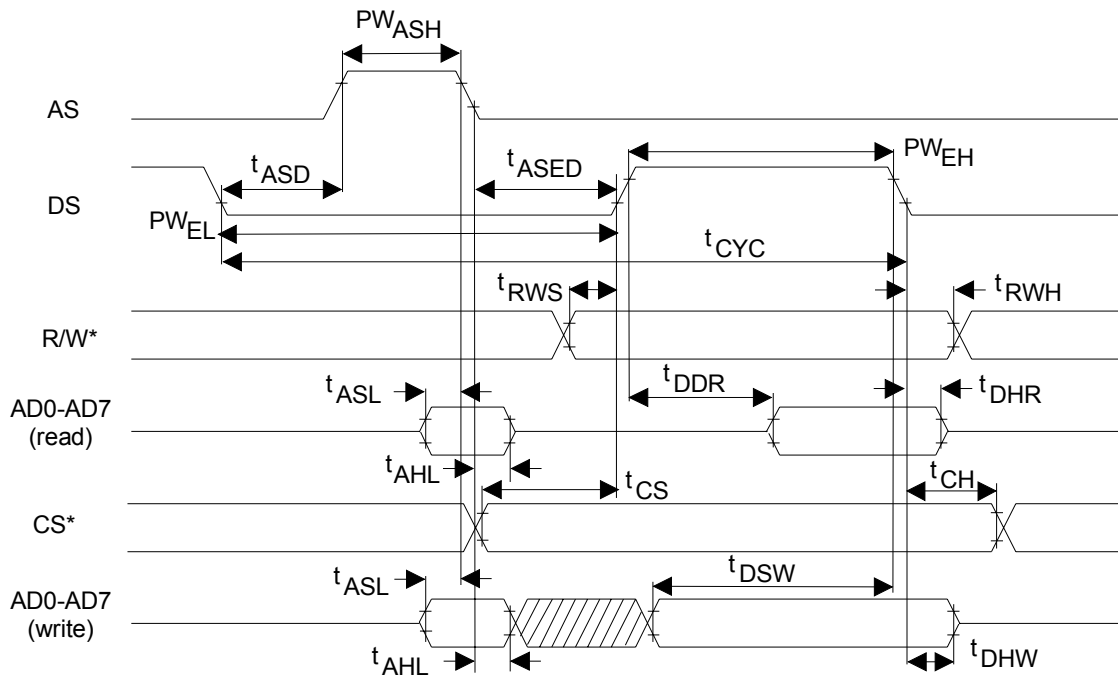
See Figure 12-1, Figure 12-2, Figure 12-3

## INTEL BUS READ TIMING (PBTS = 0, BIS1 = 0, BIS0 = 0) Figure 12-1



## INTEL BUS WRITE TIMING (PBTS = 0, BIS1 = 0, BIS0 = 0) Figure 12-2



**MOTOROLA BUS TIMING (PBTS = 1, BIS1 = 0, BIS0 = 0) Figure 12-3**


**AC CHARACTERISTICS—NONMULTIPLEXED PARALLEL PORT**

(BIS1 = 0, BIS0 = 1)

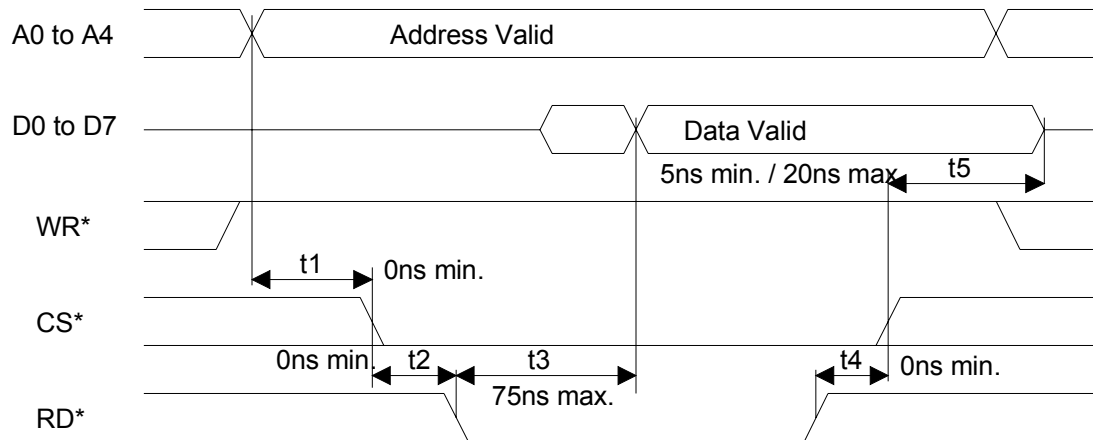
(-40°C to +85°C;  $V_{DD} = 3.3V \pm 5\%$ )

| PARAMETER   | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|--------|-----|-----|-----|-------|-------|
| Setup Time for A0 to A4, Valid to CS* Active                    | t1     | 0   |     |     | ns    |       |
| Setup Time for CS* Active to Either RD*, WR*, or DS* Active     | t2     | 0   |     |     | ns    |       |
| Delay Time from Either RD* or DS* Active to Data Valid          | t3     |     |     | 75  | ns    |       |
| Hold Time from Either RD*, WR*, or DS* Inactive to CS* Inactive | t4     | 0   |     |     | ns    |       |
| Hold Time from CS* Inactive to Data Bus 3-State                 | t5     | 5   |     | 20  | ns    |       |
| Wait Time from Either WR* or DS* Active to Latch Data           | t6     | 75  |     |     | ns    |       |
| Data Setup Time to Either WR* or DS* Inactive                   | t7     | 10  |     |     | ns    |       |
| Data Hold Time from Either WR* or DS* Inactive                  | t8     | 10  |     |     | ns    |       |
| Address Hold from Either WR* or DS* Inactive                    | t9     | 10  |     |     | ns    |       |

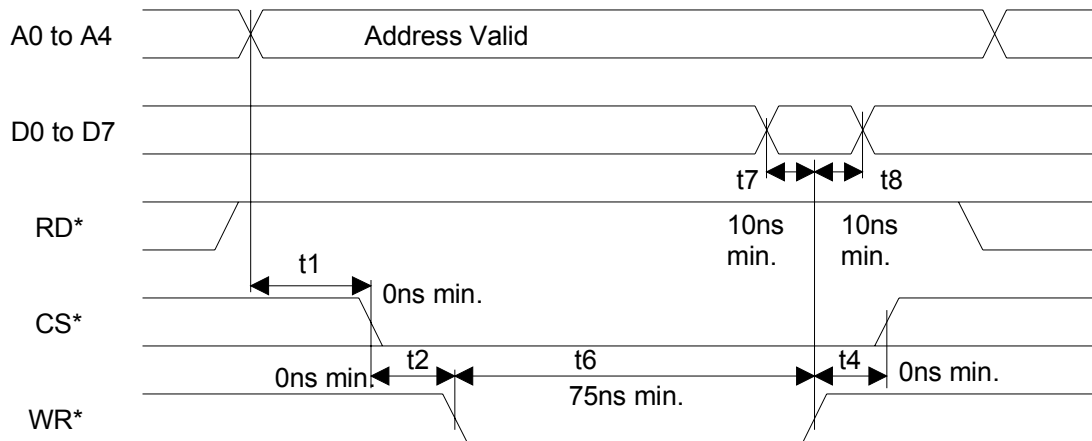
See Figure 12-4, Figure 12-5, Figure 12-6, and Figure 12-7

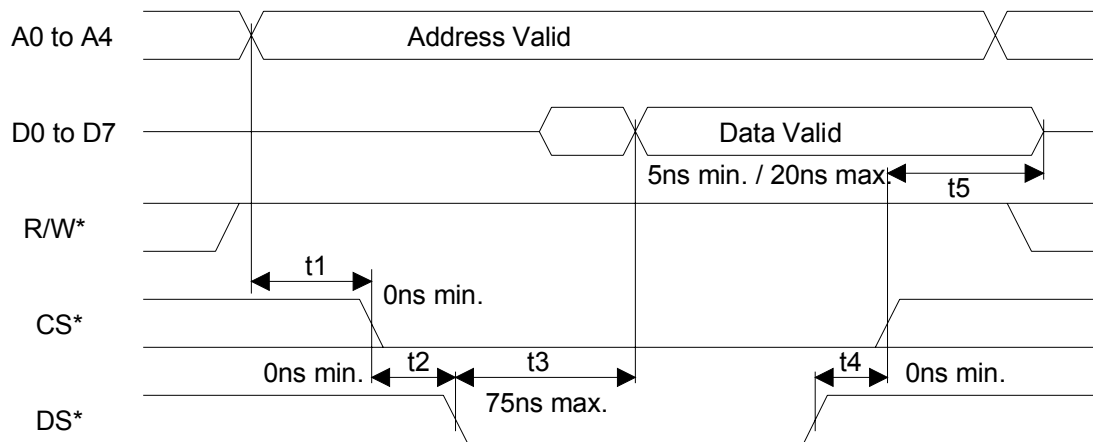
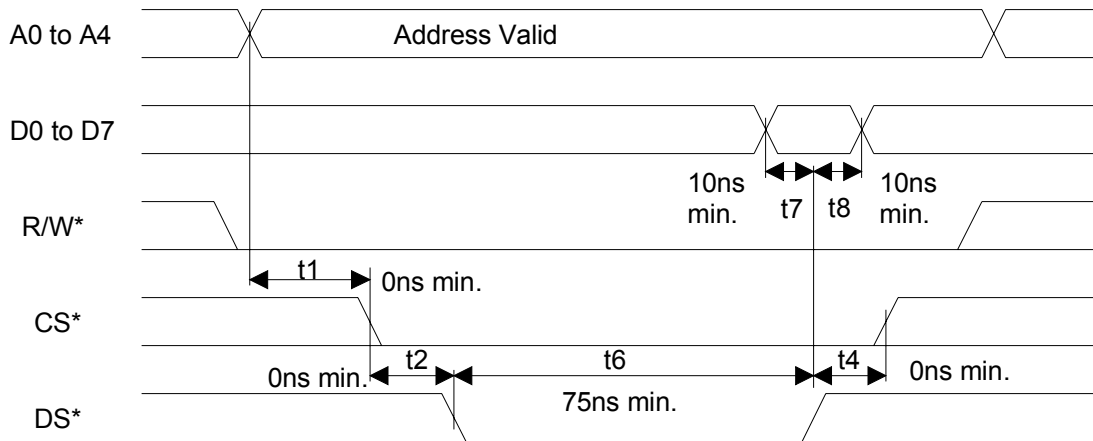


## INTEL BUS READ TIMING (PBTS = 0, BIS1 = 0, BIS0 = 1) Figure12-4



## INTEL BUS WRITE TIMING (PBTS = 0, BIS1 = 0, BIS0 = 1) Figure 12-5



**MOTOROLA BUS READ TIMING (PBTS = 1, BIS1 = 0, BIS0 = 1) Figure 12-6****MOTOROLA BUS WRITE TIMING (PBTS = 1, BIS1 = 0, BIS0 = 1) Figure 12-7**

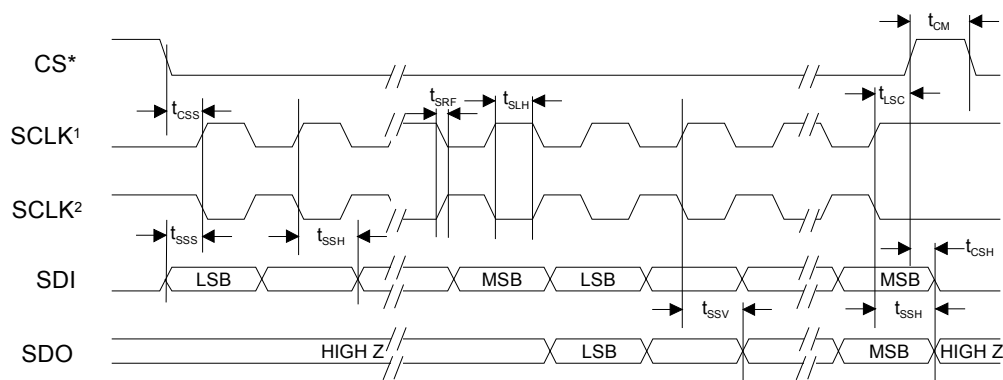
**AC CHARACTERISTICS—SERIAL PORT**

(BIS1 = 1, BIS0 = 0)

(-40°C to +85°C;  $V_{DD} = 3.3V \pm 5\%$ )

| PARAMETER                   | SYMBOL    | MIN | TYP | MAX | UNITS | NOTES |
|-----------------------------|-----------|-----|-----|-----|-------|-------|
| Setup Time CS* to SCLK      | $t_{CSS}$ | 50  |     |     | ns    |       |
| Setup Time SDI to SCLK      | $t_{SSS}$ | 50  |     |     | ns    |       |
| Hold Time SCLK to SDI       | $t_{SSH}$ | 50  |     |     | ns    |       |
| SCLK High/Low Time          | $t_{SLH}$ | 200 |     |     | ns    |       |
| SCLK Rise/Fall Time         | $t_{SRF}$ |     |     | 50  | ns    |       |
| SCLK to CS* Inactive        | $t_{LSC}$ | 50  |     |     | ns    |       |
| CS* Inactive Time           | $t_{CM}$  | 250 |     |     | ns    |       |
| SCLK to SDO Valid           | $t_{SSV}$ |     |     | 50  | ns    |       |
| SCLK to SDO 3-State         | $t_{SSH}$ |     | 100 |     | ns    |       |
| CS* Inactive to SDO 3-State | $t_{CSH}$ |     | 100 |     | ns    |       |

See

**SERIAL BUS TIMING (BIS1 = 1, BIS0 = 0) Figure 12-8****NOTES:**

- 1) OCES = 1 and ICES = 0.
- 2) OCES = 0 and ICES = 1.

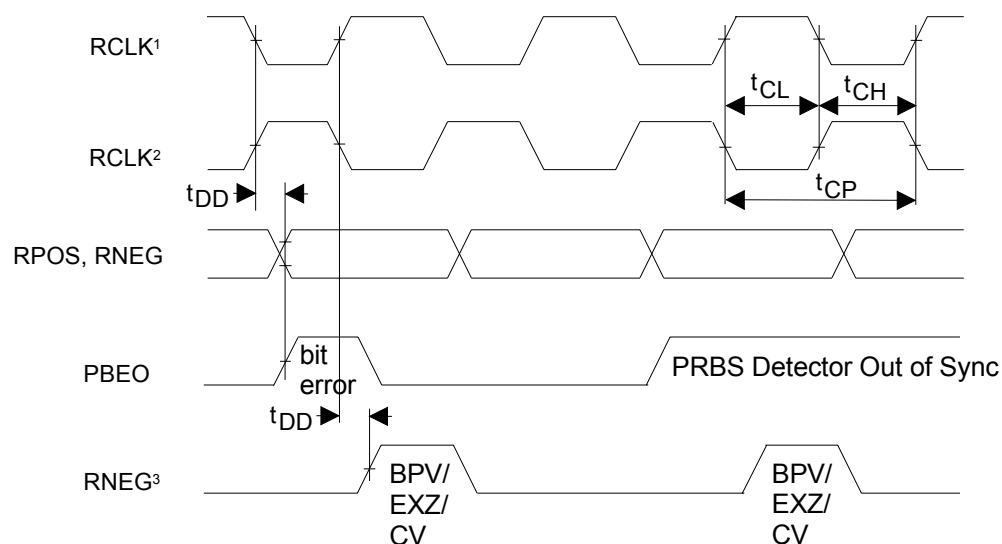
**AC CHARACTERISTICS—RECEIVE SIDE** (-40°C to +85°C;  $V_{DD} = 3.3V \pm 5\%$ )

| PARAMETER                                  | SYMBOL               | MIN | TYP | MAX | UNITS | NOTES |
|--|----------------------|-----|-----|-----|-------|-------|
| RCLK Period                                | $t_{CP}$             |     | 488 |     | ns    | 1     |
|  |                      |     | 648 |     | ns    | 2     |
| RCLK Pulse Width                           | $t_{CH}$<br>$t_{CL}$ | 200 |     |     | ns    | 3     |
|  |                      | 200 |     |     | ns    | 3     |
| RCLK Pulse Width                           | $t_{CH}$<br>$t_{CL}$ | 150 |     |     | ns    | 4     |
|  |                      | 150 |     |     | ns    | 4     |
| Delay RCLK to RPOS, RNEG, PBE0, RBPV Valid | $t_{DD}$             |     |     | 50  | ns    |       |

See Figure 12-9

**NOTES:**

- 1) E1 Mode.
- 2) T1 or J1 Mode.
- 3) Jitter attenuator enabled in the receive path.
- 4) Jitter attenuator disabled or enabled in the transmit path.

**Figure 12-9 RECEIVE SIDE TIMING****NOTES:**

- 1) RCES = 1 (CCR2.0) or CES = 1.
- 2) RCES = 0 (CCR2.0) or CES = 0.
- 3) RNEG is in NRZ mode (CCR1.6 = 1).

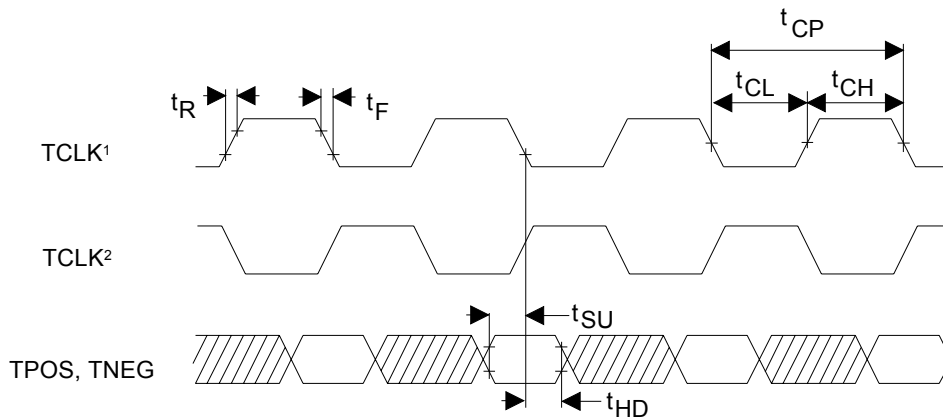
**AC CHARACTERISTICS—TRANSMIT SIDE** (-40°C to +85°C;  $V_{DD} = 3.3V \pm 5\%$ )

| PARAMETER                                     | SYMBOL     | MIN | TYP | MAX | UNITS | NOTES |
|---|------------|-----|-----|-----|-------|-------|
| TCLK Period                                   | $t_{CP}$   |     | 488 |     | ns    | 1     |
|   |            |     | 648 |     | ns    | 2     |
| TCLK Pulse Width                              | $t_{CH}$   | 75  |     |     | ns    |       |
|   | $t_{CL}$   | 75  |     |     | ns    |       |
| TPOS/TNEG Setup to TCLK<br>Falling or Rising  | $t_{SU}$   | 20  |     |     | ns    |       |
| TPOS/TNEG Hold from TCLK<br>Falling or Rising | $t_{HD}$   | 20  |     |     | ns    |       |
| TCLK Rise and Fall Times                      | $t_R, t_F$ |     |     | 25  | ns    |       |

See

**NOTES:**

- 1) E1 Mode.
- 2) T1 or J1 Mode.

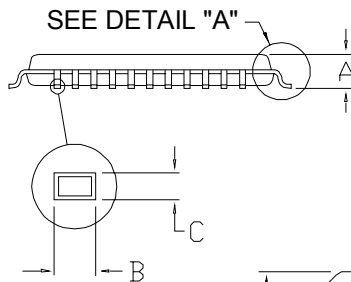
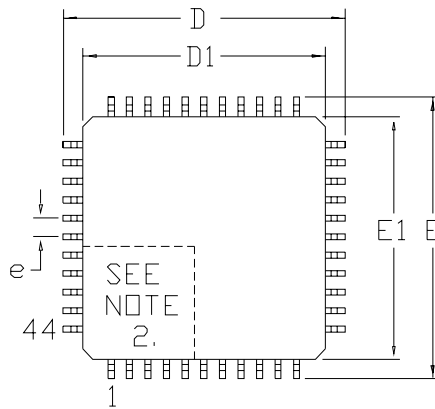
**TRANSMIT SIDE TIMING** Figure 12-10**NOTES:**

- 1) TCES = 0 (CCR2.1) or CES = 0.
- 2) TCES = 1 (CCR2.1) or CES = 1.

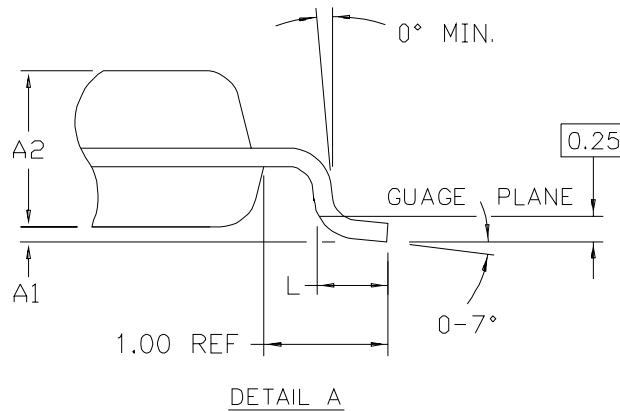
# 13. MECHANICAL DIMENSIONS

NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



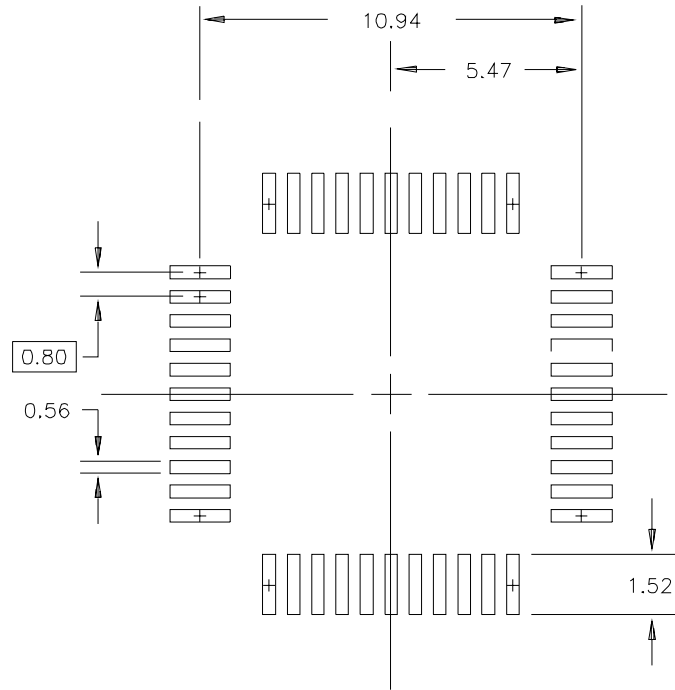
| DIM | MIN   | MAX   |
|-----|-------|-------|
| A   | -     | 1.20  |
| A1  | 0.05  | 0.15  |
| A2  | 0.95  | 1.05  |
| D   | 11.80 | 12.20 |
| D1  | 10.00 | BSC   |
| E   | 11.80 | 12.20 |
| E1  | 10.00 | BSC   |
| L   | 0.45  | 0.75  |
| e   | 0.80  | BSC   |
| B   | 0.30  | 0.45  |
| C   | 0.09  | 0.20  |

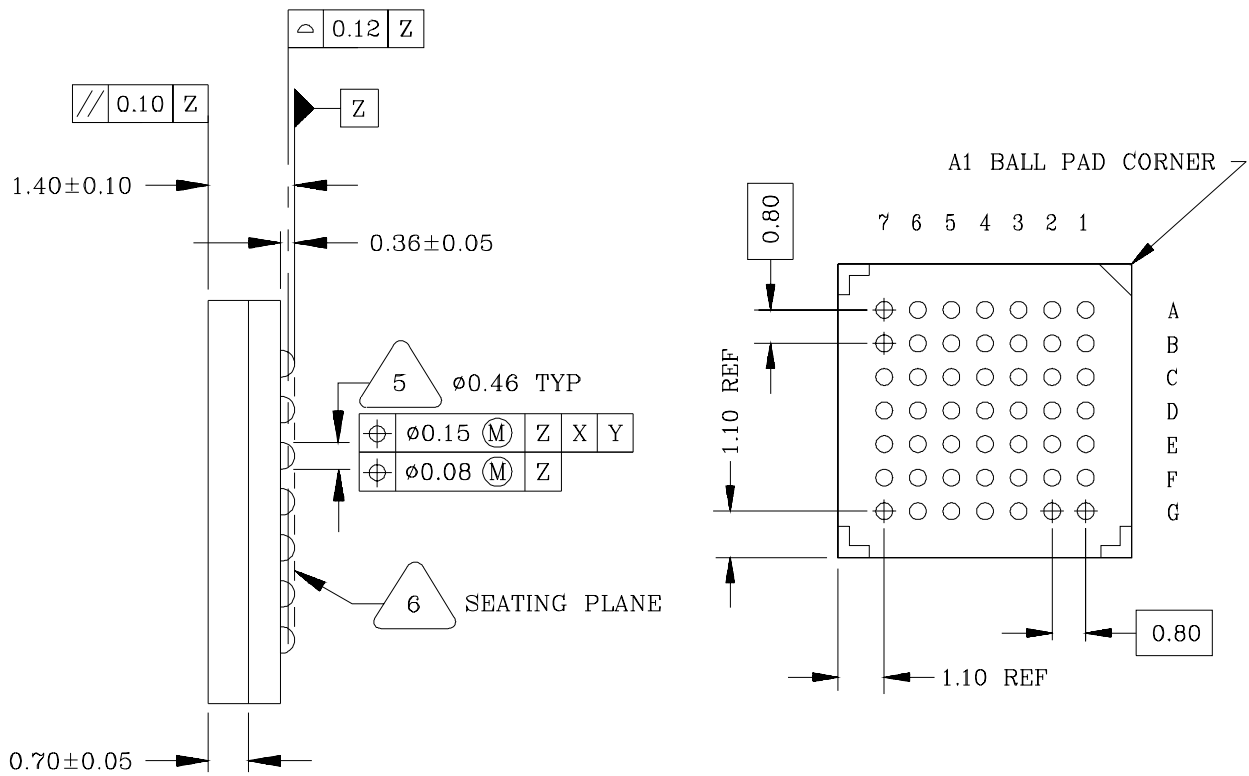
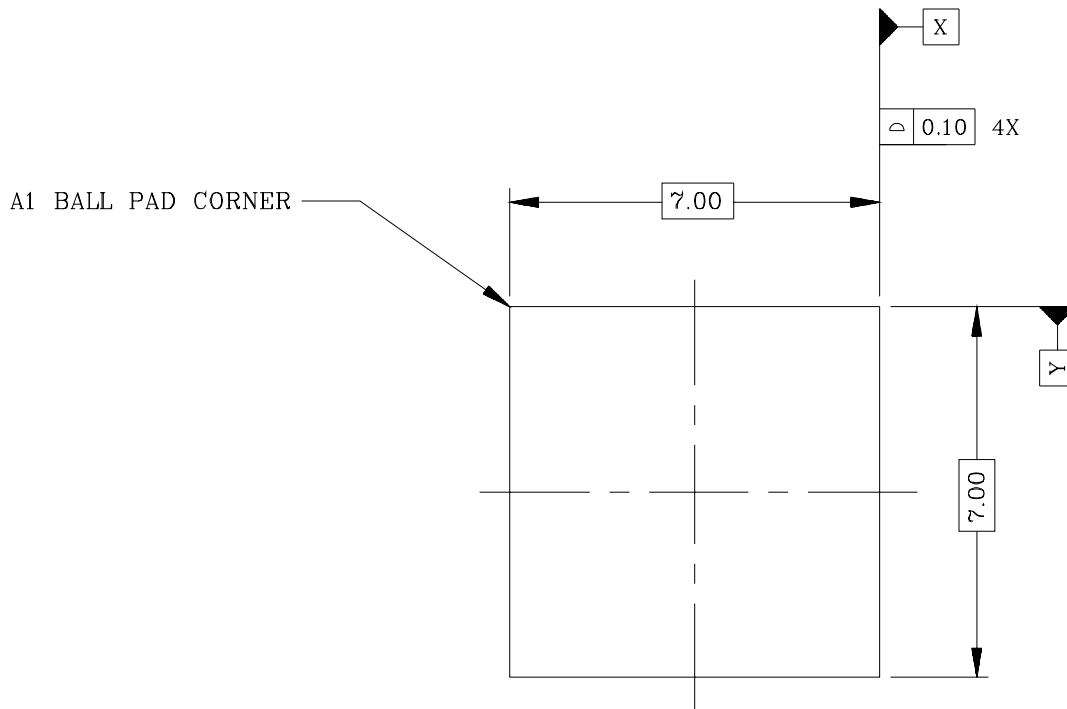


DIMENSIONS ARE IN MILLIMETERS

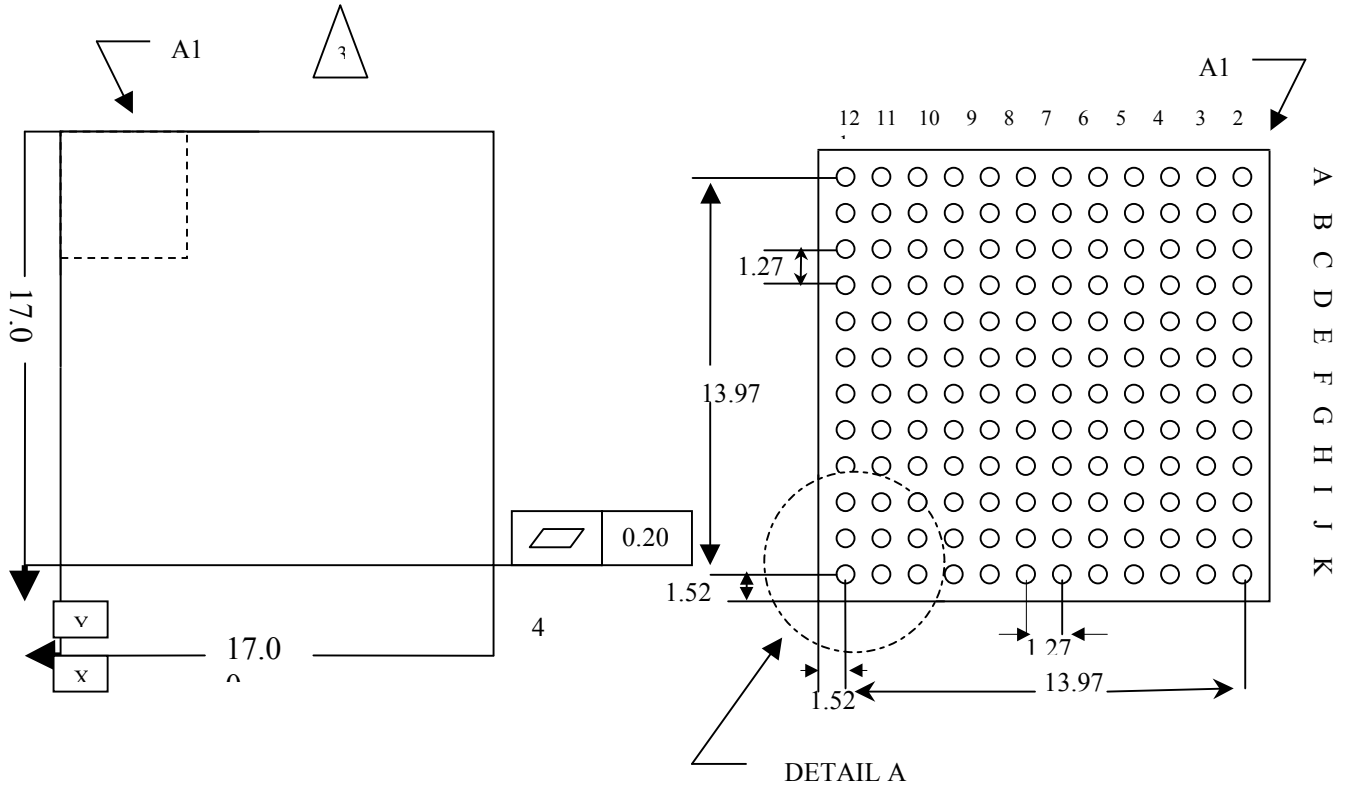
## SUGGESTED PAD LAYOUT

### 44 PIN TQFP, 10\*10\*1.0



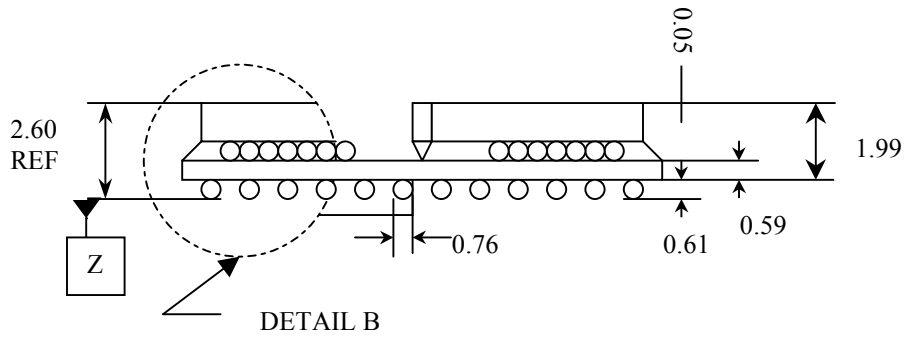


### 13.1 Mechanical Dimensions—Quad Version



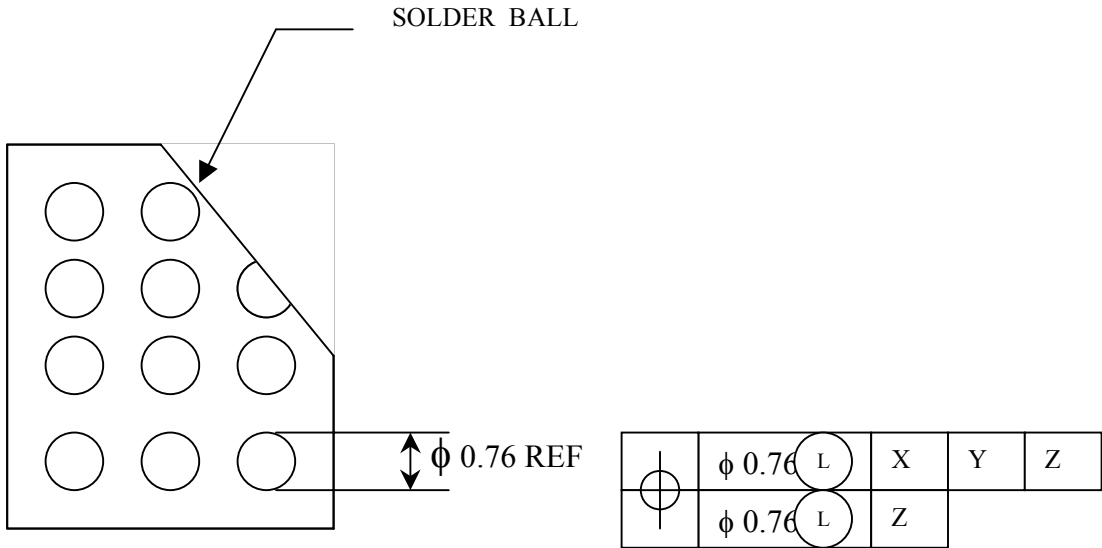
**TOP VIEW (DIE SIDE)**

**BOTTOM VIEW (BALL SIDE)**

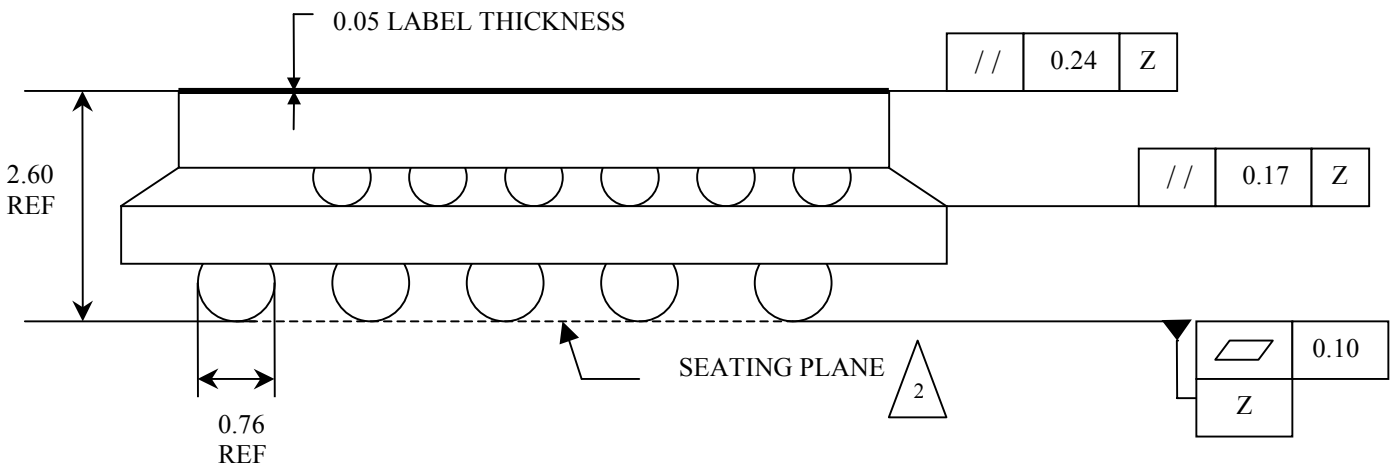


**SIDE VIEW**





**DETAIL A**



**DETAIL B**