Rev 2; 12/04

DALLAS SEMICONDUCTOR MAXIM

RTC with Constant-Voltage Trickle Charger

General Description

The DS12R885 is a functional drop-in replacement for the DS12885 real-time clock (RTC). The device provides an RTC/calendar, one time-of-day alarm, three maskable interrupts with a common interrupt output, a programmable square wave, and 114 bytes of battery-backed static RAM. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. It also operates in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to a backup supply. The V_{BACKUP} pin supports a rechargeable battery or a super cap and includes an integrated, always enabled trickle charger. The DS12R885 is accessed through a multiplexed byte-wide interface, which supports both Intel and Motorola modes. The DS12CR887 and DS12R887 integrate the DS12R885 die with a crystal and battery.

Applications

Embedded Systems

Utility Meters

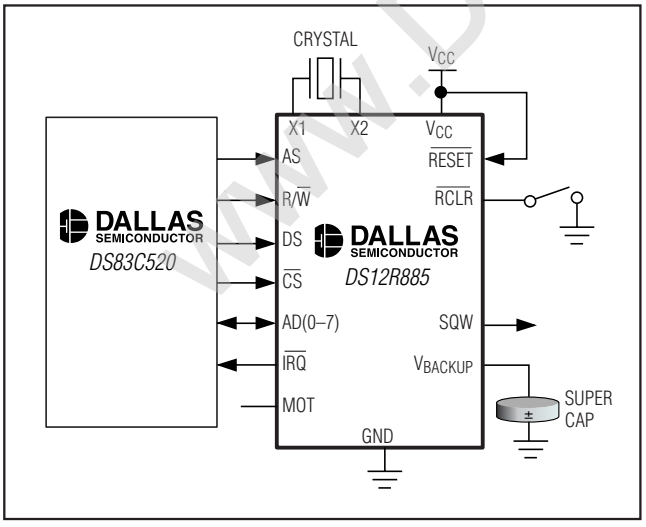
Security Systems

Network Hubs, Bridges, and Routers

Features

- **Trickle-Charge Capability for a Rechargeable Battery or Super Cap**
- **Selectable Intel or Motorola Bus Timing**
- **RTC Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation to 2100**
- **Interrupt Output with Three Independently Maskable Interrupt Flags**
- **Time-of-Day Alarm is Once-per-Second to Once-per-Day**
- **Periodic Rates from 122µs to 500ms**
- **End-of-Clock Update Cycle Flag**
- **14 Bytes of Clock and Control Registers**
- **114 Bytes of General-Purpose RAM with Clear Input**
- **Programmable Square-Wave Output**
- **Automatic Power-Fail Detect and Switch Circuitry**
- **+5.0V or +3.3V Operation**
- **Industrial Temperature Range**
- **DS12CR887 Encapsulated DIP (EDIP) Module with Integrated Battery and Crystal**
- **DS12R887 BGA Module Surface-Mountable Package with Integrated Crystal and Rechargeable Battery**

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS12R885-5	-40°C to +85°C	24 SO (300 mils)	DS12R885-5
DS12R885-33	-40°C to +85°C	24 SO (300 mils)	DS12R885-33
DS12CR887-5	-40°C to +85°C	24 EDIP (700 mils)	DS12CR887-5
DS12CR887-33	-40°C to +85°C	24 EDIP (700 mils)	DS12CR887-33
DS12R887-5	-40°C to +85°C	48 BGA	DS12R887-5
DS12R887-33	-40°C to +85°C	48 BGA	DS12R887-33

Pin Configurations appear at end of data sheet.

RTC with Constant-Voltage Trickle Charger

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground .....-0.3V to +6.0V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification
Soldering Temperature (leads, 10s) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	V_{CC}	-33	2.97	3.3	3.63	V
		-5	4.5	5.0	5.5	
V_{BACKUP} Input Voltage (DS12R885 Only)	V_{BACKUP}	(Note 2)	2.0		V_{OUT}	V
Input Logic 1	V_{IH}	(Note 2)	2.2		V_{CC} + 0.3	V
Input Logic 0	V_{IL}	(Note 2)	-0.3		+0.8	V
V_{CC} Power-Supply Current (Note 3)	I_{CC1}	-33		0.7	2	mA
		-5		0.8	2	
V_{CC} Standby Current (Note 4)	I_{CCS}	-5		0.250	0.5	mA
		-33		0.140	0.3	
Input Leakage	I_{IL}		-1.0		+1.0	µA
I/O Leakage	I_{OL}	(Note 5)	-1.0		+1.0	µA
Input Current	I_{MOT}	(Note 6)	-1.0		+500	µA
Output Current at 2.4V	I_{OH}	(Note 2)	-1.0			mA
Output Current at 0.4V	I_{OL}	(Note 2)			4.0	mA
Power-Fail Voltage (Note 2)	V_{PF}	-33	2.7	2.88	2.97	V
		-5	4.05	4.33	4.5	
VRT Trip Point	VRT_{TRIP}	-33		1.3		V
		-5				
Trickle-Charger Current-Limiting Resistor	R1	DS12R885 Only		10		kΩ
Trickle-Charger Output Voltage	V_{OUT}	DS12R885 Only		3.05		V

DC ELECTRICAL CHARACTERISTICS (DS12R885 Only)

(**V_{CC} = 0V, V_{BACKUP} = 3.2V**, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current (OSC On); T_A = +25°C, V_{BACKUP} = 3.0V	$I_{BACKUP2}$	(Note 7)		800	1000	nA
V_{BACKUP} Current (Oscillator Off)	$I_{BACKUPDR}$	(Note 7)			100	nA

AC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 4.5V to 5.5V**, T_A = -40°C to +85°C.) (Note 1)

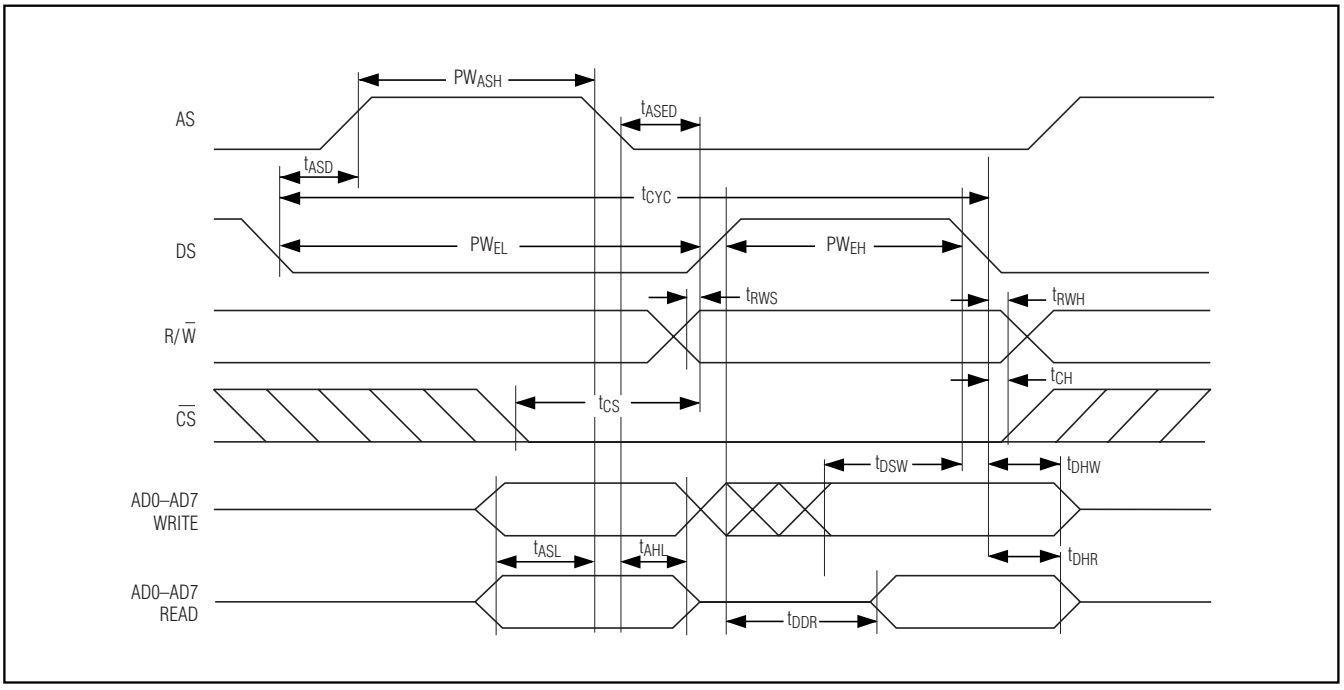
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}		180		DC	ns
Pulse Width, DS Low or R/$\overline{W}$ High	PW_{EL}		80			ns
Pulse Width, DS High or R/$\overline{W}$ Low	PW_{EH}		65			ns
Input Rise and Fall	t_R, t_F				30	ns
R/$\overline{W}$ Hold Time	t_{RWH}		0			ns
R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}		10			ns
Chip-Select Setup Time Before DS or R/$\overline{W}$	t_{CS}		5			ns
Chip-Select Hold Time	t_{CH}		0			ns
Read-Data Hold Time	t_{DHR}		5		35	ns
Write-Data Hold Time	t_{DHW}		0			ns
Address Valid Time to AS Fall	t_{ASL}		20			ns
Address Hold Time to AS Fall	t_{AHL}		5			ns
Delay Time DS/E to AS Rise	t_{ASD}		10			ns
Pulse Width AS High	PW_{ASH}		30			ns
Delay Time, AS to DS/E Rise	t_{ASED}		35			ns
Output Data Delay Time from DS or R/$\overline{W}$	t_{DDR}	(Note 8)	15		60	ns
Data Setup Time	t_{DSW}		50			ns
Reset Pulse Width	t_{RWL}		5			µs
$\overline{IRQ}$ Release from DS	t_{IRDS}		0		2	µs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}		0		2	µs

AC ELECTRICAL CHARACTERISTICS

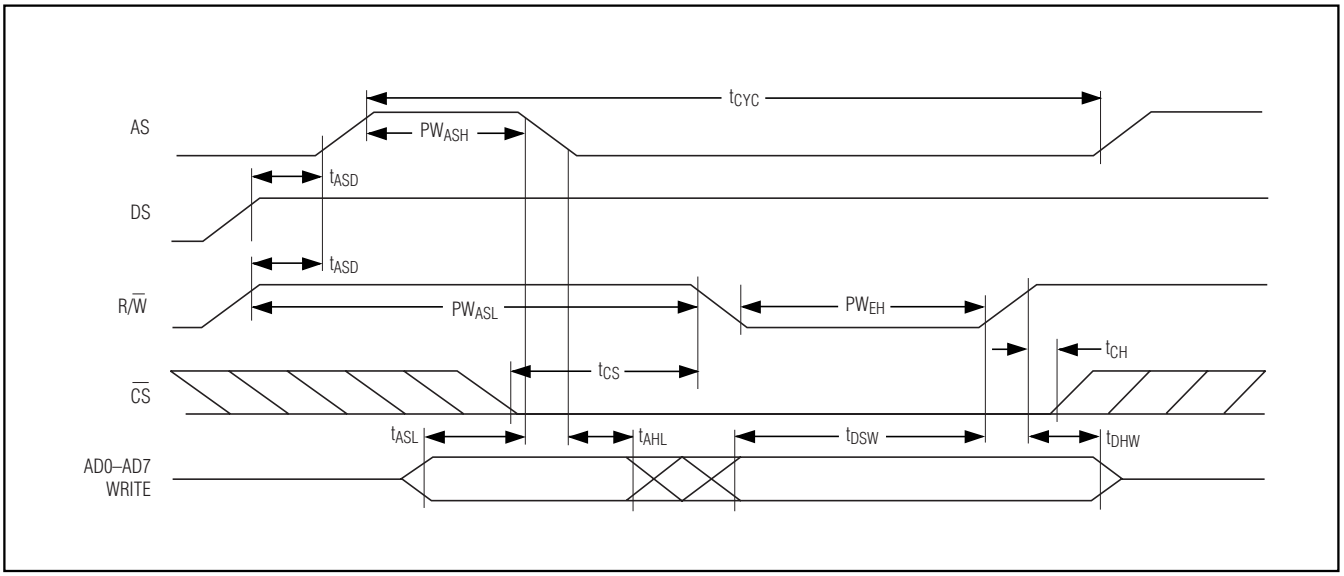
(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time	t_{CYC}		280		DC	ns
Pulse Width, DS Low or R/$\overline{W}$ High	PW_{EL}		130			ns
Pulse Width, DS High or R/$\overline{W}$ Low	PW_{EH}		90			ns
Input Rise and Fall	t_R, t_F				30	ns
R/$\overline{W}$ Hold Time	t_{RWH}		0			ns
R/$\overline{W}$ Setup Time Before DS	t_{RWS}		15			ns
Chip-Select Setup Time Before DS or R/$\overline{W}$	t_{CS}		8			ns
Chip-Select Hold Time	t_{CH}		0			ns
Read-Data Hold Time	t_{DHR}		5		55	ns
Write-Data Hold Time	t_{DHW}		0			ns
Address Valid Time to AS Fall	t_{ASL}		30			ns
Address Hold Time to AS Fall	t_{AHL}		15			ns
Delay Time DS to AS Rise	t_{ASD}		15			ns
Pulse Width AS High	PW_{ASH}		45			ns
Delay Time, AS to DS Rise	t_{ASED}		55			ns
Output Data Delay Time from DS or R/$\overline{W}$	t_{DDR}	(Note 8)	20		80	ns
Data Setup Time	t_{DSW}		70			ns
Reset Pulse Width	t_{RWL}		5			µs
$\overline{IRQ}$ Release from DS	t_{IRDS}		0		2	µs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}		0		2	µs

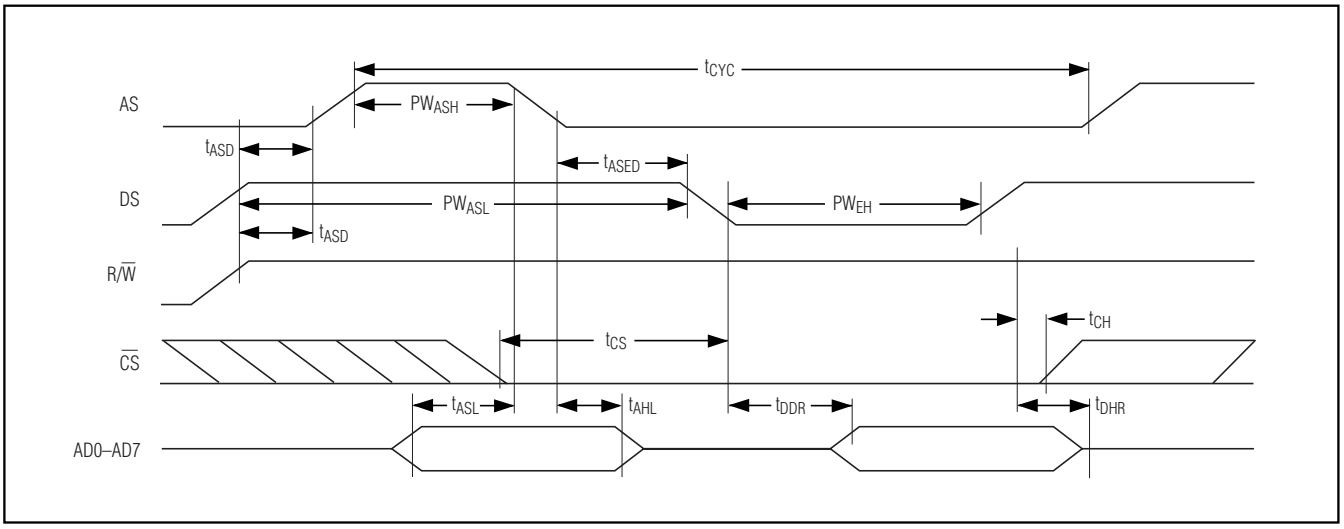
Motorola Bus Read/Write Timing



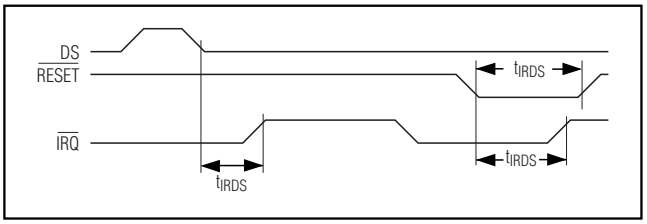
Intel Bus Write Timing



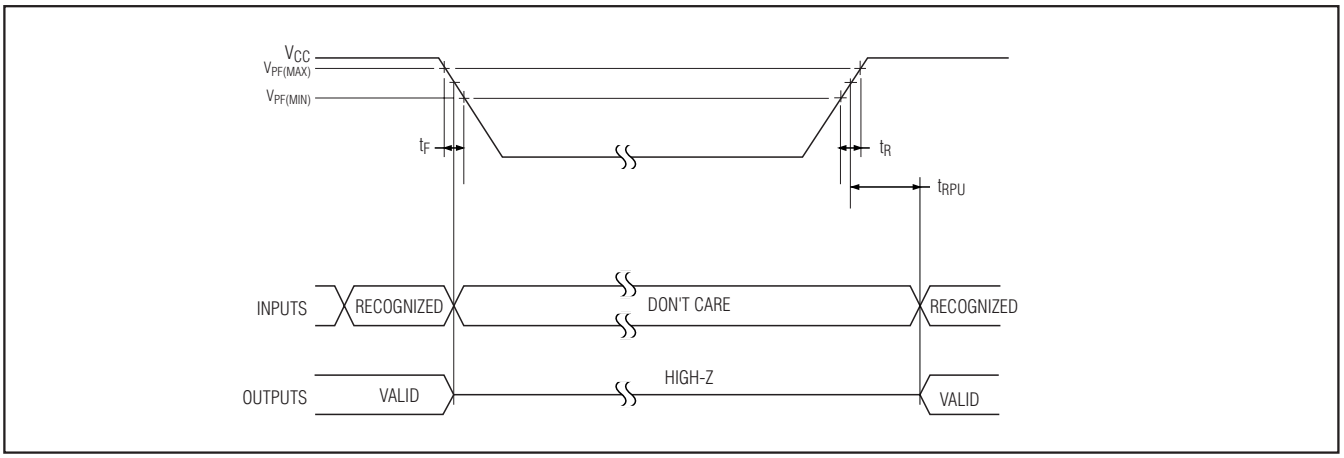
Intel Bus Read Timing



IRQ Release Delay Timing



Power-Up/Power-Down Timing



POWER-UP/POWER-DOWN CHARACTERISTICS

(T_A = -40°C to +85°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{RPU}		20		200	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R		0			µs

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins Except X1 and X2	C_{IN}	(Note 9)			10	pF
Capacitance on $\overline{IRQ}$, SQW, and DQ Pins	C_{IO}	(Note 9)			10	pF

AC TEST CONDITIONS

PARAMETER	TEST CONDITIONS
Input Pulse Levels (-5)	0 to 3.0V
Input Pulse Levels (-33)	0 to 2.7V
Output Load Including Scope and Jig (-5)	50pF + 1TTL Gate
Output Load Including Scope and Jig (-33)	25pF + 1TTL Gate
Input and Output Timing Measurement Reference Levels	Input/Output: V_{IL} maximum and V_{IH} minimum
Input-Pulse Rise and Fall Times	5ns

WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

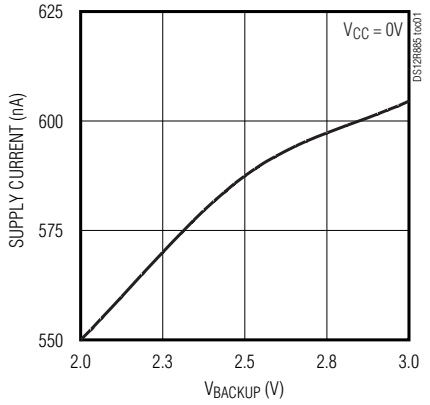
Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: All outputs are open.
Note 4: Specified with $\overline{CS}$ = DS = R/$\overline{W}$ = $\overline{RESET}$ = V_{CC}; MOT, AS, AD0–AD7 = 0; V_{BACKUP} open.
Note 5: Applies to the AD0 to AD7 pins, the $\overline{IRQ}$ pin, and the SQW pin when each is in a high-impedance state.
Note 6: The MOT pin has an internal 20kΩ pulldown.
Note 7: Measured with a 32.768kHz crystal attached to X1 and X2.
Note 8: Measured with a 50pF capacitance load.
Note 9: Guaranteed by design. Not production tested.

RTC with Constant-Voltage Trickle Charger

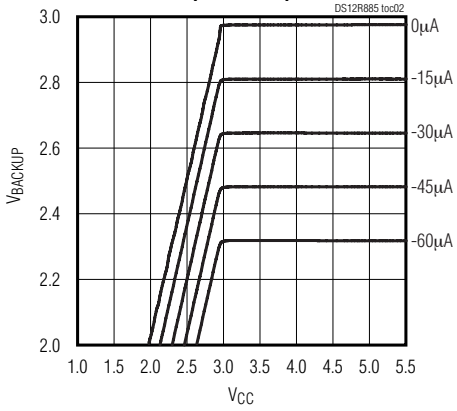
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

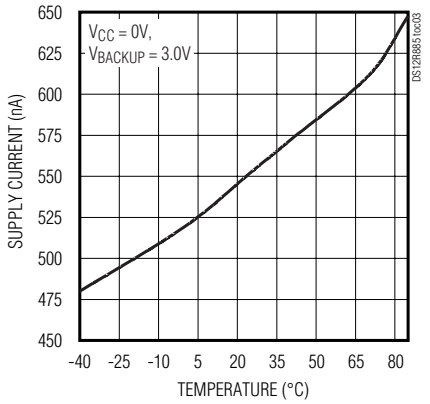
IBACKUP vs. VBACKUP (DS12R885)



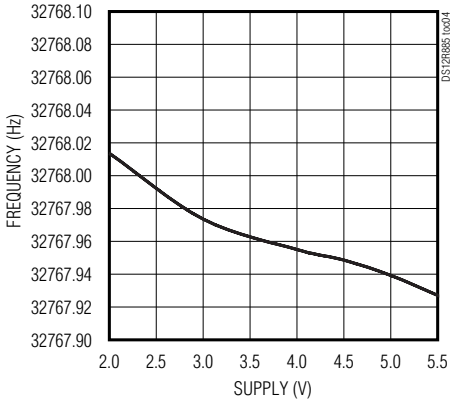
VBACKUP vs. VCC vs. IBACKUP (DS12R885)



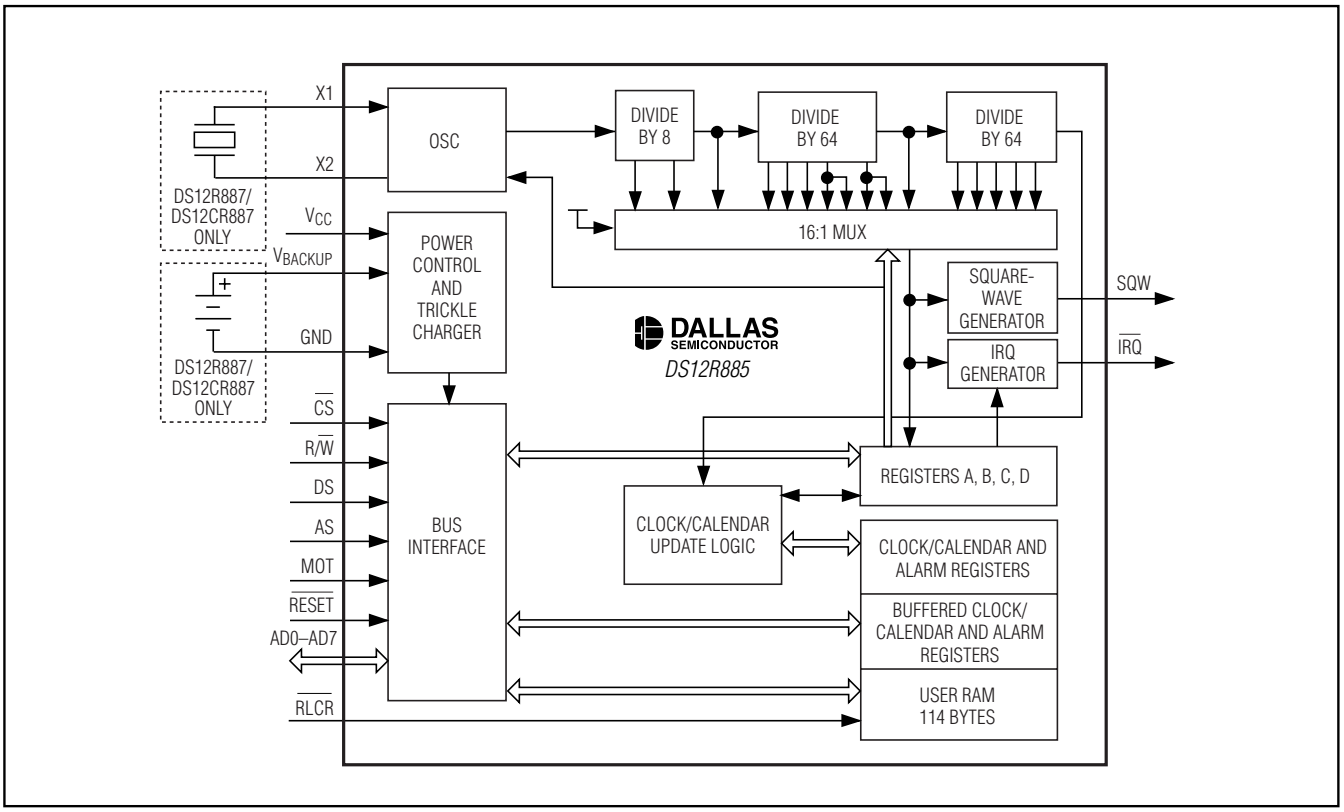
IBACKUP vs. TEMPERATURE (DS12R885)



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



Functional Diagram



Pin Description

PIN			NAME	FUNCTION
SO	EDIP	BGA		
1	1	C5	MOT	Motorola or Intel Bus Timing Selector. This pin selects one of two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pulldown resistor.
2	—	—	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a 12.5pF specified load capacitance (C_L). Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1.
3	—	—	X2	
4–11	4–11	F4, D4, F3, D3, F2, D2, F1, D1	AD0–AD7	Multiplexed, Bidirectional Address/Data Bus. The addresses are presented during the first portion of the bus cycle and latched into the DS12R885 by the falling edge of AS. Write data is latched by the falling edge of DS (Motorola timing) or the rising edge of R/$\overline{W}$ (Intel timing). In a read cycle, the DS12R885 outputs data during the latter portion of DS (DS and R/$\overline{W}$ high for Motorola timing, DS low and R/$\overline{W}$ high for Intel timing). The read cycle is terminated and the bus returns to a high-impedance state as DS transitions low in the case of Motorola timing or as DS transitions high in the case of Intel timing.

RTC with Constant-Voltage Trickle Charger

Pin Description (continued)

PIN			NAME	FUNCTION
SO	EDIP	BGA		
12	12	D5–D8, E1–E8, F5–F8	GND	Ground
13	13	C1	$\overline{CS}$	Chip-Select Input. The active-low chip-select signal must be asserted low for a bus cycle in the DS12R885 to be accessed. $\overline{CS}$ must be kept in the active state during DS and AS for Motorola timing and during DS and R/$\overline{W}$ for Intel timing. Bus cycles that take place without asserting $\overline{CS}$ latch addresses, but no access occurs. When V_{CC} is below V_{PF} volts, the DS12R885 inhibits access by internally disabling the $\overline{CS}$ input. This action protects the RTC data and the RAM data during power outages.
14	14	C3	AS	Address Strobe Input. A positive-going address-strobe pulse serves to demultiplex the bus. The falling edge of AS causes the address to be latched within the DS12R885. The next rising edge that occurs on the AS bus clears the address regardless of whether $\overline{CS}$ is asserted. An address strobe must immediately precede each write or read access. If a write or read is performed with $\overline{CS}$ deasserted, another address strobe must be performed prior to a read or write access with $\overline{CS}$ asserted.
15	15	C2	R/$\overline{W}$	Read/Write Input. The R/$\overline{W}$ pin has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, R/$\overline{W}$ is at a level that indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high. A write cycle is indicated when R/$\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the R/$\overline{W}$ signal is an active-low signal. In this mode, the R/$\overline{W}$ pin operates in a similar fashion as the write-enable signal ($\overline{WE}$) on generic RAMs. Data are latched on the rising edge of the signal.
16, 22	2, 3, 16, 20–22	A3	N.C.	No Connection. This pin should remain unconnected. On the EDIP, these pins are missing by design.
17	17	A1	DS	Data Strobe or Read Input. The DS pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode, DS is a positive pulse during the latter portion of the bus cycle and is called data strobe. During read cycles, DS signifies the time that the DS12R885 is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the DS12R885 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. DS identifies the time period when the DS12R885 drives the bus with read data. In this mode, the DS pin operates in a similar fashion as the output-enable ($\overline{OE}$) signal on a generic RAM.

Pin Description (continued)

PIN			NAME	FUNCTION
SO	EDIP	BGA		
18	18	A2	$\overline{\text{RESET}}$	Reset Input. The $\overline{\text{RESET}}$ pin has no effect on the clock, calendar, or RAM. On power-up, the $\overline{\text{RESET}}$ pin can be held low for a time to allow the power supply to stabilize. The amount of time that $\overline{\text{RESET}}$ is held low is dependent on the application. However, if $\overline{\text{RESET}}$ is used on power-up, the time $\overline{\text{RESET}}$ is low should exceed 200ms to ensure that the internal timer that controls the DS12R885 on power-up has timed out. When $\overline{\text{RESET}}$ is low and V_{CC} is above V_{PF}, the following occurs: A. Periodic interrupt-enable (PIE) bit is cleared to 0. B. Alarm interrupt-enable (AIE) bit is cleared to 0. C. Update-ended interrupt-enable (UIE) bit is cleared to 0. D. Periodic-interrupt flag (PF) bit is cleared to 0. E. Alarm-interrupt flag (AF) bit is cleared to 0. F. Update-ended interrupt flag (UF) bit is cleared to 0. G. Interrupt-request status flag (IRQF) bit is cleared to 0. H. $\overline{\text{IRQ}}$ pin is in the high-impedance state. I. The device is not accessible until $\overline{\text{RESET}}$ is returned high. J. Square-wave output-enable (SQWE) bit is cleared to 0. In a typical application, $\overline{\text{RESET}}$ can be connected to V_{CC}. This connection allows the DS12R885 to go in and out of power fail without affecting any of the control registers.
19	19	A4	$\overline{\text{IRQ}}$	Interrupt Request Output. The $\overline{\text{IRQ}}$ pin is an active-low output of the DS12R885 that can be used as an interrupt input to a processor. The $\overline{\text{IRQ}}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The processor program normally reads the C register to clear the $\overline{\text{IRQ}}$ pin. The $\overline{\text{RESET}}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high-impedance state. Multiple interrupting devices can be connected to an $\overline{\text{IRQ}}$ bus, provided that they are all open drain. The $\overline{\text{IRQ}}$ pin is an open-drain output and requires an external pullup resistor to V_{CC}.
20	—	—	V_{BACKUP}	Connection for Rechargeable Battery or Super Cap. This pin provides trickle charging when V_{CC} is greater than V_{BACKUP}.
21	—	A5	$\overline{\text{RCLR}}$	RAM Clear. The active-low $\overline{\text{RCLR}}$ pin is used to clear (set to logic 1) all 114 bytes of general-purpose RAM, but does not affect the RAM associated with the RTC. To clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic 0 during battery-backup mode when V_{CC} is not applied. The $\overline{\text{RCLR}}$ function is designed to be used through a human interface (shorting to ground manually or by a switch) and not to be driven with external buffers. This pin is internally pulled up. Do not use an external pullup resistor on this pin.
23	23	C4	SQW	Square-Wave Output. The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the RTC. The frequency of the SQW pin can be changed by programming Register A, as shown in Table 1. The SQW signal can be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PF}.
24	24	A6–A8, B1–B8, C6–C8	V_{CC}	DC Power Pin for Primary Power Supply. When V_{CC} is applied within normal limits, the device is fully accessible and data can be written and read. When V_{CC} is below V_{PF} reads and writes are inhibited.

RTC with Constant-Voltage Trickle Charger

Detailed Description

The DS12R885 is a drop-in replacement for the DS12885 RTC. The device provides 14 bytes of real-time clock/calendar, alarm, and control/status registers and 114 bytes of nonvolatile, battery-backed static RAM. A time-of-day alarm, three maskable interrupts with a common interrupt output, and a programmable square-wave output are available. The DS12R885 also operates in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power-supply failure is detected, the device automatically switches to a backup supply. The backup supply input supports either a rechargeable battery or a super cap, and includes an integrated trickle charger. The trickle charger is always enabled. The DS12R885 is accessed through a multiplexed address/data bus that supports Intel and Motorola modes.

The DS12R887 is a surface-mount package using the DS12R885 die, a 32.768kHz crystal, and a rechargeable battery. The device provides a real-time clock/calendar, one time-of-day alarm, three maskable interrupts with a common interrupt output, a programmable square wave, and 114 bytes of nonvolatile, battery-backed static RAM. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. It also operates in either 24-hour or 12-hour format with an AM/PM indicator. A precision temperature-compensated circuit monitors the status of V_{CC}. If a primary power failure is detected, the device automatically switches to a backup battery included in the package. The device is accessed through a multiplexed byte-wide interface, which supports both Intel and Motorola modes.

The DS12CR887 EDIP integrates a DS12R885 die with a crystal and battery. The charging circuit on the DS12R885 die is disabled. The battery has sufficient capacity to power the oscillator and registers for five years in the absence of V_{CC} at +25°C.

The DS12R887 BGA includes a crystal and a rechargeable battery. A fully charged battery can power the oscillator and registers (typical current at +25°C) in the absence of V_{CC} for approximately 11 days (10% of capacity consumed) or 98 days (90% capacity consumed). When the discharge depth is 10% of capacity, the battery can be recharged up to 1,000 times. If the discharge depth is 90% of capacity, the battery can be recharged up to 30 times. Thus, the life of the device would be approximately 30 years (11 days X 1,000 cycles) or 8 years (98 days x 30 cycles). Charging time to full capacity is approximately two days with V_{CC} applied.

Please consult related application notes for detailed information on battery lifetime versus depth of discharge, and expected product lifetime based upon battery cycles.

Oscillator Circuit

The DS12R885 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. An enable bit in the control register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

An external 32.768kHz oscillator can also drive the DS12R885. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			50	kΩ
Load Capacitance	C_L		12.5		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

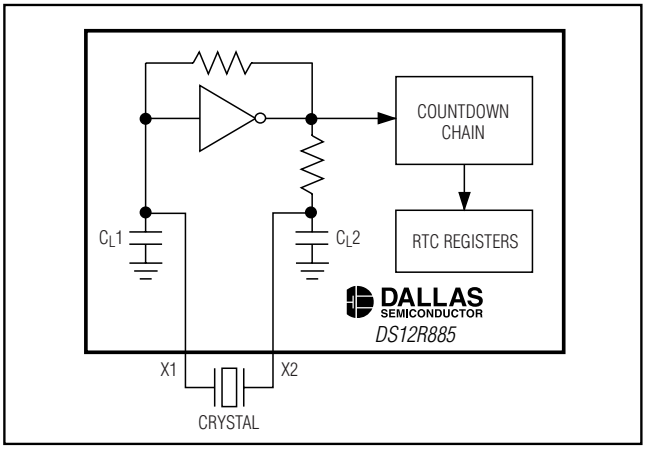


Figure 1. Oscillator Circuit Showing Internal Bias Network

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 2 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for more detailed information.

The DS12R887 and DS12CR887 are calibrated at the factory to an accuracy of ±1 minute per month at +25°C during data-retention time for the period t_{OR}.

Power-Down/Power-Up Considerations

The real-time clock continues to operate regardless of the V_{CC} input level, and the RAM and alarm memory locations remain nonvolatile. V_{BACKUP} must remain within the minimum and maximum limits when V_{CC} is not applied. When V_{CC} is applied and exceeds V_{PF} (power-fail trip point), the device becomes accessible after t_{REC}—if the oscillator is running and the oscillator countdown chain is not in reset (Register A). This time allows the system to stablize after power is applied. If the oscillator is not enabled, the oscillator-enable bit is enabled on power-up, and the device becomes immediately accessible.

Time, Calendar, and Alarm Locations

The time and calendar information is obtained by reading the appropriate register bytes. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. The contents of the 10 time, calendar, and alarm bytes can be either binary or binary-coded decimal (BCD) format.

The day-of-week register increments at midnight, incrementing from 1 through 7. The day-of-week register is used by the daylight savings function, so the value 1 is defined as Sunday. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years.

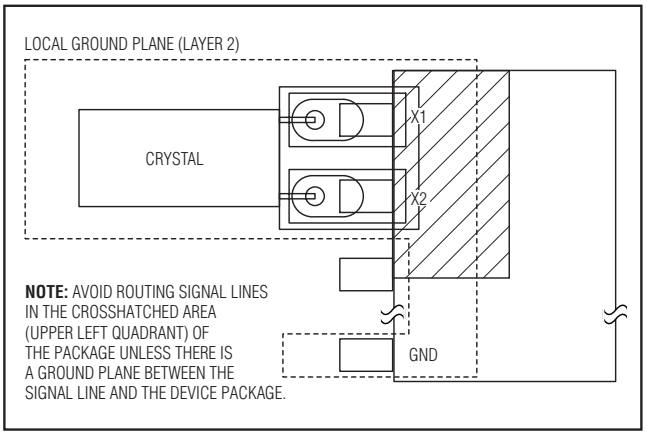


Figure 2. Layout Example

Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to logic 1 to prevent updates from occurring while access is being attempted. In addition to writing the 10 time, calendar, and alarm registers in a selected format (binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All 10 time, calendar, and alarm bytes must use the same data mode. The SET bit in Register B should be cleared after the data mode bit has been written to allow the RTC to update the time and calendar bytes. Once initialized, the RTC makes all updates in the selected mode. The data mode cannot be changed without reinitializing the 10 data bytes. Tables 2A and 2B show the BCD and binary formats of the time, calendar, and alarm locations.

The 24-12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the higher-order bit of the hours byte represents PM when it is logic 1. The time, calendar, and alarm bytes are always accessible because they are double-buffered. Once per second the seven bytes are advanced by one second and checked for an alarm condition.

If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

The three alarm bytes can be used in two ways. First, when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm-enable bit is high. In this mode, the "0" bits in the alarm registers and the corresponding time registers must always be written to 0 (Table 2A and 2B). Writing the 0 bits in the alarm and/or time registers to 1 can result in undefined operation.

The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The don't-care code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the don't-care condition when at logic 1. An alarm is generated each hour when the don't-care bits are set in the hours byte. Similarly, an alarm is generated every minute with don't-care codes in the hours and minute alarm bytes. The don't-care codes in all three alarm bytes create an interrupt every second.

All 128 bytes can be directly written or read, except for the following:

1) Registers C and D are read-only.
2) Bit 7 of register A is read-only.
3) The MSB of the seconds byte is read-only.

Table 2A. Time, Calendar, and Alarm Data Modes—BCD Mode (DM = 0)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	10 Seconds			Seconds				Seconds	00–59
01H	0	10 Seconds			Seconds				Seconds Alarm	00–59
02H	0	10 Minutes			Minutes				Minutes	00–59
03H	0	10 Minutes			Minutes				Minutes Alarm	00–59
04H	AM/PM	0	0	10 Hours	Hours				Hours	1–12 +AM/PM
	0		10 Hours							00–23
05H	AM/PM	0	0	10 Hours	Hours				Hours Alarm	1–12 +AM/PM
	0		10 Hours							00–23
06H	0	0	0	0	0	Day			Day	01–07
07H	0	0	10 Date		Date				Date	01–31
08H	0	0	0	10 Months	Month				Month	01–12
09H	10 Years				Year				Year	00–99
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH-7F	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Table 2B. Time, Calendar, and Alarm Data Modes—Binary Mode (DM = 1)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	0	0	Seconds						Seconds	00–3B
01H	0	0	Seconds						Seconds Alarm	00–3B
02H	0	0	Minutes						Minutes	00–3B
03H	0	0	Minutes						Minutes Alarm	00–3B
04H	AM/PM	0	0	0	Hours				Hours	01–0C +AM/PM 00–17
	0			Hours						
05H	AM/PM	0	0	0	Hours				Hours Alarm	01–0C +AM/PM 00–17
	0			Hours						
06H	0	0	0	0	0		Day		Day	01–07
07H	0	0	0	Date					Date	01–1F
08H	0	0	0	0	Month				Month	01–0C
09H	0	Year							Year	00–63
0AH	UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Control	—
0BH	SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Control	—
0CH	IRQF	PF	AF	UF	0	0	0	0	Control	—
0DH	VRT	0	0	0	0	0	0	0	Control	—
0EH-7F	X	X	X	X	X	X	X	X	RAM	—

X = Read/Write Bit.

Note: *Unless otherwise specified, the state of the registers is not defined when power is first applied. Except for the seconds register, 0 bits in the time and date registers can be written to 1, but may be modified when the clock updates. 0 bits should always be written to 0 except for alarm mask bits.*

Control Registers

The DS12R885 has four control registers that are accessible at all times, even during the update cycle.

Control Register A

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7: Update-In-Progress (UIP). This bit is a status flag that can be monitored. When the UIP bit is a 1, the update transfer occurs soon. When UIP is a 0, the update transfer does not occur for at least 244µs. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is 0. The UIP bit is read-only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a 1 inhibits any update transfer and clears the UIP status bit.

Bits 6, 5, and 4: DV2, DV1, DV0. These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits that turn the oscillator on and allow the RTC to keep time. A pattern of 11x enables the oscillator but holds the countdown chain in reset. The next update occurs at 500ms after a pattern of 010 is written to DV0, DV1, and DV2.

Bits 3 to 0: Rate Selector (RS3, RS2, RS1, RS0). These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected can be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user can do one of the following:

1) Enable the interrupt with the PIE bit;
2) Enable the SQW output pin with the SQWE bit;
3) Enable both at the same time and the same rate; or
4) Enable neither.

Table 3 lists the periodic interrupt rates and the square-wave frequencies that can be chosen with the RS bits. These four read/write bits are not affected by $\overline{\text{RESET}}$.

Control Register B

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7: SET. When the SET bit is 0, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to 1, any update transfer is inhibited, and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit and is not affected by $\overline{\text{RESET}}$ or internal functions of the DS12R885.

Bit 6: Periodic Interrupt Enable (PIE). The PIE bit is a read/write bit that allows the periodic interrupt flag (PF) bit in Register C to drive the $\overline{\text{IRQ}}$ pin low. When the PIE bit is set to 1, periodic interrupts are generated by driving the $\overline{\text{IRQ}}$ pin low at a rate specified by the RS3–RS0 bits of Register A. A 0 in the PIE bit blocks the $\overline{\text{IRQ}}$ output from being driven by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal DS12R885 functions, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 5: Alarm Interrupt Enable (AIE). This bit is a read/write bit that, when set to 1, permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes, including a don't-care alarm code of binary 11XXXXXX. The AF bit does not initiate the $\overline{\text{IRQ}}$ signal when the AIE bit is set to 0. The internal functions of the DS12R885 do not affect the AIE bit, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 4: Update-Ended Interrupt Enable (UIE). This bit is a read/write bit that enables the update-end flag (UF) bit in Register C to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit. UIE is not modified by any internal DS12R885 functions, but is cleared to 0 on $\overline{\text{RESET}}$.

Bit 3: Square-Wave Enable (SQWE). When this bit is set to 1, a square-wave signal at the frequency set by the rate-selection bits RS3–RS0 is driven out on the SQW pin. When the SQWE bit is set to 0, the SQW pin is held low. SQWE is a read/write bit and is cleared by $\overline{\text{RESET}}$. SQWE is low if disabled, and is high impedance when V_{CC} is below V_{PF}. SQWE is cleared to 0 on $\overline{\text{RESET}}$.

Bit 2: Data Mode (DM). This bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or $\overline{\text{RESET}}$. A 1 in DM signifies binary data, while a 0 in DM specifies BCD data.

Bit 1: 24/12. The 24/12 control bit establishes the format of the hours byte. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or $\overline{\text{RESET}}$.

Bit 0: Daylight Savings Enable (DSE). This bit is a read/write bit that enables two daylight savings adjustments when DSE is set to 1. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. When DSE is enabled, the internal logic tests for the first/last Sunday condition at midnight. If the DSE bit is not set when the test occurs, the daylight savings function does not operate correctly. These adjustments do not occur when the DSE bit is 0. This bit is not affected by internal functions or $\overline{\text{RESET}}$.

Control Register C

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

Bit 7: Interrupt Request Flag (IRQF). This bit is set to 1 when any of the following are true:

PF = PIE = 1

AF = AIE = 1

UF = UIE = 1

Any time the IRQF bit is 1, the $\overline{IRQ}$ pin is driven low. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 6: Periodic Interrupt Flag (PF). This bit is read-only and is set to 1 when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to 1 independent of the state of the PIE bit. When both PF and PIE are 1s, the $\overline{IRQ}$ signal is active and sets the IRQF bit. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 5: Alarm Interrupt Flag (AF). A 1 in the AF bit indicates that the current time has matched the alarm time. If the AIE bit is also 1, the $\overline{IRQ}$ pin goes low and a 1 appears in the IRQF bit. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bit 5: Update-Ended Interrupt Flag (UF). This bit is set after each update cycle. When the UIE bit is set to 1, the 1 in UF causes the IRQF bit to be a 1, which asserts the $\overline{IRQ}$ pin. This bit can be cleared by reading Register C or with a $\overline{RESET}$.

Bits 3 to 0: Unused. These bits are unused in Register C. These bits always read 0 and cannot be written.

Control Register D

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

Bit 7: Valid RAM and Time (VRT). This bit indicates the condition of the battery connected to the V_{BACKUP} pin. This bit is not writeable and should always be 1 when read. If a 0 is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

Bits 6 to 0: Unused. The remaining bits of Register D are not usable. They cannot be written and they always read 0.

Nonvolatile RAM (NV RAM)

The 114 general-purpose NV RAM bytes are not dedicated to any special function within the DS12R885. They can be used by the processor program as battery-backed memory and are fully available during the update cycle.

Interrupts

The DS12R885 includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected for rates from 500ms to 122µs. The update-ended interrupt can be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are to be used. Three bits in Register B enable the interrupts. Writing a logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A 0 in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the interrupt initiating the event may have occurred earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit that software can interrogate as necessary. When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits that are set remain stable throughout the read cycle. All bits that are set (high) are cleared when read, and new interrupts that are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each used flag bit should be examined when Register C is read to ensure that no interrupts are lost.

The second flag bit method is used with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits set. The IRQF bit in Register C is a 1 whenever the $\overline{IRQ}$ pin is driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic 1 in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the DS12R885. The act of reading Register C clears all active flag bits and the IRQF bit.

Oscillator Control Bits

When the DS12R887 and DS12CR887 are shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in a system.

A pattern of 010 in bits 4 to 6 of Register A turns the oscillator on and enables the countdown chain. A pattern of 11x (DV2 = 1, DV1 = 1, DV0 = X) turns the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 to 6 keep the oscillator off.

Square-Wave Output Selection

Thirteen of the 15 divider taps are made available to a 1-of-16 multiplexer, as shown in the functional diagram. The square-wave and periodic-interrupt generators share the output of the multiplexer. The RS0–RS3 bits in Register A establish the output frequency of the multiplexer (see Table 1). Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square-wave enable bit, SQWE.

Periodic Interrupt Selection

The periodic interrupt causes the $\overline{IRQ}$ pin to go to an active state from once every 500ms to once every 122µs. This function is separate from the alarm interrupt, which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits that select the square-wave frequency (Table 1). Changing the Register A bits affects the square-wave frequency and the periodic-interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square-wave output. Similarly, the PIE bit in Register B enables the periodic interrupt. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 3. Periodic Interrupt Rate and Square-Wave Output Frequency

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625ms	256Hz
0	0	1	0	7.8125ms	128Hz
0	0	1	1	122.070µs	8.192kHz
0	1	0	0	244.141µs	4.096kHz
0	1	0	1	488.281µs	2.048kHz
0	1	1	0	976.5625µs	1.024kHz
0	1	1	1	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz
1	1	0	1	125ms	8Hz
1	1	1	0	250ms	4Hz
1	1	1	1	500ms	2Hz

Update Cycle

The DS12R885 executes an update cycle once per second regardless of the SET bit in Register B. When the SET bit in Register B is set to 1, the user copy of the double-buffered time, calendar, and alarm bytes is frozen and does not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy independent of reading or writing the time, calendar, and alarm buffers, and also guarantees that time and calendar information is consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a don't-care code is present in all three positions.

There are three methods that can handle RTC access that avoid any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle that indicates over 999ms is available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit pulses once per second. After the UIP bit goes high, the update transfer occurs 244µs later. If a low is read on the UIP bit, the user has at least 244µs before the time/calendar data is changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (Figure 3). Periodic interrupts that occur at a rate greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within 1($t_{PI/2}$ + t_{BUC}) to ensure that data is not read during the update cycle.

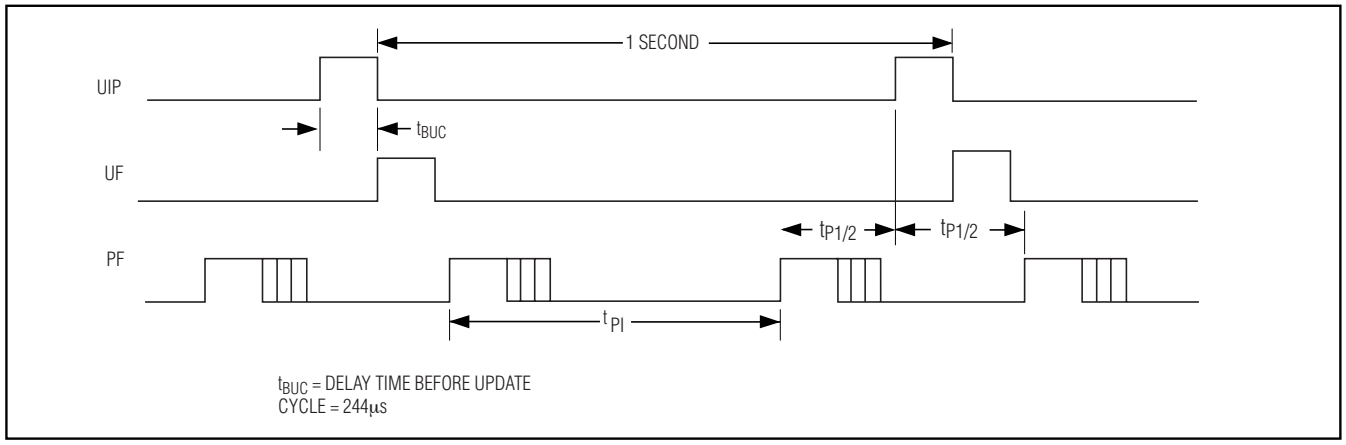


Figure 3. UIP and Periodic Interrupt Timing

Handling, PC Board Layout, and Assembly

The EDIP and BGA packages contain a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

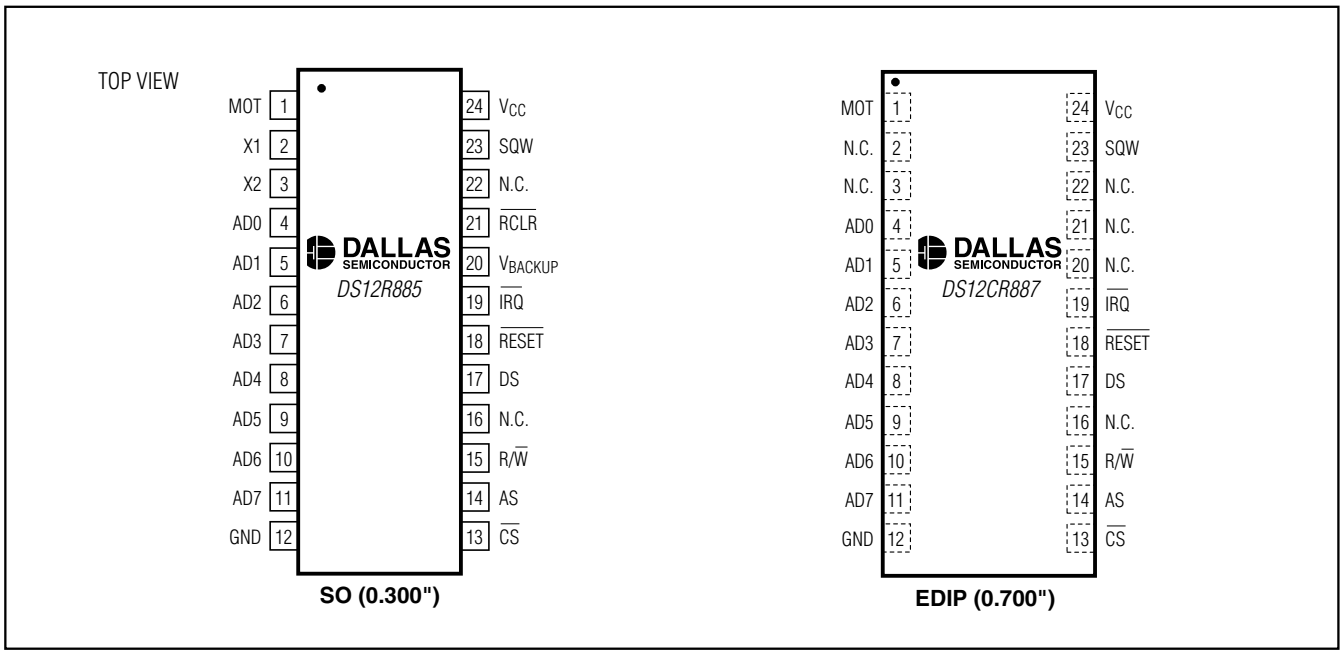
The BGA package can be reflowed as long as the following conditions are met:

1. Preheating (below 160°C) is within 90 seconds.
2. Maximum time above 150°C is less than 180 seconds.
3. Maximum time above 170°C is less than 100 seconds.
4. Maximum time above 200°C is less than 60 seconds.
5. Maximum time above 220°C is less than 30 seconds.
6. Peak temperature is less than or equal to 230°C.

Exposure to reflow is limited to two times maximum.

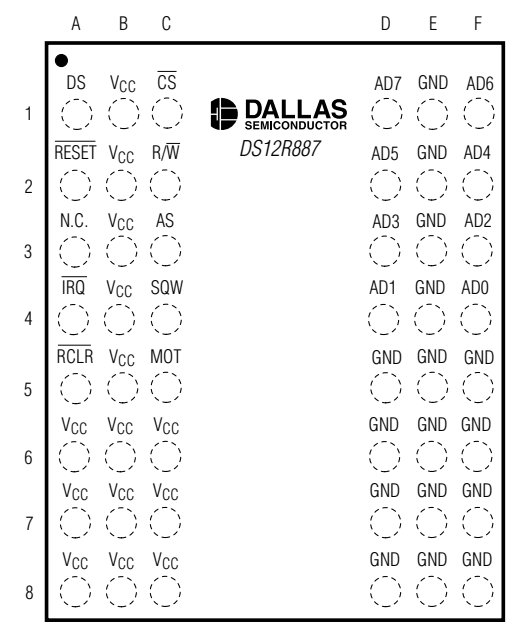
Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020B standard for Moisture-Sensitive Device (MSD) classifications.

Pin Configurations



RTC with Constant-Voltage Trickle Charger

Pin Configurations (continued)



48 BGA

Thermal Information

PACKAGE	THETA-JA (°C/W)	THETA-JC (°C/W)
SO	105	22

Chip Information

TRANSISTOR COUNT: 17,061

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.