

EC103D1

Sensitive gate thyristor

Rev. 01 — 1 November 2001

Product data

1. Description

Very sensitive gate thyristor intended to be interfaced directly to low power gate trigger circuits, with very low drive current capability.

Product availability:

EC103D1 in SOT54 (TO-92).

2. Features

- Blocking voltage to 400 V
- On-state RMS current to 0.8 A
- Ultra low gate trigger current
- Low cost package.

3. Applications

- Earth leakage circuit breakers
- Solid state relays
- General purpose switching.

4. Pinning information

Table 1: Pinning - SOT54 (TO-92), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	anode (a)		
2	gate (g)		
3	cathode (k)		

SOT54 (TO-92)

5. Quick reference data

Table 2: Quick reference data

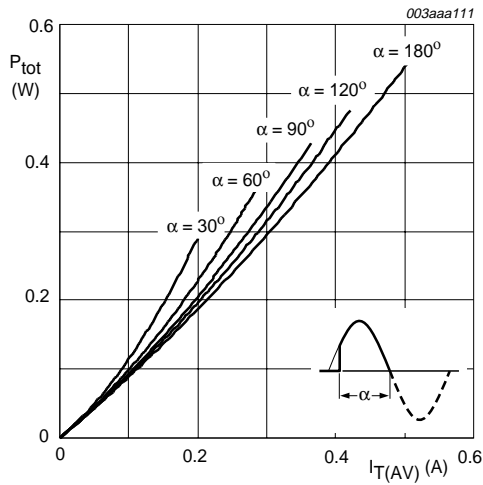
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage	$25\text{ °C} \leq T_j \leq 125\text{ °C}$	-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{T(RMS)}$	on-state current (RMS value)		-	0.8	A
I_{TSM}	non-repetitive peak on-state current		-	8.0	A

6. Limiting values

Table 3: Limiting values

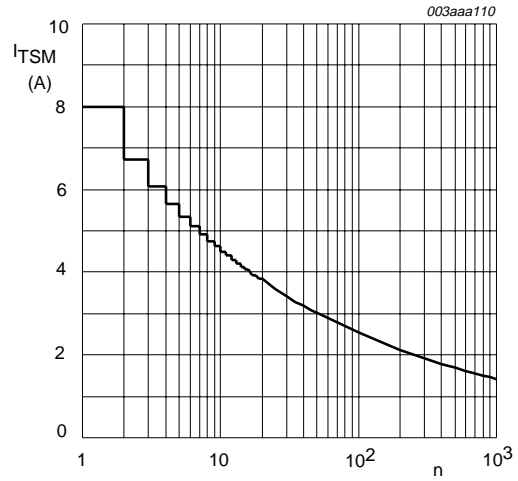
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage	$25\text{ °C} \leq T_j \leq 125\text{ °C}$	-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$	-	0.5	A
$I_{T(RMS)}$	on-state current (RMS value)	all conduction angles	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge			
		$t = 10\text{ ms}$	-	8.0	A
		$t = 8.3\text{ ms}$	-	9.0	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	0.32	A ² s
di_T/dt	rate of rise on-state current	$I_{TM} = 2.0\text{ A}$; $I_G = 10\text{ mA}$; $di_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	peak gate current		-	1.0	A
V_{GM}	peak gate voltage		-	5.0	V
V_{RGM}	peak reverse gate voltage		-	5.0	V
P_{GM}	peak gate power		-	2.0	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	°C
T_j	operating junction temperature		-	+125	°C



α = conduction angle

Fig 1. Maximum on-state dissipation as a function of average on-state current; typical values.



n = number of cycles at $f = 50$ Hz

Fig 2. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

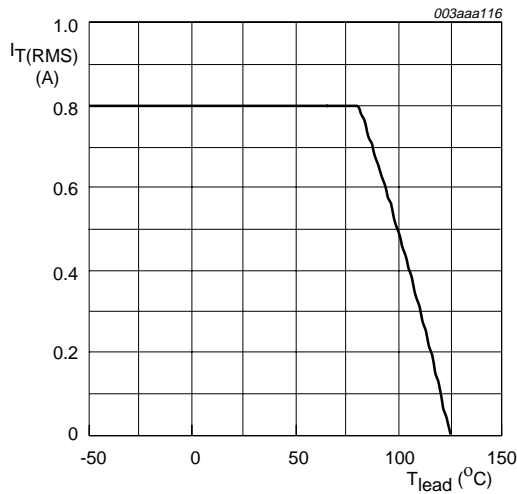
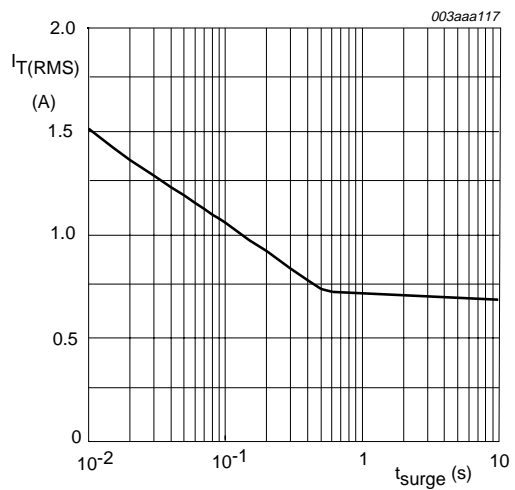


Fig 3. Maximum permissible on-state current (RMS value) as a function of lead temperature; typical values.



$f = 50$ Hz; $T_{lead} \leq 83^\circ\text{C}$.

Fig 4. Maximum permissible repetitive on-state current (RMS value) as a function of surge duration for sinusoidal currents; typical values.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead		80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; lead length = 4 mm	150	K/W

7.1 Transient thermal impedance

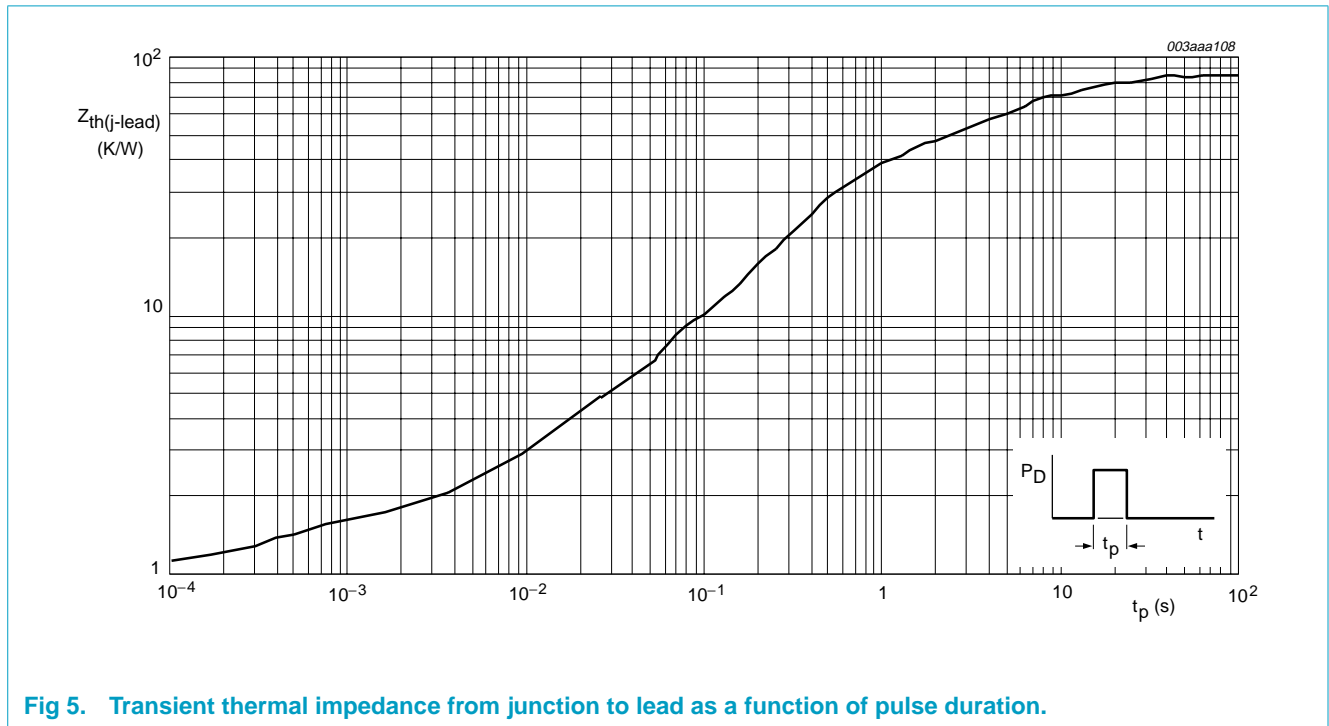


Fig 5. Transient thermal impedance from junction to lead as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; gate open circuit	-	3	12	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$	-	2	6	mA
I_H	holding current		-	2	5	mA
V_T	on-state voltage	$I_T = 1.0\text{ A}$	-	1.2	1.35	V
V_{GT}	gate trigger voltage	$I_T = 10\text{ mA}$; gate open circuit				
		$V_D = 12\text{ V}$	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	0.2	0.3	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$;	-	50	100	μA
I_R	reverse current	$T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$	-	50	100	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_D = 0.67 V_{DRM(max)}$; $T_{case} = 125\text{ °C}$; exponential waveform; $R_{GK} = 1\text{ k}\Omega$	-	25	-	$\text{V}/\mu\text{s}$
t_{gt}	gate controlled turn-on time	$I_{TM} = 2.0\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	commutated turn-off time	$V_D = 0.67 V_{DRM(max)}$; $T_j = 125\text{ °C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $dI_{TM}/dt = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$	-	100	-	μs

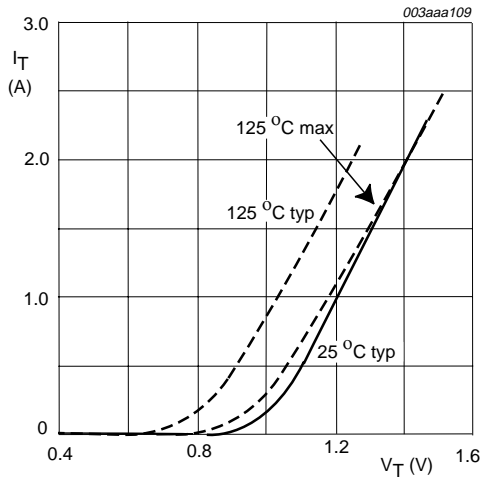
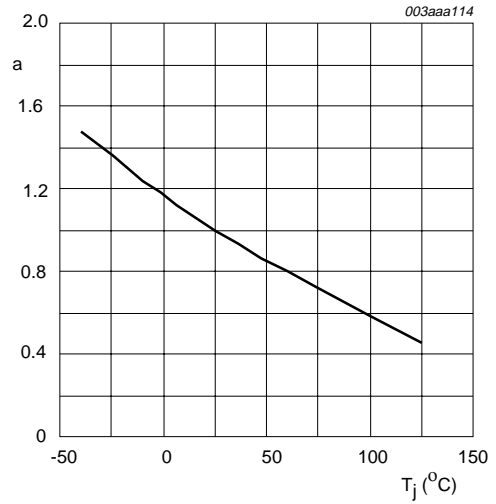
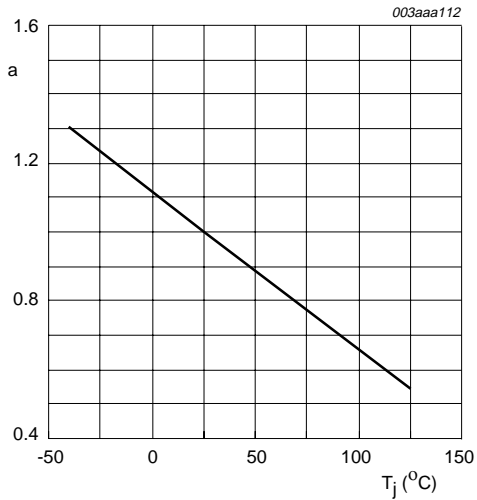


Fig 6. On-state current as a function of on-state voltage; typical and maximum values.



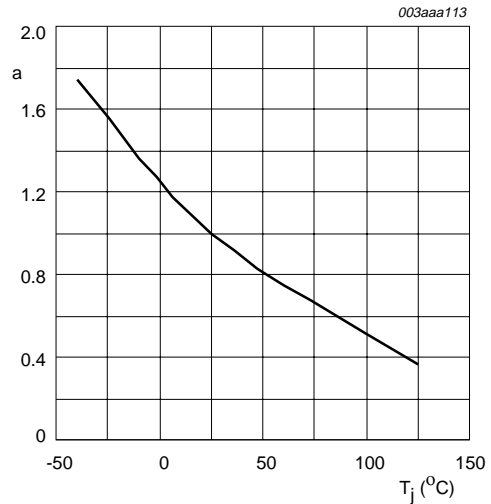
$$a = \frac{I_{L(Tj)}}{I_{L(25^{\circ}\text{C})}}$$

Fig 7. Normalized latching current as a function of junction temperature; typical values.



$$a = \frac{V_{GT(Tj)}}{V_{GT(25^{\circ}\text{C})}}$$

Fig 8. Normalized gate trigger voltage as a function of junction temperature; typical values.



$$a = \frac{I_{GT(Tj)}}{I_{GT(25^{\circ}\text{C})}}$$

Fig 9. Normalized gate trigger current as a function of junction temperature; typical values.

9. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

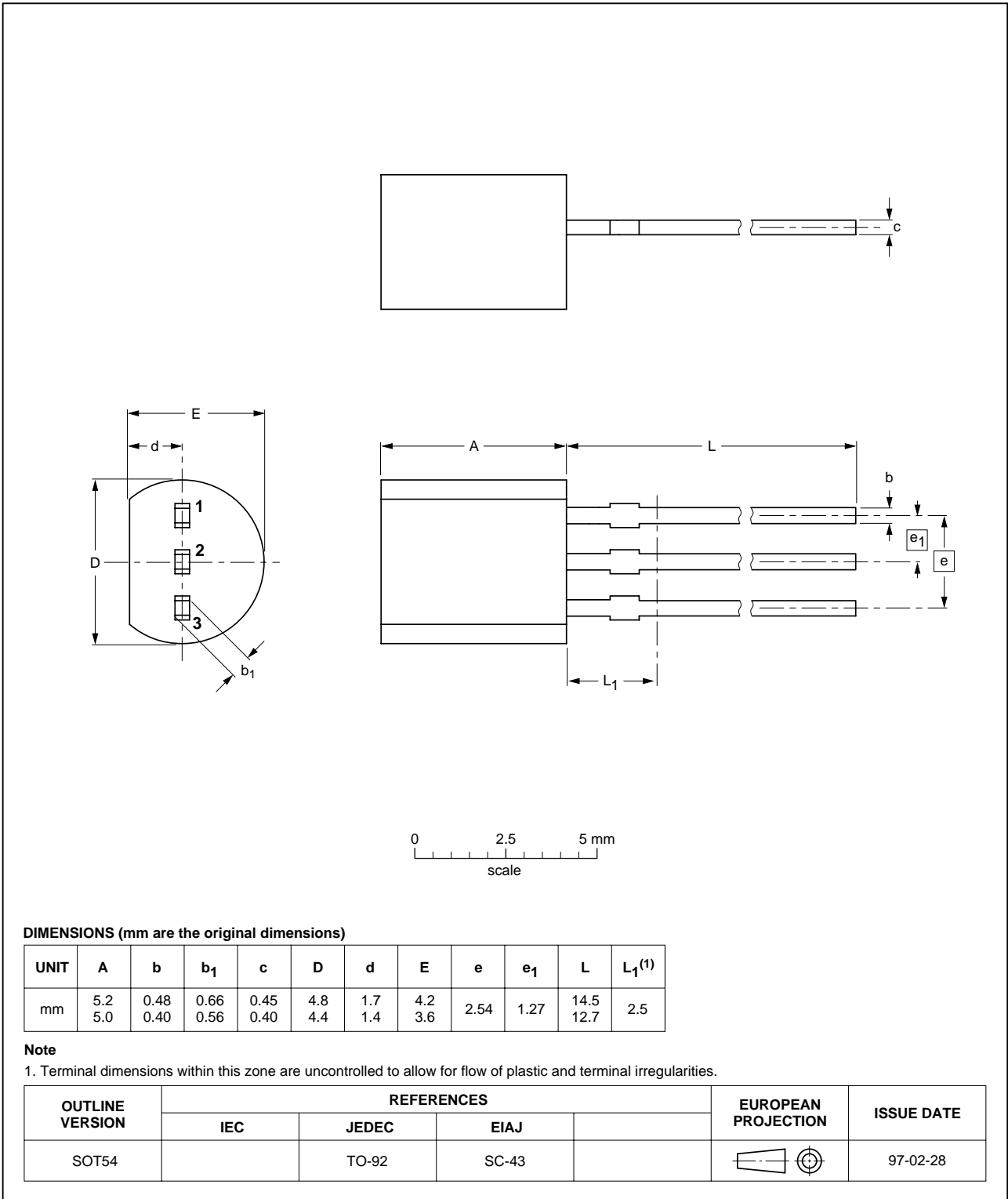


Fig 10. SOT54 (TO-92).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20011101	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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