



# MP7502

## CMOS 4-CHANNEL ANALOG MULTIPLEXERS

T-51-11

### FEATURES

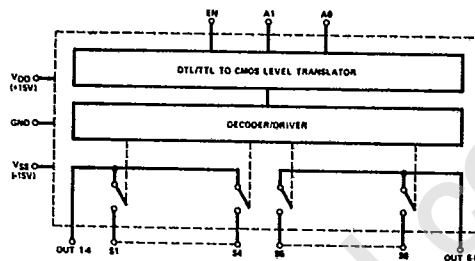
- DTL/TTL/CMOS Direct Interface
- Power Dissipation: 30μW
- R<sub>ON</sub>: 170Ω
- Output "Enable" Control

### GENERAL DESCRIPTION

The MP7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output busses to two of 8 inputs.

The MP7502 is an excellent example of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

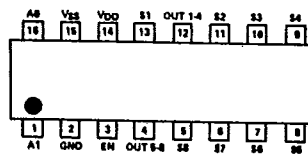
### FUNCTIONAL DIAGRAM



### TRUTH TABLE

MP7502			
A <sub>1</sub>	A <sub>0</sub>	E <sub>N</sub>	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

### PIN CONFIGURATION (Top View)



See Section 7 for Ordering Information

### ABSOLUTE MAXIMUM RATINGS

(T<sub>A</sub> = +25°C unless otherwise noted.)

- V<sub>DD</sub> to GND ..... +17V
- V<sub>SS</sub> to GND ..... -17V
- V Between Any Switch Terminals ..... 25V
- Switch Current (I<sub>S</sub>, Continuous) ..... 35mA
- Switch Current (I<sub>S</sub>, Surge) ..... 50mA
- 1mS duration, 10% duty cycle ..... 50mA
- Digital Input Voltage Range ..... V<sub>DD</sub> to GND

### Power Dissipation (Package)\*

- 16 Pin Ceramic DIP\*\* ..... 900mW
- 16 Pin Plastic DIP\*\*\* ..... 470mW

- \* Device mounted with all leads soldered or welded to PC board
- \*\* Derate 12mW/°C above +75°C
- \*\*\* Derate 6.5mW/°C above +25°C

### Operating Temperature

- Plastic ..... 0°C to +70°C
- Ceramic (J, K versions) ..... -25°C to +85°C
- Ceramic (S version) ..... -55°C to +125°C
- Storage Temperature ..... -65°C to +150°C

### CAUTION:

1. Do not apply voltages higher than V<sub>DD</sub> and V<sub>SS</sub> to any other terminal, especially when V<sub>SS</sub> = V<sub>DD</sub> = 0V all other pins should be set at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

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**SPECIFICATIONS**  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$  unless otherwise noted.**3**

PARAMETER Note 1	VERSION Note 2	SWITCH CONDITION	25°C			UNITS	TEST CONDITIONS
			TYP.	MIN	MAX		
<b>ANALOG SWITCH</b>							
RON	All	ON	300		375	$\Omega$	$-10\text{ V} < V_S < +10\text{ V}$
RON vs. VS	All	ON	2C			%	$I_S = 1.0\text{ mA}$
RON vs. Temperature	All	ON	0.5			%/°C	
$\Delta$ RON Between Switches	All	ON	4			%	$V_S = 0\text{ V}$ , $I_S = 1.0\text{ mA}$
RON vs. Temperature Between Switches	All	ON	$\pm 0.01$			%/°C	
IS	J, K	OFF	2		50	nA	$V_S = -10\text{ V}$ , $V_{OUT} = +10\text{ V}$ and $V_S = +10\text{ V}$ , $V_{OUT} = -10\text{ V}$
	S	OFF	0.5		50	nA	
IOUT	J, K	OFF	5		125	nA	$V_S = -10\text{ V}$ , $V_{OUT} = +10\text{ V}$ and $V_S = +10\text{ V}$ , $V_{OUT} = -10\text{ V}$ Enable LOW
	S	OFF	3		125	nA	
IOUT - IS	J, K	ON	7		175	nA	$V_S = 0$
	S	ON	3.5		175	nA	
<b>DIGITAL CONTROL</b>							
VINL	All				0.8	V	
VINH	J			3.0		V	Note 3
	K, S			2.4		V	
IINL or IINH	All		10			nA	
CIN	All		3			pF	
<b>DYNAMIC CHARACTERISTICS</b>							
TON	All		0.8			$\mu\text{s}$	$V_{IN} = 0$ to $+5.0\text{ V}$ (See Test Circuit 2, Page 19)
TOFF	All		0.8			$\mu\text{s}$	
CS	All	OFF	5			pF	
COUT	All	OFF	15			pF	
CS-OUT	All	OFF	0.5			pF	
CSS Between Any Two Switches	All	OFF	0.5			pF	
<b>POWER SUPPLY</b>							
IDD	J, K		100			$\mu\text{A}$	All Digital Inputs Low
	J, K		100			$\mu\text{A}$	
	S		500	500		$\mu\text{A}$	
	S		500	500		$\mu\text{A}$	
ISS	J, K		500			$\mu\text{A}$	All Digital Inputs High
	J, K		100			$\mu\text{A}$	
	S		800	800		$\mu\text{A}$	
	S		800	800		$\mu\text{A}$	

**NOTES:**

- Specifications subject to change without notice.
- JN, KN versions specified for  $0^\circ\text{C}$  to  $+70^\circ\text{C}$ ; JD, KD versions for  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$ ; and SD versions for  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .
- A pullup resistor, typically 1-2 k $\Omega$  is required to make the MP7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.