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μPD78238 Family (μPD78233/234/237/238/P238) 8-Bit, K-Series Microcontrollers With A/D and D/A Converters, Real-Time Output Ports

June 1993

Description

The μPD78233, μPD78234, μPD78237, μPD78238, and μPD78P238 are members of the K-Series® of microcontrollers and are designed for real-time embedded control applications. These 8-bit, single-chip microcontrollers have a minimum instruction time of 333 ns at 12 MHz (500 ns for the μPD78233/237). They feature 8-bit hardware multiply and divide instructions, four banks of main registers, an advanced interrupt handling facility, a powerful set of memory mapped on-chip peripherals, and the ability to address up to 1M bytes of external data memory. On board memory includes 640 or 1024 bytes of RAM, 16K or 32K bytes of mask ROM, or 32K bytes of UV EPROM or one-time programmable (OTP) ROM.

The advanced interrupt handling facility provides two levels of programmable hardware priority control and two separate methods of servicing interrupt requests: vectored and macro service. The macro service facility reduces the overhead involved in servicing peripheral interrupts by transferring data between the memory-mapped special function registers (SFRs) and memory without the use of time consuming interrupt service routines. In addition, the macro service facility can be initialized to automatically alter timer compare register values or to repeatedly output a prespecified pattern at a fixed or variable rate. By using macro service to control the real-time output ports, the μPD78238 family can easily and accurately drive two independent stepper motors.

The combination of the macro service facility, four banks of main registers, extended data memory address space, and powerful on-chip peripherals makes these devices ideal for applications in office automation, communication, HVAC, and industrial control.

Features

- Complete single-chip microcontroller
  - 8-bit ALU
  - Program memory (ROM)
    μPD78233/237: ROMless
    μPD78234: 16K bytes
    μPD78238/P238: 32K bytes
  - Data memory (RAM)
    μPD78233/234: 640 bytes
    μPD78237/238/P238: 1024 bytes
- Powerful instruction set
  - 8-bit unsigned multiply and divide
  - 16-bit arithmetic instructions
  - 1-bit and 8-bit logic instructions
- Minimum instruction time
  - 333 ns at 12 MHz (μPD78234/238/P238)
  - 500 ns at 12 MHz (μPD78233/237)
- Memory expansion
  - 8085 bus-compatible
  - 64K program address space
  - 1M data address space
- Large I/O capacity
  - Up to 64 I/O port lines on μPD78234/238/P238
  - Up to 46 I/O port lines on μPD78233/237
  - Software programmable pullup resistors
- Memory-mapped on-chip peripherals (special function registers)
- Timer/counter unit
  - 16-bit timer 0:
    Two 16-bit compare registers
    One 16-bit capture register
    One external interrupt/capture line
  - 8-bit timer 1:
    One 8-bit compare register
    One 8-bit capture/compare register
    One external interrupt/capture line
  - 8-bit timer/counter 2:
    Two 8-bit compare registers
    One 8-bit capture register
    One external interrupt/capture line
    One external event counter line
  - 8-bit timer 3:
    One 8-bit compare register
- Pulse-width modulated (PWM) outputs
  - Two 12-bit precision hardware controlled
  - Four 8-bit precision timer controlled
- Two 4-bit (or one 8-bit) real-time output ports
- Eight-channel 8-bit A/D converter
- Two-channel 8-bit D/A converter
- Programmable priority interrupt controller (two levels)
- Two methods of interrupt service
  - Vectored interrupts
  - Macro service mode with choice of three different types

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Features (cont)

- Two-channel serial communication interface
  - — Asynchronous serial interface (UART)
    Dedicated baud rate generator
  - — Clock-synchronized interface
    Full-duplex, three-wire mode
    NEC serial bus interface (SBI) mode
- Refresh output for pseudostatic RAM
- STOP and HALT standby functions
- 5-volt CMOS technology

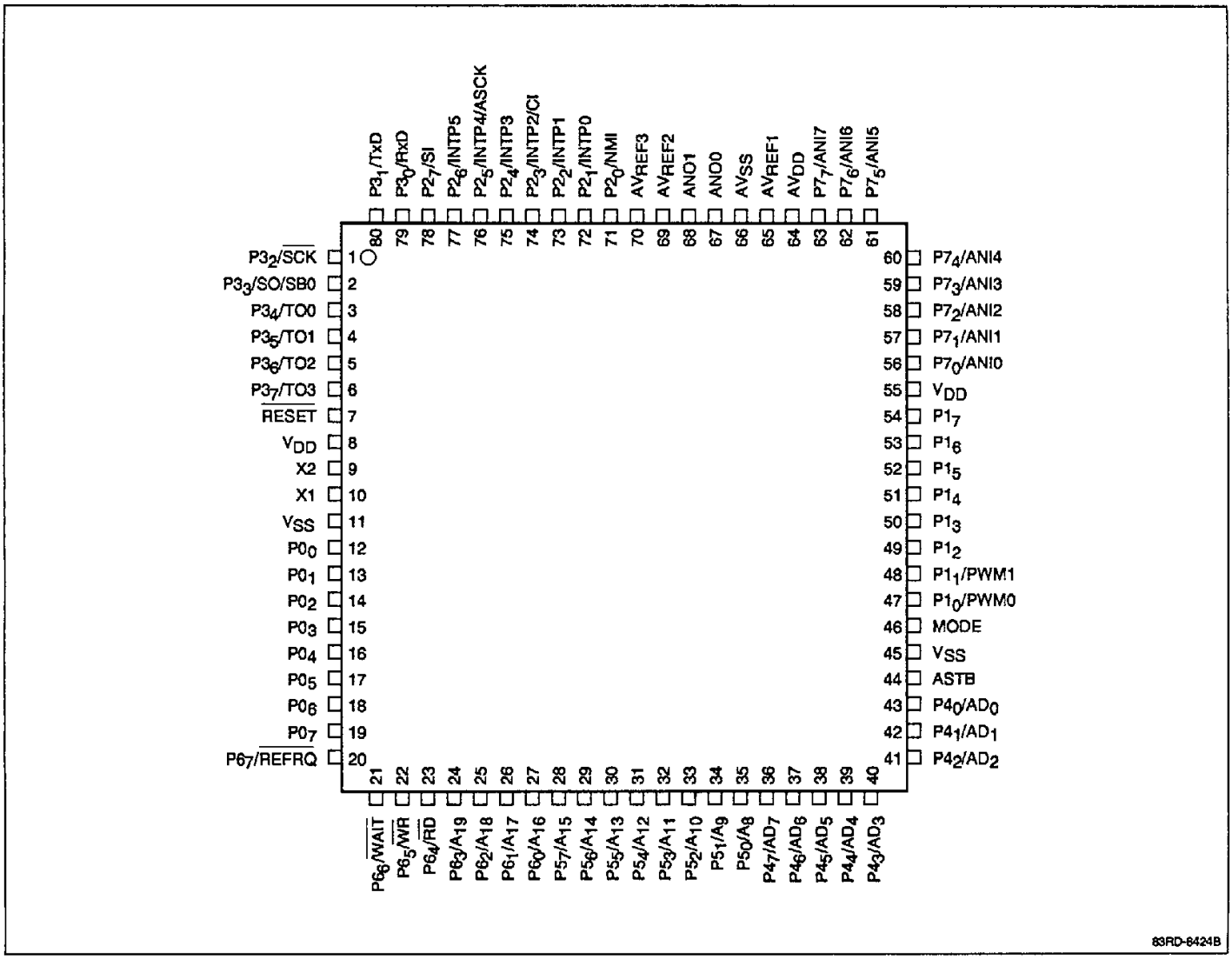
Ordering Information

Part Number	ROM	Package	Package Drawing
μPD78233GC	ROMless	80-pin plastic QFP	S80GC-65-3B9-1
μPD78234GC-xxx	16K mask ROM		
μPD78237GC	ROMless		
μPD78238GC-xxx	32K mask ROM		
μPD78P238GC	32K OTP ROM		
μPD78233GJ	ROMless	94-pin plastic QFP	S94GJ-80-5BG-1
μPD78234GJ-xxx	16K mask ROM		
μPD78237GJ	ROMless		
μPD78238GJ-xxx	32K mask ROM		
μPD78P238GJ	32K OTP ROM		
μPD78233LQ	ROMless	84-pin PLCC	P84L-50A3-1
μPD78234LQ-xxx	16K mask ROM		
μPD78237LQ	ROMless		
μPD78238LQ-xxx	32K mask ROM		
μPD78P238LQ	32K OTP ROM		
μPD78P238KF	32K UV EPROM	94-pin ceramic LCC with window	X94KW-80A

Note: xxx indicates ROM code suffix.

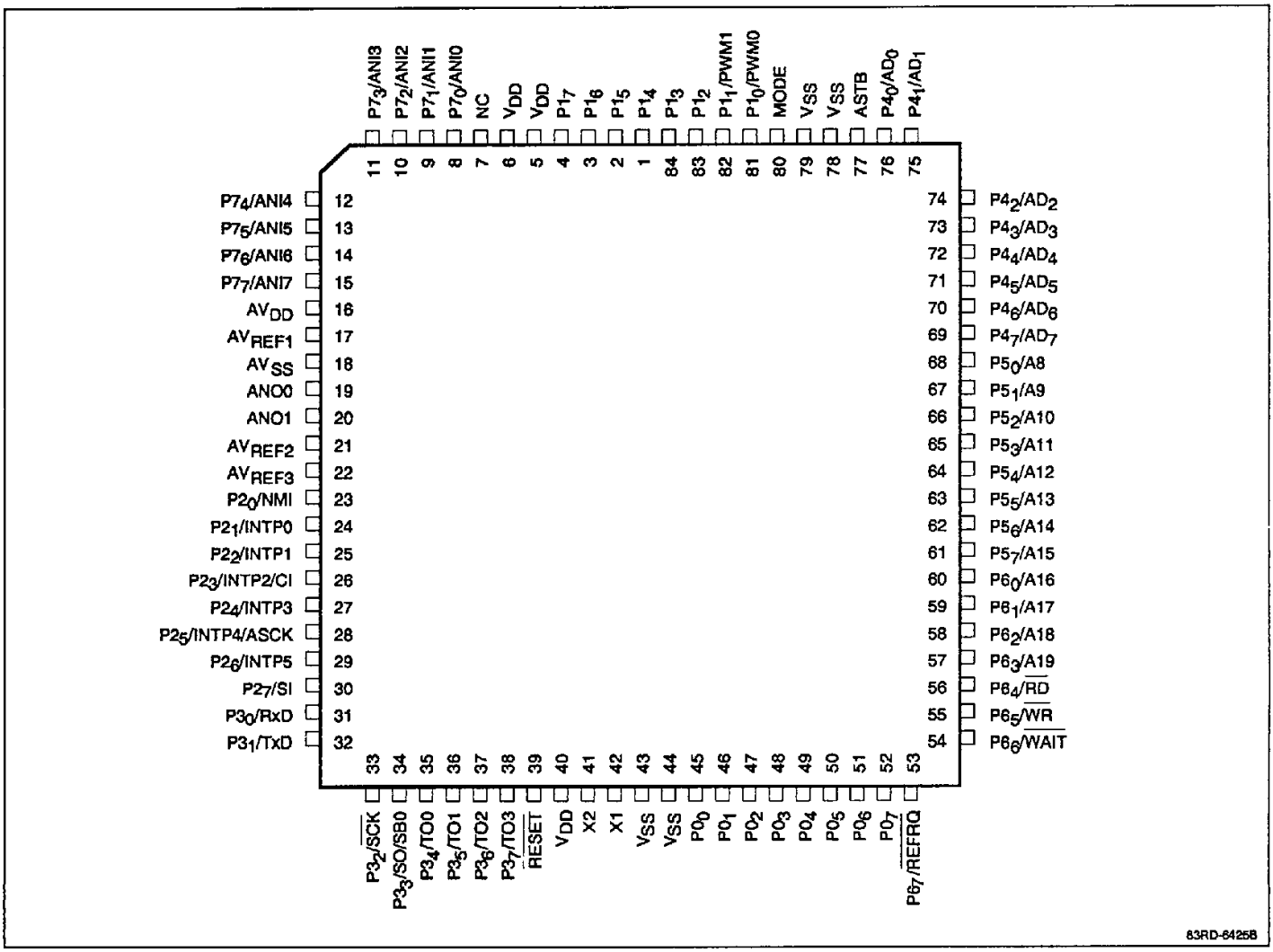
Pin Configurations

80-Pin Plastic QFP



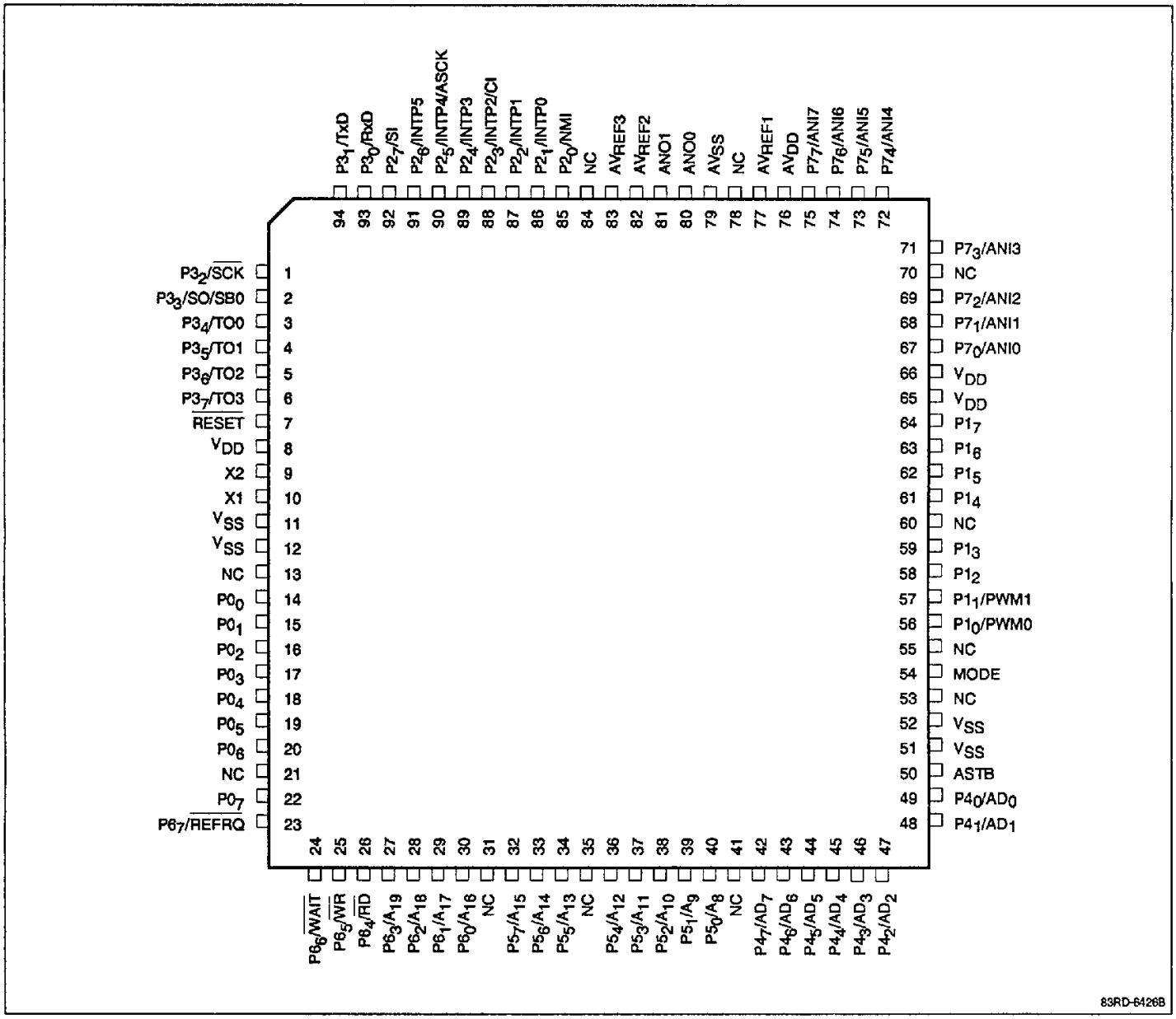
Pin Configurations (cont)

84-Pin PLCC (Plastic Leaded Chip Carrier)



Pin Configurations (cont)

94-Pin Plastic QFP and Ceramic LCC with Window



Pin Functions; Normal Operating Mode

Symbol	First Function	Symbol	Second Function
$P0_0$ - $P0_7$	Port 0; 8-bit tristate output port/real time output port		
$P1_0$ $P1_1$	Port 1; 8-bit, bit-selectable tristate input/output port	PWM0 PWM1	Pulse-width modulated outputs
$P1_2$ - $P1_7$		—	
$P2_0$	Port 2; 8-bit input port	NMI	External nonmaskable interrupt
$P2_1$ $P2_2$		INTP0 INTP1	Maskable external interrupts
$P2_3$		INTP2 CI	Maskable external interrupt External clock input to timer/counter 2
$P2_4$		INTP3	Maskable external interrupt
$P2_5$		INTP4 ASCK	Maskable external interrupt Asynchronous serial clock input
$P2_6$		INTP5	Maskable external interrupt
$P2_7$		SI	Serial data input for three-wire serial I/O mode
$P3_0$	Port 3; 8-bit, bit-selectable tristate input/output port	RxD	Asynchronous serial receive data input
$P3_1$		TxD	Asynchronous serial transmit data input
$P3_2$		$\overline{SCK}$	Serial shift clock input/output
$P3_3$		SO SBO	Serial data output for three-wire serial I/O mode I/O bus for NEC serial bus interface (SBI)
$P3_4$ - $P3_7$		TO0 - TO3	Timers T0 to T3 outputs
$P4_0$ - $P4_7$	Port 4; 8-bit tristate input/output port	AD_0 - AD_7	Low-order 8-bit multiplexed address/data bus
$P5_0$ - $P5_7$	Port 5; 8-bit, bit-selectable tristate input/output port	A_8 - A_{15}	High-order 8-bit address bus
$P6_0$ - $P6_3$	Port 6; 4-bit output port	A_{16} - A_{19}	Extended memory address bus
$P6_4$	Port 6; 4-bit, bit-selectable tristate input/output port	$\overline{RD}$	External memory read strobe
$P6_5$		$\overline{WR}$	External memory write strobe
$P6_6$		$\overline{WAIT}$	External memory wait signal input
$P6_7$		$\overline{REFRQ}$	Refresh pulse output used by external pseudostatic memory
$P7_0$ - $P7_7$	Port 7; 8-bit input port	ANI0 - ANI7	Analog voltage input to A/D converter
ANO0, ANO1	Analog voltage output from D/A converter		
ASTB	Address strobe output used to latch the low-order 8 address for external memory		
$\overline{RESET}$	External system reset input		
MODE	Internal ROM or external memory control signal input. A low-level input selects internal ROM. A high-level input selects external memory. The μPD78234/238 can be used in ROMless mode by setting the MODE pin high. However, the μPD78P238 cannot be used in ROMless mode and its MODE pin must only be set low.		
X1	Crystal/ceramic resonator connection or external clock input		
X2	Crystal/ceramic resonator connection or inverse of external clock		
AV_{REF1}	A/D converter reference voltage		

Pin Functions; Normal Operating Mode (cont)

Symbol	First Function	Symbol	Second Function
AV_{REF2}, AV_{REF3}	D/A converter reference voltages		
AV_{DD}	A/D converter power supply		
AV_{SS}	A/D converter ground		
V_{DD}	+5 volt power supply input		
V_{SS}	Power supply ground		
NC	No connection		

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The μPD78238 family CPU features 8- and 16-bit arithmetic including an 8 x 8-bit unsigned multiply and 16 x 8-bit unsigned divide (producing a 16-bit quotient and an 8-bit remainder). The multiply executes in 3.67 μs and the divide in 12.36 μs at 12 MHz (4.00 and 12.69 μs respectively for μPD78233/237).

A CALLT vector table and a CALLF program area decrease the number of bytes in the call instructions for commonly used subroutines. A 1-byte call instruction (CALLT) can access up to 32 subroutines through the addresses contained in the CALLT vector table. A 2-byte call instruction (CALLF) can access any routine beginning at a specific address in the CALLF area.

The internal system clock (f_{CLK}) is generated by dividing the oscillator frequency by two. Therefore, at the maximum oscillator frequency of 12 MHz, the internal system clock is 6 MHz. The minimum instruction execution time for an instruction fetched from internal ROM is 333 ns (500 ns when fetched from external memory).

Memory Space

The μPD78238 family has a 1M byte address space (see figure 1). The first 64K bytes of this address space (00000H-0FFFFH) can be used as both program and data memory. The remaining 960K bytes of this address space (10000H-FFFFFH) can only be used as data memory and is known as expanded memory.

Block Diagram

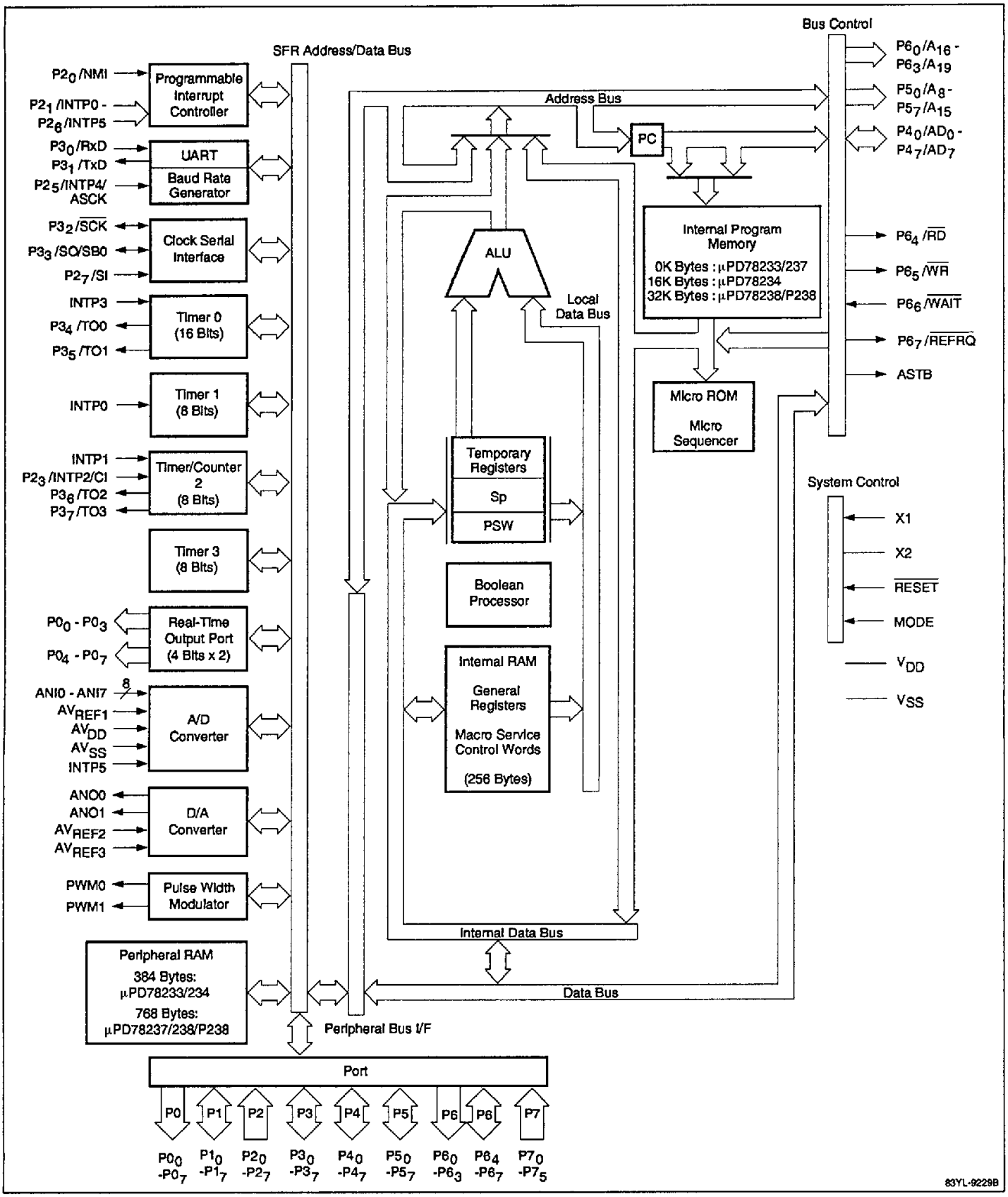
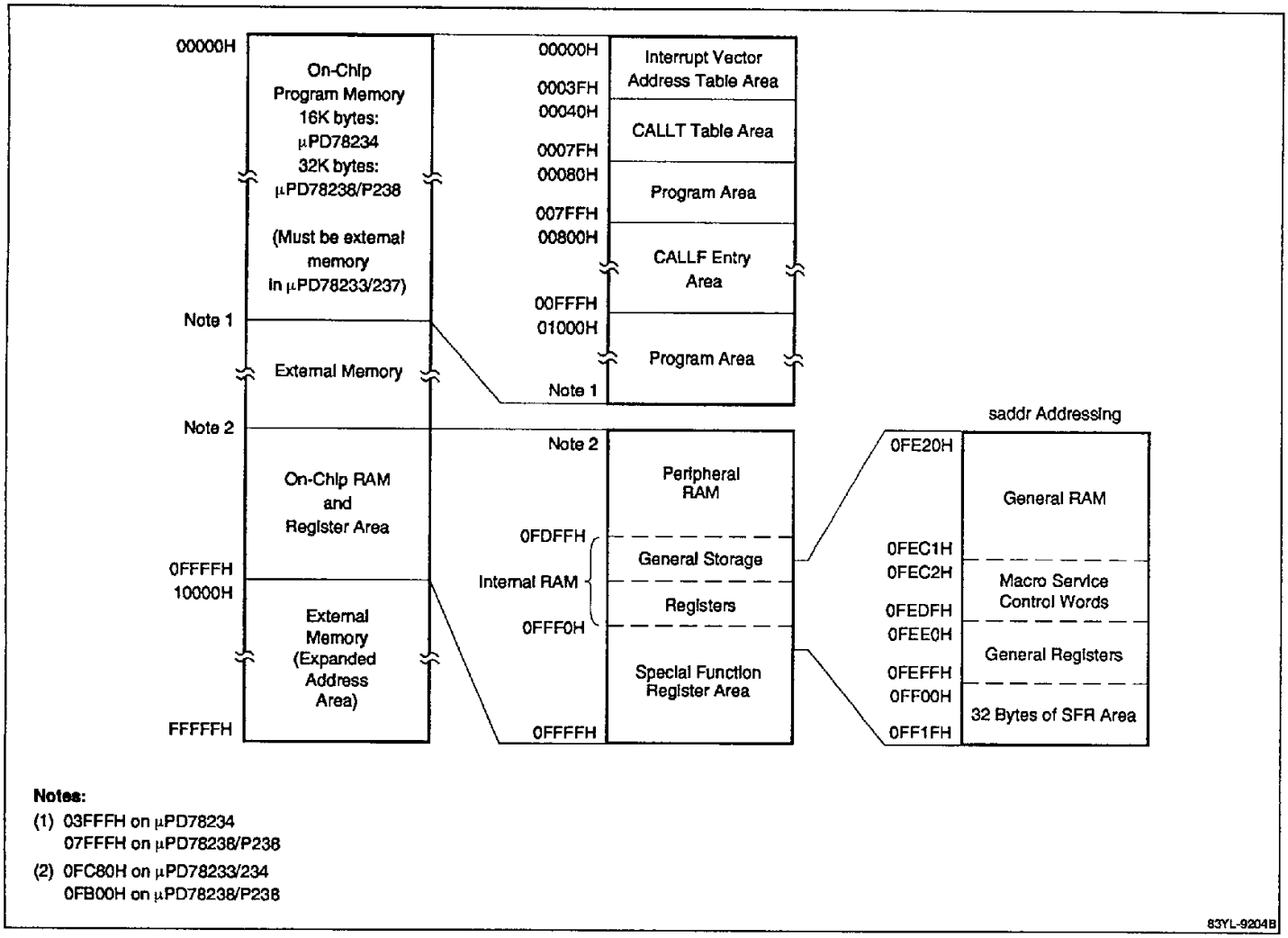


Figure 1. Memory Map



Notes:
(1) 03FFFH on μPD78234
07FFFH on μPD78238/P238
(2) 0FC80H on μPD78233/234
0FB00H on μPD78238/P238

External Memory

The μPD78238 family has an 8-bit wide external data bus and a 16-bit wide external address bus (20-bit wide if expanded memory is enabled). The low-order 8 bits of the address bus are multiplexed to provide the 8-bit data bus and are supplied by I/O port 4. The high-order address bits of the 16-bit address bus are taken from port 5. If expanded memory is enabled, the expanded address nibble is provided by $P6_0$ to $P6_3$. Address latch, read, and write strobes are also provided.

The memory expansion mode register (MM) is used to enable external memory, to specify up to two additional wait states or the use of the $\overline{WAIT}$ input pin for the first 64K bytes of memory, and to enable the high-speed internal ROM fetch. Ports 4, 5, and 6 are available as general purpose I/O ports when only internal ROM is used and no external program or data space is required.

Expanded Data Memory

The MM register is also used to enable the external expanded data memory space, addresses 10000H to FFFFFH. When the expanded data memory is enabled, the entire 1M byte address space is divided into 16 banks of 64K bytes each. The low-order 4-bits of the P6 or the PM6 registers are used as bank selection registers to supply the address information to A_{16} to A_{19}. Data can easily be transferred from one memory bank to another by using the appropriate instructions. Address lines A_{16} to A_{19} are only active when an instruction that uses expanded addressing is being executed. A programmable wait control register (PW) allows the programmer to specify up to two additional wait states or the use of the $\overline{WAIT}$ input pin for expanded data memory space.

On-Chip RAM

The μPD78237/238 have a total of 1024 bytes of on-chip RAM (640 bytes in the μPD78233/234).

The μPD78P238 also contains 1024 bytes of on-chip RAM. By using the memory size select (IMS) register, the μPD78P238 can be programmed to emulate either a μPD78234 device with 640 bytes of on-chip RAM or a μPD78238 with 1024 bytes. The programming of this register is transparent to the ROM-based device, allowing easy transfer of code to a ROM-based device.

The upper 256-byte area (FE00H-FEFFH) features high-speed access and is known as "Internal RAM." The remainder (FB00H-FDFFH and FC80H-FDFFH in the μPD78233/234) is accessed at the same speed as external memory and is known as "Peripheral RAM." The general register banks and the macro service control words are stored in Internal RAM. The remainder of Internal RAM and any unused register bank locations are available for general storage.

On-Chip Program Memory

The μPD78234/238 contain 16K and 32K bytes of internal ROM respectively. The μPD78P238 contains 32K bytes of UV EPROM or one-time programmable ROM. By using the IMS register, the μPD78P238 can be programmed to emulate a μPD78234 device with 16K bytes of internal PROM or a μPD78238 with 32K bytes. This programming is transparent to the ROM-based device, allowing easy transfer of code to a ROM-based device. Instructions from on-chip program memory can be fetched at high speed or at the same rate as from external memory. The μPD78233 and the μPD78237 do not have on-chip program memory.

CPU Control Registers

Program Counter. The program counter is a 16-bit binary counter register that holds the address of the next instruction to be executed. During reset, the program counter is loaded with the address stored in locations 0000H and 0001H.

Stack Pointer. The stack pointer is a 16-bit register that holds the address of the last item pushed onto the stack. It is decremented before new data is pushed onto the stack and incremented after data is popped off the stack.

Program Status Word. The program status word (PSW) is an 8-bit register that contains flags that are set or reset depending on the results of an instruction. This register can be written to or read from 8 bits at a time. The individual flags can also be manipulated on a bit-by-bit basis. The assignment of PSW bits follows.

7							0
IE	Z	RBS1	AC	RBS0	0	ISP	CY

CY	Carry flag
ISP	Interrupt priority status flag
RBS0, RBS1	Register bank selection flags
AC	Auxiliary carry flag
Z	Zero flag
IE	Interrupt request enable flag

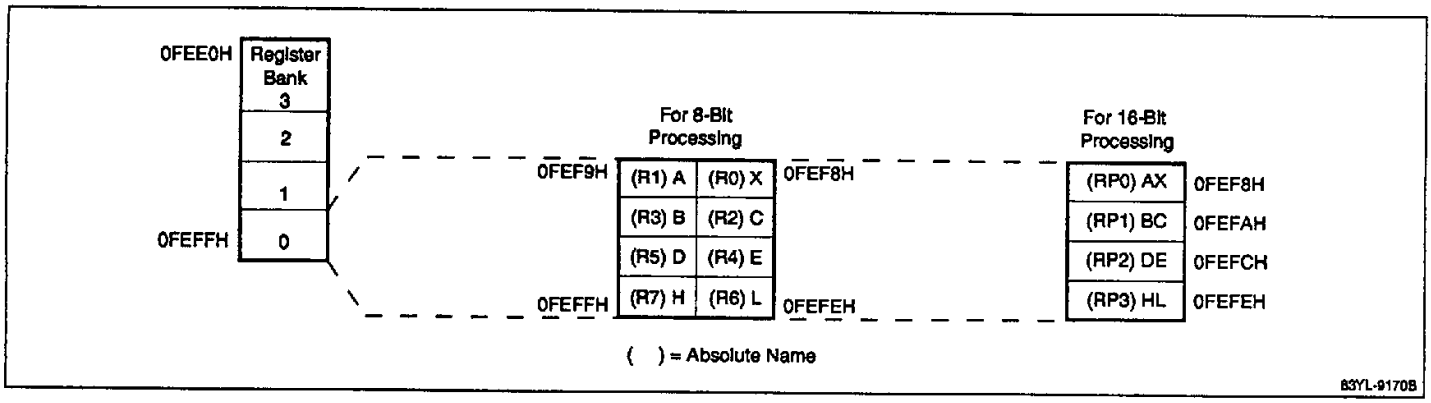
General Registers

The general-purpose registers (figure 2) consist of four banks of registers located at addresses FEE0H to FEFFH in Internal RAM. Each bank consists of eight 8-bit general registers that can also be used in pairs to function as four 16-bit registers. Two bits in the PSW (RBS0 and RBS1) specify which of the register banks is active. The bits are set under program control. Registers have both functional names (like A, X, B, C for 8-bit registers and AX, BC for 16-bit registers) and absolute names (like R1, R0, R3, R2 for 8-bit registers and RP0, RP1 for 16-bit registers). Each instruction determines whether a register is referred to by its functional or absolute name and whether it is 8 or 16 bits.

Addressing

The μPD78238 family features 1-byte addressing of both the special function registers and the portion of on-chip RAM from FE20H to FEFFH. The 1-byte sfr addressing accesses the entire SFR area, while the 1-byte saddr addressing accesses the first 32 bytes of the SFR area and 224 bytes of internal RAM. Sixteen-bit SFRs and words of memory in these areas can be addressed by 1-byte saddrp addressing, which is valid for even addresses only. Since many instructions use 1-byte addressing, access to these locations is almost as fast and versatile as access to the general registers. There are seven addressing modes for data in main memory: direct, register, register indirect with autoincrement and decrement, saddr, SFR, based, and indexed. There are also both 8-bit and 16-bit immediate operands.

Figure 2. General Registers



Special Function Registers

The input/output ports, timers, capture and compare registers, and mode and control registers for both the peripherals and the CPU are collectively known as special function registers. They are all memory-mapped between FF00H and FFFFH and can be accessed either by main memory addressing or by 1-byte sfr addressing. They are either 8 or 16 bits as required, and many of the 8-bit registers are capable of single-bit access as well. Locations FFD0H through FFDFH are known as the external SFR area. Registers in external circuitry interfaced and mapped to these addresses can be addressed with SFR addressing. Table 1 is a list of the special function registers.

Table 1. Special Function Registers

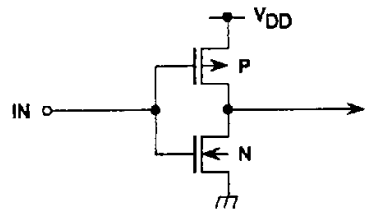
Address	Register (SFR)	Symbol	R/W	Access Units (Bits) 1	8	16	State After Reset
0FF00H	Port 0	P0	R/W	x	x	—	Undefined
0FF01H	Port 1	P1	R/W	x	x	—	Undefined
0FF02H	Port 2	P2	R	x	x	—	Undefined
0FF03H	Port 3	P3	R/W	x	x	—	Undefined
0FF04H	Port 4	P4	R/W	x	x	—	Undefined
0FF05H	Port 5	P5	R/W	x	x	—	Undefined
0FF06H	Port 6	P6	R/W	x	x	—	x0H
0FF07H	Port 7	P7	R	x	x	—	Undefined
0FF0AH	Port 0 buffer register (low)	P0L	R/W	x	x	—	Undefined
0FF0BH	Port 0 buffer register (high)	P0H	R/W	x	x	—	Undefined
0FF0CH	Real-time output port control register	RTPC	R/W	x	x	—	00H
0FF10H-0FF11H	16-bit compare register 0 (16-bit timer 0)	CR00	R/W	—	—	x	Undefined
0FF12H-0FF13H	16-bit compare register (16-bit timer 0)	CR01	R/W	—	—	x	Undefined
0FF14H	8-bit compare register (8-bit timer 1)	CR10	R/W	—	x	—	Undefined
0FF15H	8-bit compare register (8-bit timer/counter 2)	CR20	R/W	—	x	—	Undefined
0FF16H	8-bit compare register (8-bit timer/counter 2)	CR21	R/W	—	x	—	Undefined
0FF17H	8-bit compare register (8-bit timer 3)	CR30	R/W	—	x	—	Undefined
0FF18H-0FF19H	16-bit capture register (16-bit timer 0)	CR02	R	—	—	x	Undefined
0FF1AH	8-bit capture register (8-bit timer/counter 2)	CR22	R	—	x	—	Undefined
0FF1CH	8-bit capture/compare register (8-bit timer 1)	CR11	R/W	—	x	—	Undefined
0FF20H	Port 0 mode register	PM0	W	—	x	—	FFH
0FF21H	Port 1 mode register	PM1	W	—	x	—	FFH
0FF23H	Port 3 mode register	PM3	W	—	x	—	FFH
0FF25H	Port 5 mode register	PM5	W	—	x	—	FFH
0FF26H	Port 6 mode register	PM6	R/W	x	x	—	FxH
0FF30H	Capture/compare control register 0	CRC0	W	—	x	—	10H
0FF31H	Timer output control register	TOC	W	—	x	—	00H
0FF32H	Capture/compare control register 1	CRC1	W	—	x	—	00H
0FF34H	Capture/compare control register 2	CRC2	W	—	x	—	00H
0FF40H	Pullup resistor option register	PUO	R/W	x	x	—	00H
0FF43H	Port 3 mode control register	PMC3	R/W	x	x	—	00H
0FF50H-0FF51H	16-bit timer register 0	TM0	R	—	—	x	0000H
0FF52H	8-bit timer register 1	TM1	R	—	x	—	00H
0FF54H	8-bit timer register 2	TM2	R	—	x	—	00H
0FF56H	8-bit timer register 3	TM3	R	—	x	—	00H
0FF5CH	Prescaler mode register 0	PRM0	W	—	x	—	00H
0FF5DH	Timer control register 0	TMC0	R/W	—	x	—	00H
0FF5EH	Prescaler mode register 1	PRM1	W	—	x	—	00H
0FF5FH	Timer control register 1	TMC1	R/W	—	x	—	00H
0FF60H	D/A converter value setting register 0	DACS0	R/W	—	x	—	00H

Table 1. Special Function Registers (cont)

Address	Register (SFR)	Symbol	R/W	Access Units (Bits) 1	8	16	State After Reset
0FF61H	D/A converter value setting register 1	DACS1	R/W	—	x	—	00H
0FF68H	A/D converter mode register	ADM	R/W	x	x	—	00H
0FF6AH	A/D conversion result register	ADCR	R	—	x	—	Undefined
0FF70H	PWM control register	PWMC	R/W	—	x	—	05H
0FF72H-0FF73H	PWM modulo register 0	PWM0	W	—	—	x	Undefined
0FF74H-0FF75H	PWM modulo register 1	PWM1	W	—	—	x	Undefined
0FF7DH	One-shot pulse output control register	OSPC	R/W	x	x	—	00H
0FF80H	Clocked serial interface mode register	CSIM	R/W	x	x	—	00H
0FF82H	Serial bus interface control register	SBIC	R/W	x	x	—	00H
0FF86H	Serial shift register	SIO	R/W	—	x	—	Undefined
0FF88H	Asynchronous serial interface mode register	ASIM	R/W	x	x	—	80H
0FF8AH	Asynchronous serial interface status register	ASIS	R	x	x	—	00H
0FF8CH	Serial receive buffer· UART	RxB	R	—	x	—	Undefined
0FF8EH	Serial transmit shift register: UART	TxS	W	—	x	—	Undefined
0FF90H	Baud rate generator control register	BRGC	W	—	x	—	00H
0FFC0H	Standby control register	STBC	R/W	—	x	—	0000x000B
0FFC4H	Memory expansion mode register	MM	R/W	x	x	—	20H
0FFC5H	Programmable wait control register	PW	R/W	x	x	—	80H
0FFC6H	Refresh mode register	RFM	R/W	x	x	—	00H
0FFCFH	Memory size select register	IMS	W	—	x	—	Undefined
0FFD0H-0FFDFH	External SFR area	—	R/W	x	x	—	Undefined
0FFE0H	Interrupt request flag register L	IF0L	R/W	x	x	—	00H
0FFE1H	Interrupt request flag register H	IF0H	R/W	x	x	—	00H
0FFE0H-0FFE1H	Interrupt request flag register H	IF0	R/W	—	—	x	0000H
0FFE4H	Interrupt mask flag register L	MK0L	R/W	x	x	—	FFH
0FFE5H	Interrupt mask flag register H	MK0H	R/W	x	x	—	FFH
0FFE4H-0FFE5H	Interrupt mask flag register H	MK0H	R/W	—	—	x	FFFH
0FFE8H	Priority specification flag register L	PR0L	R/W	x	x	—	FFH
0FFE9H	Priority specification flag register H	PR0H	R/W	x	x	—	FFH
0FFE8H-0FFE9H	Priority specification flag register H	IF0	R/W	—	—	x	FFFH
0FFECH	Interrupt service mode specification flag register L	ISM0L	R/W	x	x	—	00H
0FFEDH	Interrupt service mode specification flag register H	ISM0H	R/W	x	x	—	00H
0FFECH-0FFEDH	Interrupt service mode specification flag register	ISM0	R/W	—	—	x	00H
0FFF4H	External interrupt mode register 0	INTM0	R/W	x	x	—	00H
0FFF5H	External interrupt mode register 1	INTM1	R/W	x	x	—	00H
0FFF8H	Interrupt status register	IST	R/W	x	x	—	00H

Figure 3. Pin I/O Circuits

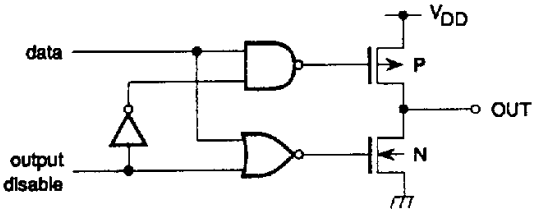
Type 1 (MODE)



Type 2 ($P2_0$, $P2_1$, $\overline{RESET}$)

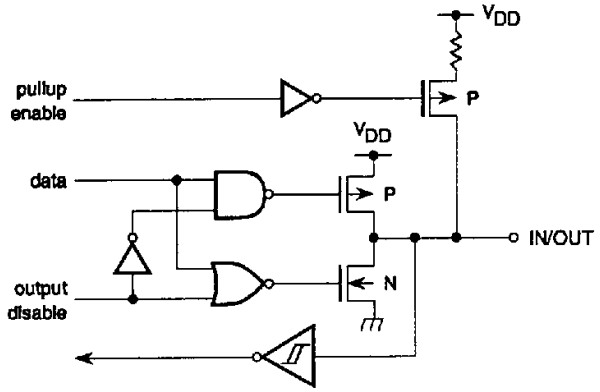
Schmitt trigger input with hysteresis characteristic.

Type 4 (P0, $P6_0$ - $P6_3$, ASTB)

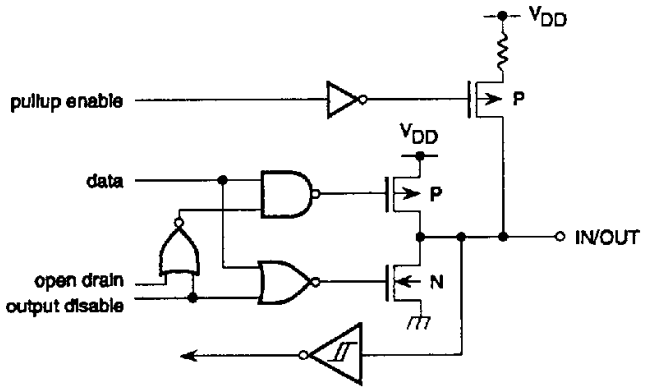


Push-pull output where the output can be placed in high-impedance (both P and N channels are turned off).

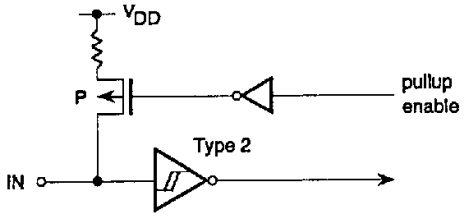
Type 8-A ($P3_2$)



Type 10-A ($P3_3$)

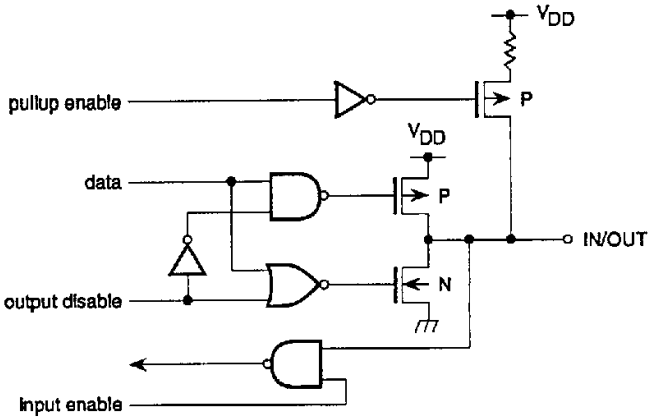


Type 2-A ($P2_2$ - $P2_7$)

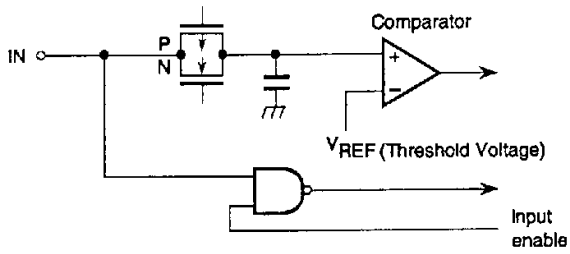


Schmitt trigger input with hysteresis characteristic.

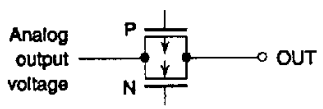
Type 5-A ($P1_0$ - $P1_7$, $P3_0$, $P3_1$, $P3_4$ - $P3_7$, P4, P5, $P6_4$, $P6_7$)



Type 9 (P7)



Type 12 (ANO0 and ANO1)



83YL-9206B

Input/Output Ports

There are up to 64 port lines on the μPD78234/238/P238 and up to 46 port lines on the μPD78233/37. (Ports 4, 5, and two bits of port 6 are not available on the μPD78233/237 since the μPD78233/237 must always use external memory.) Table 2 lists the features of each port and figure 3 shows the structure of each port pin. The pin levels of all port 2, 3, and 7 pins can always be read or tested regardless of the dual pin function.

Table 2. Digital Port Functions

Port	Operational Features	Configuration	Direct Drive Capability	Software Pullup Resistor Connection
Port 0	8-bit high impedance output		Transistor	
Port 1	8-bit input or output	Bit selectable	LED	Byte selectable, input bits only
Port 2	8-bit Schmitt trigger input			In 6-bit unit ($P2_2$-$P2_7$)
Port 3	8-bit input or output	Bit selectable		Byte selectable, input bits only
Port 4	8-bit input or output	Byte selectable	LED	Byte selectable
Port 5	8-bit input or output	Byte selectable	LED	Byte selectable, input bits only
Port 6	4-bit output (bits 0 to 3) 4-bit input or output (bits 4 to 7)	Bit selectable		In 4-bit unit, input bits only
Port 7	8-bit input			

Note:

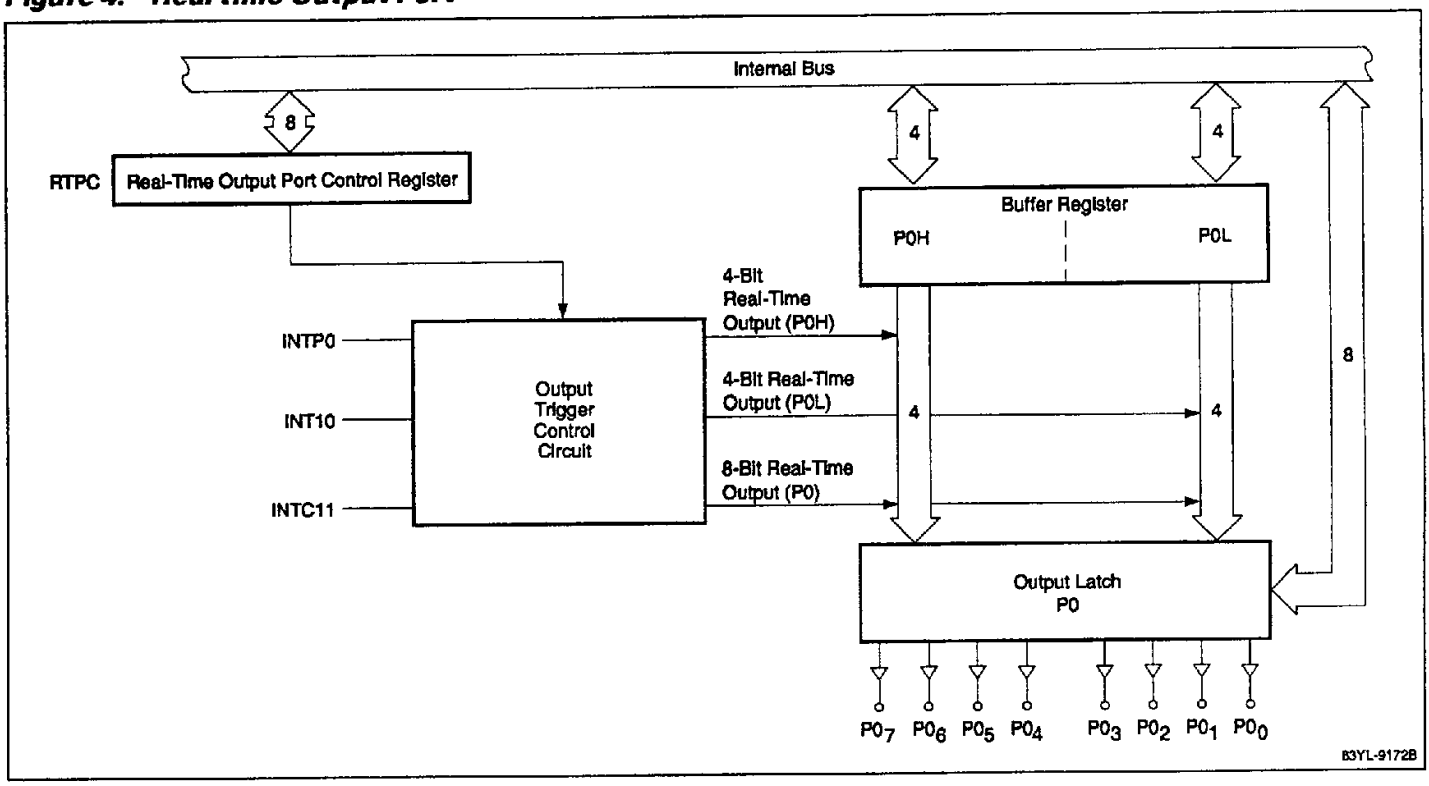
(1) Software pullup resistors can be internally connected only on a port-by-port bits to port bits set to input mode. Pullup resistors are not connected to port bits set to output mode.

Real-time Output Port

The real-time output port (RTPC) shares pins with port 0. It can be used as two independent 4-bit real-time output ports or one 8-bit real-time output port. In the real-time output mode, data stored beforehand in the buffer registers, P0H and P0L, is transferred immediately to the output latch of P0 on the occurrence of a timer 1 interrupt (INTC10 or INTC11) or external interrupt (INTP0) (see figure 4). By using the real-time output port with the macro service function, port 0 can be used to output preprogrammed patterns at preprogrammed variable time intervals. In this mode, two independent stepper motors can accurately be driven at a fixed or variable rate.

4d

Figure 4. Real-time Output Port



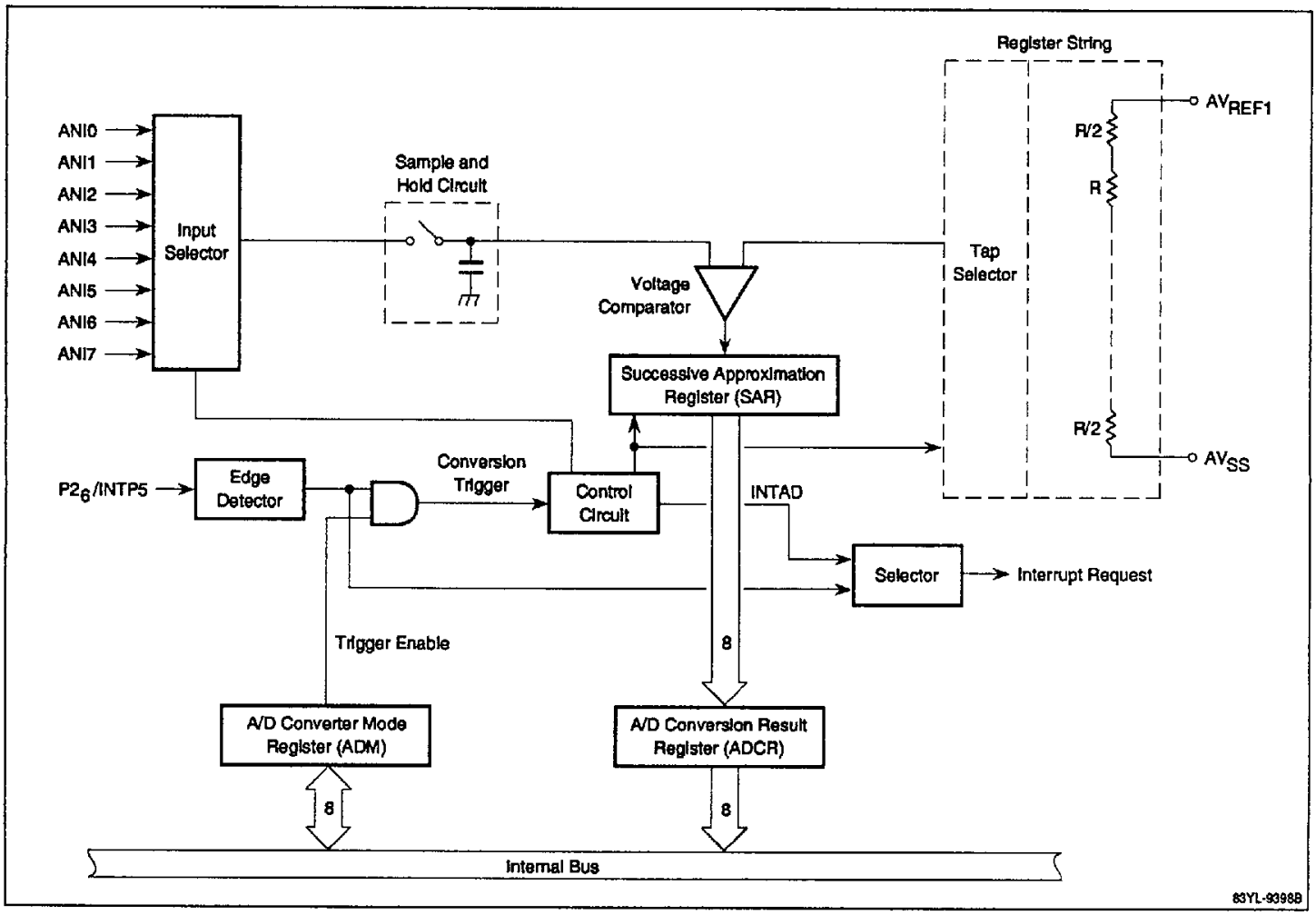
Analog-to-Digital (A/D) Converter

The μPD78238 family A/D converter (see figure 5) uses the successive-approximation method for converting up to eight multiplexed analog inputs into 8-bit digital data. The conversion time per input is 30 μs at 12 MHz operation. A/D conversion can be started by an external interrupt, INTP5, or under software control.

The A/D converter can operate in either scan mode or select mode. In scan mode, from one to eight sequential inputs can be programmed for conversion. The A/D converter selects each input in order, converts the data, stores it in the A/D conversion result (ADCR) register, and generates an interrupt (INTAD). This converted data can be easily transferred to memory by using the macro service function.

In select mode, only one of the eight A/D inputs can be selected for conversion. The ADCR register is continually updated and can be read at any time. If the A/D converter is started by an external interrupt, an INTAD interrupt occurs at the completion of each conversion. If the A/D converter is started by software, no interrupts are generated.

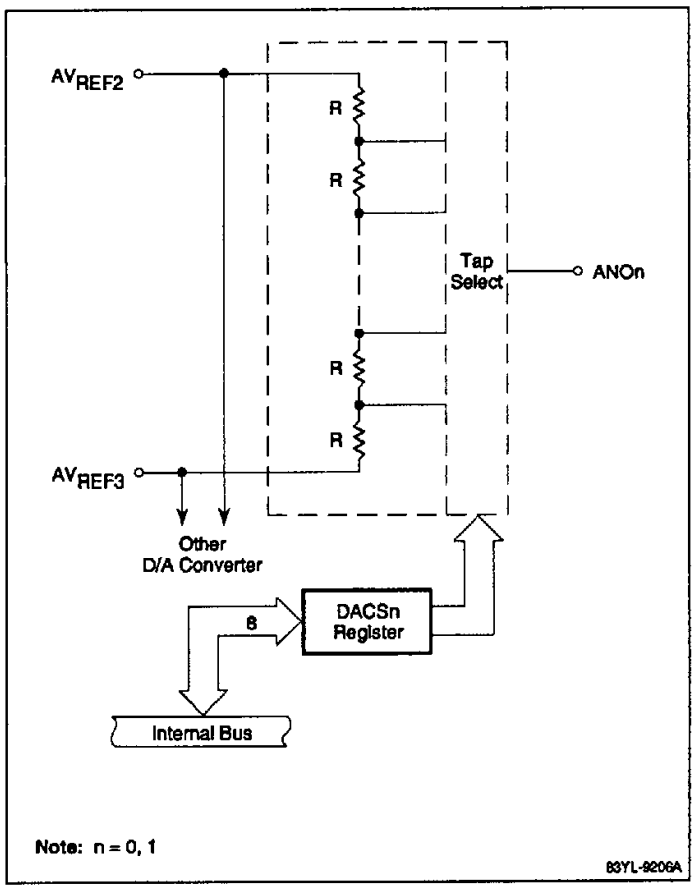
Figure 5. A/D Converter



Digital-to-Analog (D/A) Converter

The μPD78238 family has two D/A converters as shown in figure 6. The 8-bit digital data, written to the DACSn register (n= 0, 1), selects one of the 256 taps on a resistor ladder between AV_{REF2} and AV_{REF3}. The selected voltage becomes the analog output at the ANOn pin. The ANOn is a high-impedance output and requires an external buffer to drive a low-impedance load.

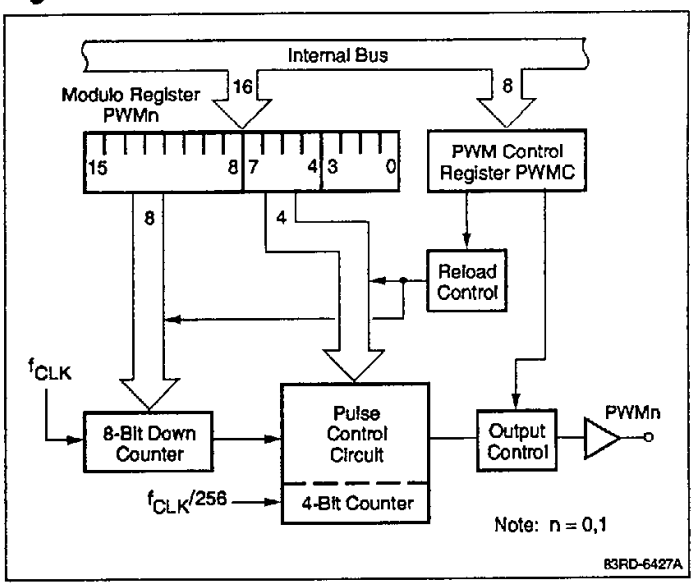
Figure 6. D/A Converter



Hardware Pulse-Width Modulated Outputs

The μPD78238 family has two 12-bit resolution pulse-width modulated (PWM) outputs (see figure 7) with a repetition rate of 23.4 kHz at 12 MHz (f_{CLK} = 6 MHz). The polarity of each output can be selected under program control. The two PWM outputs, PWM0 and PWM1, share pins with port 1, bits 0 and 1 respectively. These outputs are designed for controlling DC motors.

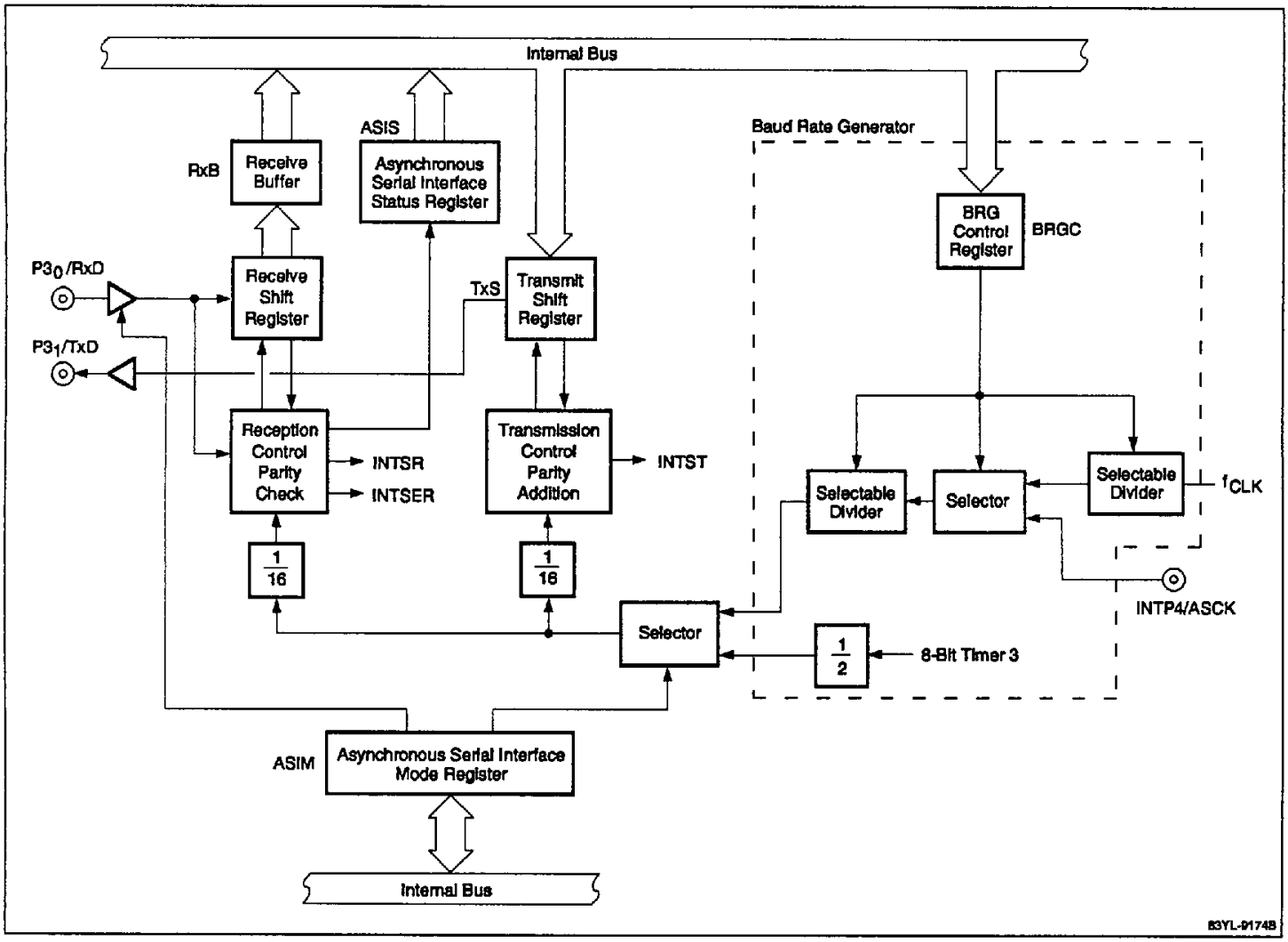
Figure 7. Hardware Pulse-Width Modulator



Serial Interface

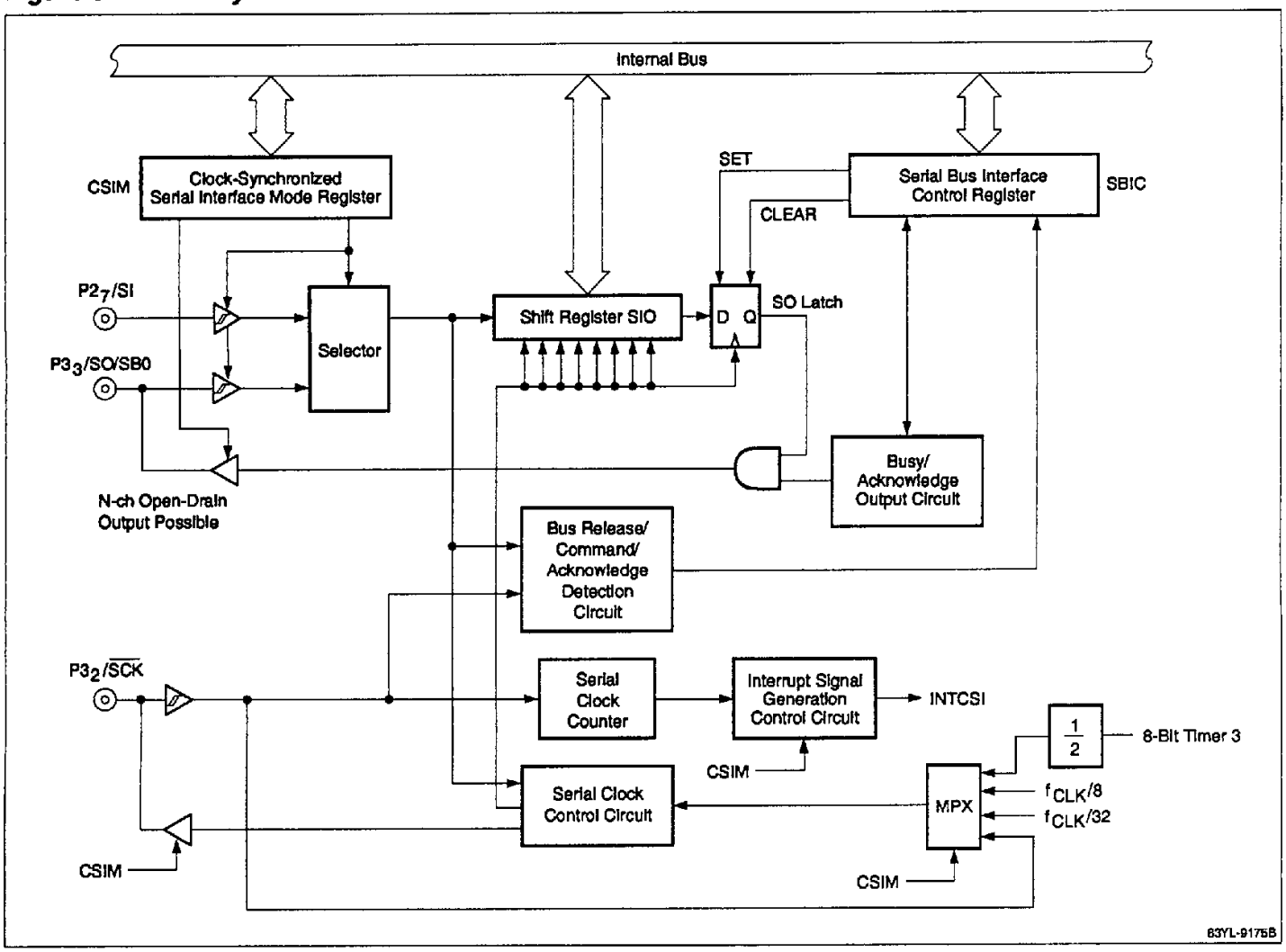
The μPD78238/P238 have two independent serial interfaces. The first is a standard UART. The UART (figure 8) permits full-duplex operation and can be programmed for 7- or 8-bits of data after the start bit, followed by one or two stop bits. Odd, even, zero or no parity can also be selected. The serial clock for the UART can be provided by an on-chip baud rate generator or timer 3. By using either the internal system clock or an external clock input into the ASCK pin, the baud rate generator is capable of generating all of the commonly used baud rates. The UART generates three interrupts: INTST (transmission complete), INTSR (reception complete), and INTSER (reception error).

Figure 8. Asynchronous Serial Interface



The second interface is an 8-bit clock-synchronized serial interface (figure 9). It can be operated in either a three-wire serial I/O mode or NEC serial bus interface (SBI) mode.

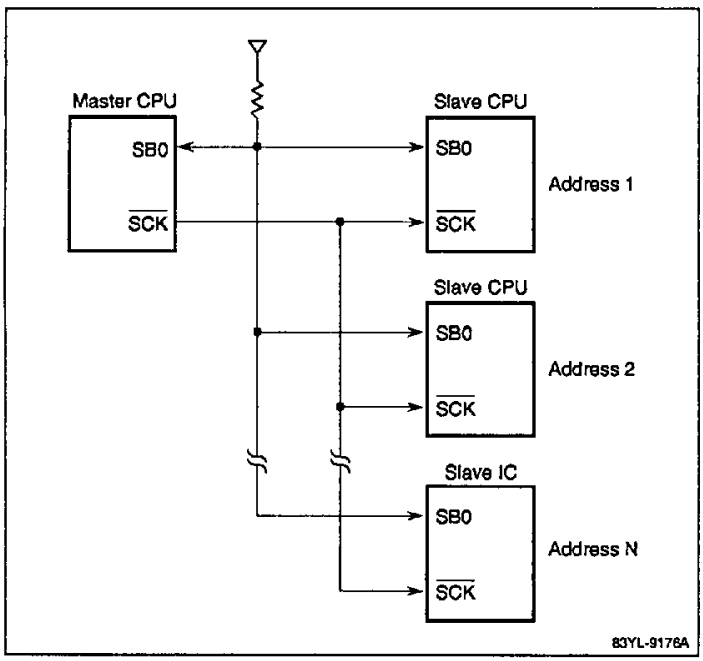
Figure 9. Clock-Synchronized Serial Interface



In the three-wire serial I/O mode, the 8-bit shift register (SIO) is loaded with a byte of data and eight clock pulses are generated. These eight pulses shift the byte of data out of the SO line (MSB first) and in from the SI line providing full-duplex operation. This interface can also be set to receive or to transmit data only. The INTCSI interrupt is generated after each 8-bit transfer. One of three internal clocks or an external clock clocks the data.

The NEC SBI mode is a two-wire high-speed proprietary serial interface available on most devices in the NEC μPD75xxx and μPD78xxx product lines. Devices are connected in a master/slave configuration (see figure 10). There is only one master device at a time; all others are slaves. The master sends addresses, commands, and data over the serial bus line (SB0) using a fixed hardware protocol synchronized with the $\overline{SCK}$ line. Each slave μPD78238 family device can be programmed in software to respond to any one of 256 addresses. There are also 256 commands and 256 data types. Since all commands are user definable, any software protocol, simple or complex, can be defined. It is even possible to develop commands to change a slave into a master and the previous master into a slave.

Figure 10. SBI Mode Master/Slave Configuration



Timers

The μPD78238 family has one 16-bit timer and three 8-bit timers. The 16-bit timer counts the internal system clock ($f_{CLK}/8$) while the three 8-bit timers can be programmed to count a number of prescaled values of the internal system clock. One of the 8-bit timers can also count external events.

Timer 0 consists of a 16-bit timer (TM0), two 16-bit compare registers (CR00 and CR01), and a 16-bit capture register (CR02). Timer 0 can be used as two interval timers, to output a programmable square wave or two pulse-width modulated signals, to measure pulse widths, or to generate a software-triggered one-shot pulse. (see figure 11).

Timer 1 consists of an 8-bit timer (TM1), 8-bit compare register (CR10), and 8-bit capture/compare register (CR11). Timer 1 can be used as two interval timers or to measure pulse widths. In addition, it can be used to generate the output trigger for the real-time output port (see figure 12).

Timer/counter 2 consists of an 8-bit timer (TM2), two 8-bit compare registers (CR20 and CR21), and an 8-bit capture register (CR22). Timer/counter 2 can also be used as two interval timers, to output a programmable square wave or two pulse-width modulated signals, or to measure pulse widths. In addition, it can be used to count external events sensed on the CI line or as a one-shot timer (see figure 13).

Timer 3 consists of an 8-bit timer (TM3) and an 8-bit compare register (CR30). Timer 3 can be used as an interval timer or as a clock for the clock-synchronized serial interface (see figure 14).

Figure 11. 16-Bit Timer 0

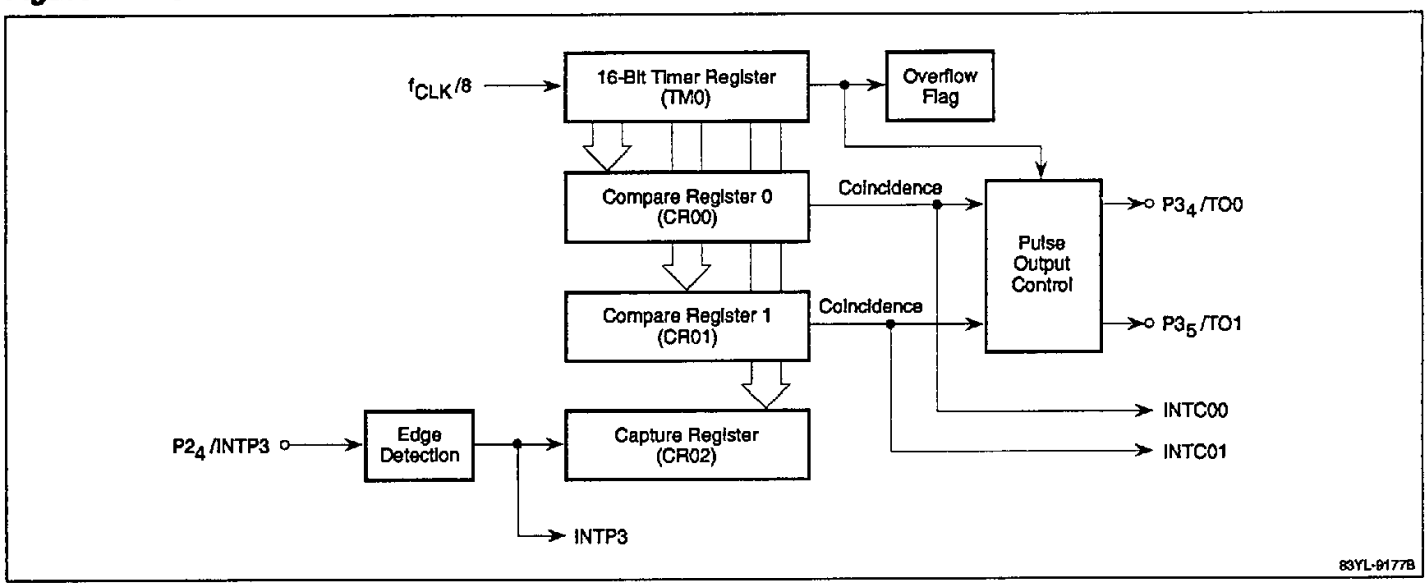


Figure 12. 8-Bit Timer 1

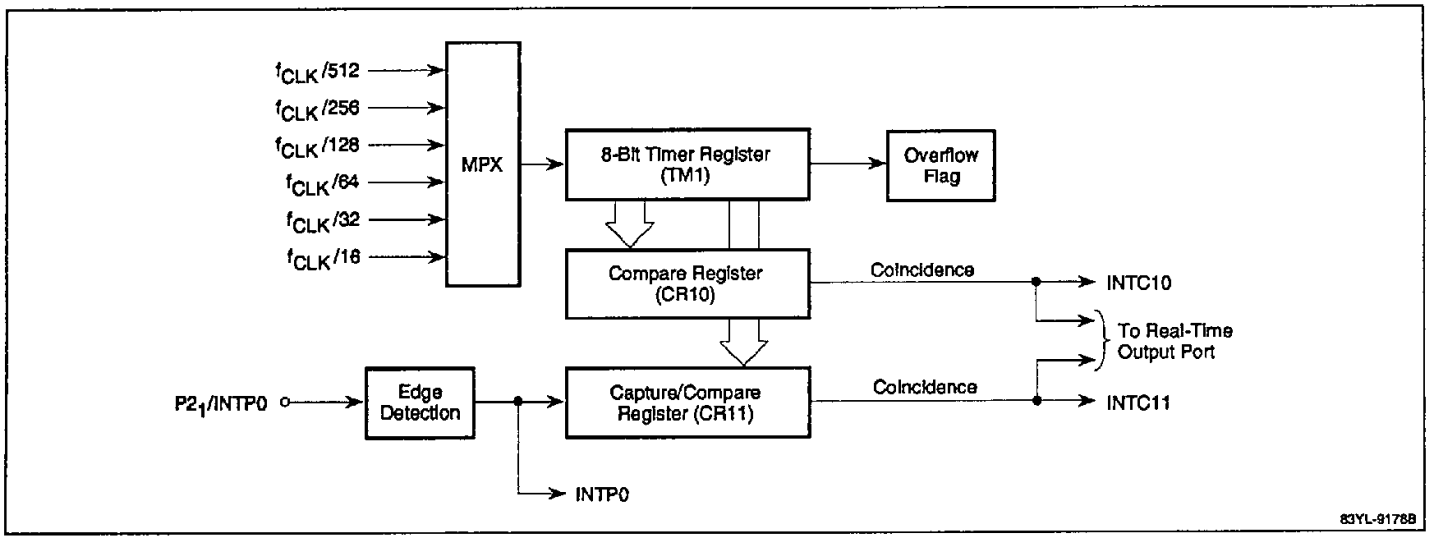


Figure 13. 8-Bit Timer/Counter 2

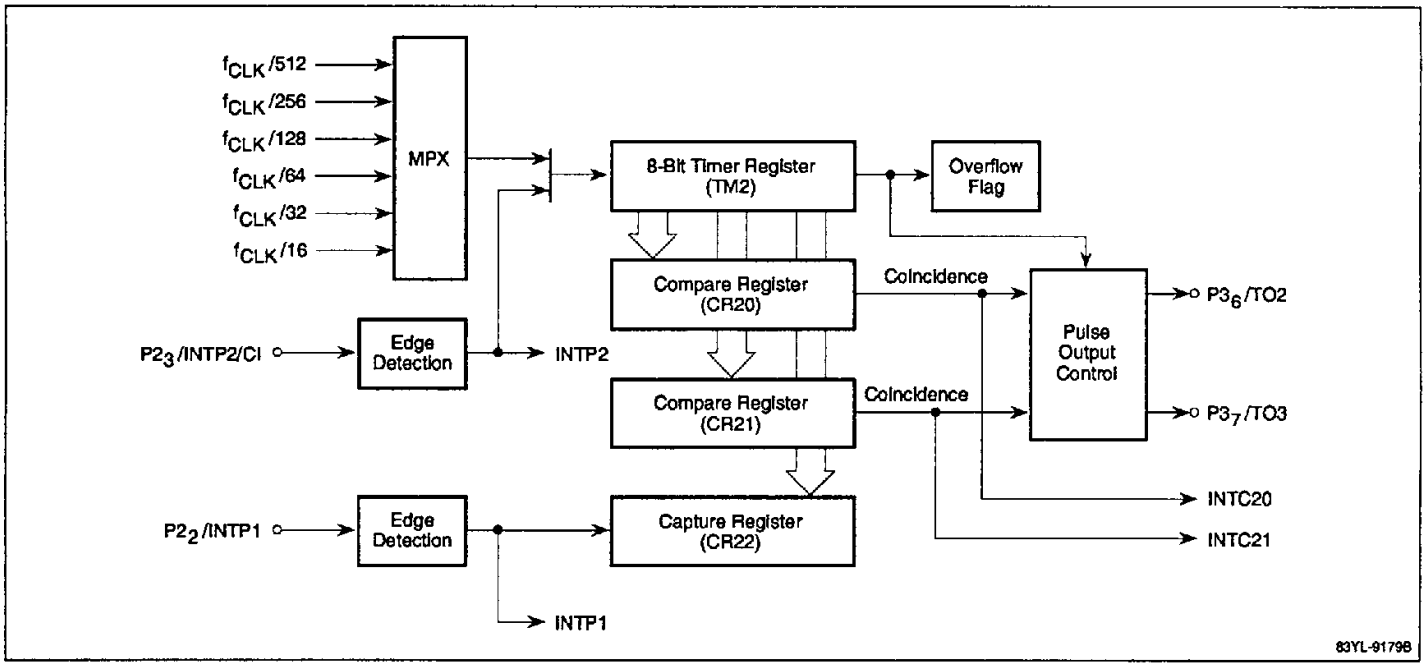
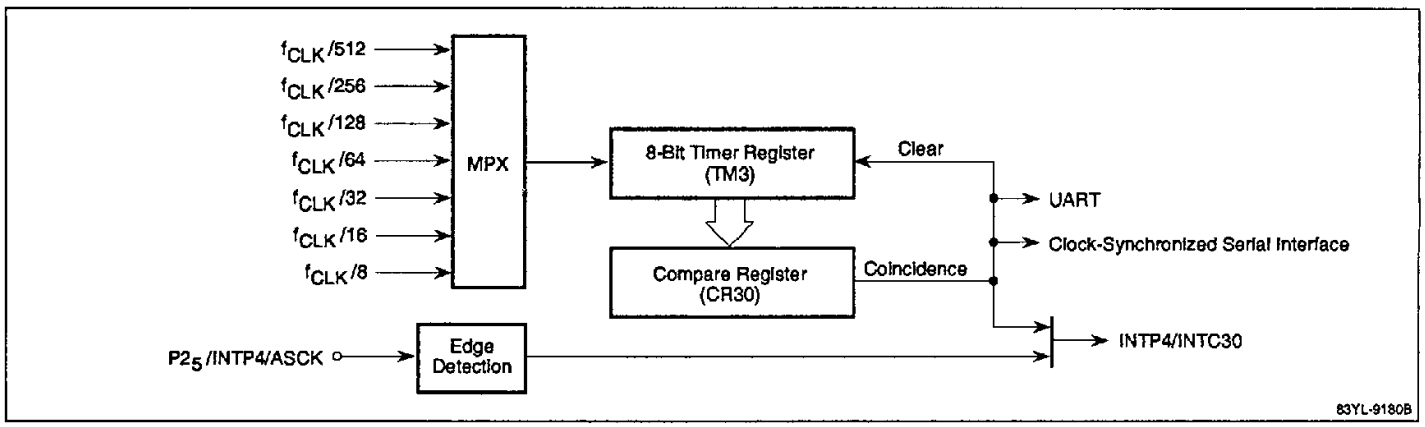


Figure 14. 8-Bit Timer 3



Interrupts

The μPD78238 family has 18 maskable hardware interrupt sources; 6 are external and 12 are internal. Since there are only 16 interrupt vectors and sets of control flags, 2 of the 6 external maskable interrupts, INTP4 and INTP5, share interrupt vectors and control flags with INTC30 and INTAD respectively. The active interrupt source for each shared vector must be chosen by the program. In addition, there is one nonmaskable interrupt and one software interrupt. The software interrupt, generated by the BRK instruction, is not maskable (see table 3).

Interrupt Servicing. The μPD78238 family provides two levels of programmable hardware priority control and two different methods of handling maskable interrupt requests: standard vectoring and macro service. The programmer can choose the priority and mode of servicing each maskable interrupt by using the interrupt control registers.

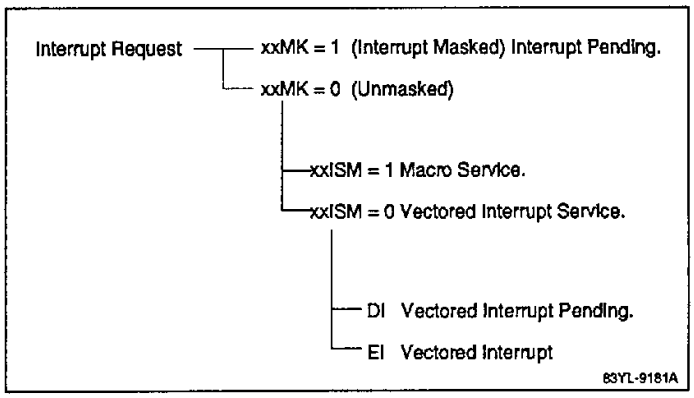
Interrupt Control Registers. The μPD78238 family has four 16-bit interrupt control registers. Each bit in each register is dedicated to one of the 16 active maskable interrupt sources. The interrupt request flag register (IF0) contains an interrupt request flag for each interrupt. The interrupt mask register (MK0) is used to enable or disable any interrupt. The interrupt service mode register (ISM0) specifies whether an interrupt is processed by vectoring or macro service. The priority flag register (PR0) can be used to specify a high or a low priority level for each interrupt.

Two other 8-bit registers are associated with interrupt processing. The interrupt status register (IST) indicates if a nonmaskable interrupt request on the NMI pin is being processed and can be used to allow nesting of nonmaskable interrupt requests. The IE and the ISP bits of the program status word are also used to control interrupts. If the IE bit is zero, all maskable interrupts, but not macro service, are disabled. The IE bit can be set or cleared using the EI and DI instructions, respectively, or by directly writing to the PSW. The IE bit is cleared each time an interrupt is accepted. The ISP bit is used by hardware to hold the priority level flag of the interrupt being serviced.

Interrupt Priority. The nonmaskable interrupt (NMI) has priority over all other interrupts. Two hardware controlled priority levels are available for the maskable interrupts. Either a high or a low priority level can be assigned by software to each of the maskable interrupts. Interrupt requests of a priority higher than the processor's current priority level are accepted; requests of the same or lower priority are held pending until the processor's priority state is lowered by program control within the current service routine or by a return instruction from the current service routine.

Interrupt requests programmed to be handled by macro service have priority over all vectored interrupt service regardless of the assigned priority level, and macro service requests are accepted even when the interrupt enable bit in the PSW is set to the disable state (see figure 15).

Figure 15. Interrupt Service Sequence



The default priorities listed in table 3 are fixed by hardware and are effective only when it is necessary to choose between two interrupt requests of the same software assigned priority. For example, the default priorities would be used after the completion of a high priority routine if two interrupts of the same priority routine were pending.

The software interrupt, initiated by the BRK instruction, is executed regardless of the processor's priority level and the state of the IE bit. It does not alter the processor's priority level.

Table 3. Interrupt Sources and Vector Addresses

Interrupt Request Type	Default Priority	Interrupt Request Generation Source	Macro Service Type	Vector Table Address
Software	None	BRK instruction execution	—	003EH
Nonmaskable	None	NMI (pin input edge detection)	—	0002H
Maskable	0	INTP0 (pin input edge detection)	A, B	0006H
	1	INTP1 (pin input edge detection)	A, B	0008H
	2	INTP2 (pin input edge detection)	A, B	000AH
	3	INTP3 (pin input edge detection)	B	000CH
	4	INTC00 (TM0-CR00 coincidence signal generation)	B	0014H
	5	INTC01 (TM0-CR01 coincidence signal generation)	B	0016H
	6	INTC10 (TM1-CR10 coincidence signal generation)	A, B, C	0018H
	7	INTC11 (TM1-CR11 coincidence signal generation)	A, B, C	001AH
	8	INTC21 (TM2-CR21 coincidence signal generation)	A, B	001CH
	9	INTP4 (pin input edge detection)	B	000EH
		INTC30 (TM3-CR30 coincidence signal generation)	A, B	
	10	INTP5 (pin input edge detection)	B	0010H
		INTAD (end of A/D conversion)	A, B	
	11	INTC20 (TM2-CR20 coincidence signal generation)	A, B	0012H
	12	INTSER (generation of asynchronous serial interface receive error)	—	0020H
	13	INTSR (end of asynchronous serial interface reception)	A, B	0022H
	14	INTST (end of asynchronous serial interface transmission)	A, B	0024H
	15	INTCSI (end of clocked serial interface transmission)	A, B	0026H

Vectored Interrupt. When vectored interrupt is specified for a given interrupt request, (1) the program status word and the program counter are saved on the stack, (2) the processor's priority is set to that specified for the interrupt, (3) the IE bit in the PSW is set to zero, and (4) the routine whose address is in the interrupt vector table is entered. At the completion of the service routine, the RETI instruction (RETB instruction for the software interrupt) reverses the process and the μPD78238 family device resumes the interrupted routine.

Macro Service

When macro service is specified for a given interrupt, the macro service hardware temporarily stops the executing program and begins to transfer data between the special function register area and the memory space. One byte is transferred each interrupt. When the data transfer is complete, control is returned to the executing program, providing a completely transparent method of interrupt service. Macro service significantly improves response time and makes it unnecessary to save any registers.

For each request on the interrupt line, one operation is performed, and an 8-or 16-bit counter is decremented. When the counter reaches zero, a vectored interrupt service routine is entered according to the specified priority.

Macro service is provided for all of the maskable interrupt requests except INTSER, the asynchronous serial interface receive error interrupt request. Each interrupt request has a dedicated macro service control word stored in Internal RAM (see figure 16). The function to be performed is specified in the control word.

The μPD78238 family provides three different types of macro service transfers:

Macro Service Type A. A byte of data is transferred in either direction between a special function register, preassigned for each interrupt request, and a buffer in internal RAM (FExx). Only the 8-bit macro service counter is available for Type A transfers. The preassigned SFRs for the 12 interrupt requests that support macro service Type A transfers are listed in table 4.

Figure 16. Macro Service Control Word Map

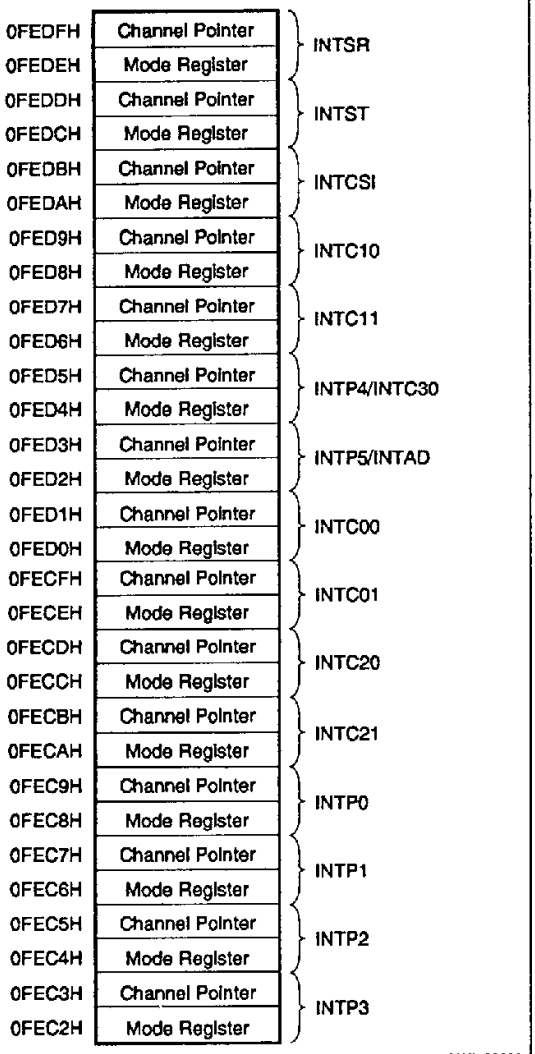


Table 4. Macro Service Type A Interrupts and Assigned SFRs

Interrupt Request	Source/Destination SFR
INTC10. TM1-CR10 coincidence	CR10. Timer 1 8-bit compare register
INTC11 TM1-CR11 coincidence	CR11. Timer 1 8-bit capture/ compare register
INTC20: TM2-CR20 coincidence	CR20 Timer 2 8-bit compare register
INTC21: TM2-CR21 coincidence	CR21 Timer 2 8-bit compare register
INTC30 TM3-CR30 coincidence	CR30: Timer 3 8-bit compare register
INTSR: End of asynchronous serial interface reception	RxB. Serial receive buffer
INTST: End of asynchronous serial interface transmission	TxS Serial transmit shift register
INTCSI End of clocked serial interface transmission	SIO Serial shift register
INTAD· End of A/D conversion	ADCR: A/D conversion result register
INTP0: External interrupt pin $P0_1$	CR11: Timer 1 8-bit capture/ compare register
INTP1· External interrupt pin $P0_2$	CR22: Timer 2 8-bit capture register
INTP2· External interrupt pin $P0_3$	TM2 Timer 2 8-bit timer register

Macro Service Type B. A byte of data is transferred in either direction between any specified special function register and a buffer anywhere in the 64K byte address space. Macro service Type B transfers can be initiated by any maskable interrupt except INTSER.

Macro Service Type C. A byte of data is transferred from a buffer anywhere in the 64K byte address space to one of the 8-bit compare registers of timer 1. At the same time, a second byte of data is transferred from a buffer anywhere in the 64K byte address space to the real-time output port buffer. The macro service counter can be programmed either to be an 8- or 16-bit counter. Macro service Type C transfers can be initiated by INTC10 with data transferred to CR10 and P0L or P0H, or by INTC11 with data transferred to CR11 and P0L or P0H.

In addition, the macro service Type C transfer can be initialized to automatically alter timer compare register values or to repeatedly output a prespecified pattern at a fixed or variable rate. By using macro service Type C transfers to control the real-time output ports, the μPD78238 family device can easily and accurately drive two independent stepper motors.

Refresh

The refresh signal is used with any pseudostatic RAM equivalent of the NEC μPD428128. The refresh cycle can be set to one of four intervals: 16, 32, 64, or $128/f_{CLK}$ (2.6, 5.3, 10.7, and 21.3 μs at 12 MHz). The refresh cycle is timed to follow a read or write operation to avoid interference with external memory access cycles.

Standby Modes

HALT and STOP modes are provided to reduce power consumption when CPU action is not required. In HALT mode, the CPU is stopped but the system clock continues to run. The HALT mode is released by any unmasked interrupt, an external NMI, or an external reset pulse. In STOP mode, both the CPU and the system clock are stopped, further minimizing the power consumption. The STOP mode is released by either an external reset pulse or an external NMI. The HALT and STOP modes are entered by programming the standby control register (STBC). This register is a protected location and can be written to only by a special instruction. If the third and fourth bytes of the instruction are not complements of each other, the data is not written and the next instruction is executed.

External Reset

The μPD78238 family is reset by taking the $\overline{\text{RESET}}$ pin low. The $\overline{\text{RESET}}$ input pin contains a noise filter to protect against spurious system resets caused by noise. On power-up, the $\overline{\text{RESET}}$ pin must remain low until the power supply reaches its operating voltage and the oscillator has stabilized. During reset, the program counter is loaded with the address contained in the reset vector table (address 0000H- 0001H); program execution starts at that address upon the $\overline{\text{RESET}}$ pin going high. While $\overline{\text{RESET}}$ is low, all external lines except V_{SS}, V_{DD}, AV_{SS}, AV_{REF1}, AV_{REF2}, AV_{REF3}, X1, and X2 are in the high impedance state.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Operating voltage, V_{DD}	−0.5 to +7.0 V
AV_{DD}	AV_{SS} to V_{DD} +0.5 V
AV_{SS}	−0.5 to +0.5 V
Input voltage, V_{I1}	−0.5 to V_{DD} + 0.5 V
V_{I2} (Note 1 for μPD78P238)	−0.5 to +13.5 V
Output voltage, V_O	−0.5 to V_{DD} +0.5 V
Low-level output current, I_{OL}	
Per pin	15 mA
Total, all output pins	100 mA
High-level output current, I_{OH}	
Per pin	−10 mA
Total, all output pins	−50 mA
A/D converter reference input voltage, AV_{REF1}	−0.5 to V_{DD} + 0.3 V
D/A converter reference input voltage, AV_{REF2}	−0.5 to V_{DD} + 0.3 V
AV_{REF3}	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Note:

(1) MODE/V_{PP} and $P2_1$/INTP0/A_9 in programming mode

Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the rating could cause permanent damage. The device should be operated within the limits specified under DC and AC chracteristics

Operating Conditions

Oscillation Frequency	T_A	V_{DD}
f_{XX} = 4 to 12 MHz	−40 to +85°C	+5 V ±10%

Capacitance

T_A = +25°C; V_{DD} = V_{SS} = 0 V

Item	Symbol	Max	Unit	Conditions
Input capacitance	C_I	20	pF	f = 1 MHz; pins not used for measurement are at 0 V
Output capacitance	C_O	20	pF	
Input/output capacitance	C_{IO}	20	pF	

External Clock Operation

T_A = −40 to +85°C; V_{DD} = +5 V 10%; V_{SS} = 0 V

Item	Symbol	Min	Max	Unit	Conditions
X1 input low-level width	t_{WXL}	30	130	ns	
X1 input high-level width	t_{WXH}	30	130	ns	
X1 input rise time	t_{XR}	0	30	ns	
X1 input fall time	t_{XF}	0	30	ns	
X1 input clock cycle time	t_{CYX}	82	250	ns	

DC Characteristics

T_A = −40 to +85°C, V_{DD} = AV_{DD} = +5 V ±10%; V_{SS} = AV_{SS} = 0 V

Item	Symbol	Min	Typ	Max	Unit	Conditions
Low-level input voltage	V_{IL}	0		0.8	V	
High-level input voltage	V_{IH1}	2.2		V_{DD}	V	Except the specified pins (Note 1)
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Specified pins (Note 1)
Low-level output voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
	V_{OL2}			1.0	V	I_{OL} = 8.0 mA (Note 2)
High-level output voltage	V_{OH1}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{DD} − 0.5			V	I_{OH} = −100 μA
	V_{OH3}	2.0			V	I_{OH} = −5.0 mA (Note 3)
X1 low-level input current	I_{IL}			−100	μA	0 V ≤ V_I ≤ V_{IL}
X1 high-level input current	I_{IH}			100	μA	V_{IH2} ≤ V_I ≤ V_{DD}
Input leakage current	I_{LI}			±10	μA	0 V ≤ V_I ≤ V_{DD}
Output leakage current	I_{LO}			±10	μA	0 V ≤ V_O ≤ V_{DD}
V_{DD} power supply current	I_{DD1}		20	40	mA	Operating mode, f_{XX} = 12 MHz
	I_{DD2}		7	20	mA	HALT mode, f_{XX} = 12 MHz
Data retention voltage	V_{DDDR}	2.5		5.5	V	STOP mode

DC Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Conditions
Data retention current	I_{DDDR}			10	μA	STOP mode; V_{DDDR} = 2.5 V
				20	μA	STOP mode, V_{DDDR} = 5 V ±10%
Pullup resistor	R_L	15	40	80	kΩ	V_I = 0 V

Notes:

(1) X1, X2, $\overline{RESET}$, $P2_0$/NMI, $P2_1$/INTP0, $P2_2$/INTP1, $P2_3$/INTP2/CI, $P2_4$/INTP3, $P2_5$/INTP4/ASCK, $P2_6$/INTP5, $P2_7$/SI, $P3_2$/SCK, $P3_3$/SO/SB0, and MODE pins.

(2) Pins $P1_0$ - $P1_7$, $P4_0/AD_0$ - $P4_7/AD_7$, and $P5_0/A_8$ - $P5_7/A_{15}$.

(3) Pins $P0_0$ - $P0_7$.

AC Characteristics—Read/Write Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V; f_{XX} = 12 MHz; C_L = 100 pF

Item	Symbol	Calculation Formula (Note 2, 3)	Min	Max	Unit	Conditions
X1 input clock cycle time	t_{CYX}	—	82	250	ns	
Address setup time to ASTB ↓	t_{SAST}	t_{CYX} − 30	52		ns	
Address hold time from ASTB ↓ (Note 1)	t_{HSTA}	—	25		ns	
Address hold time from $\overline{RD}$↑	t_{HRA}	—	30		ns	
Address hold time from $\overline{WR}$ ↑	t_{HWA}	—	30		ns	
Address to $\overline{RD}$ ↓ delay time	t_{DAR}	$2t_{CYX}$ − 35	129		ns	
Address float time to $\overline{RD}$ ↓	t_{FAR}	$t_{CYX}/2$ − 30	11		ns	
Address to data input time	t_{DAID}	(4+2n) t_{CYX} − 100		228	ns	No wait states
ASTB ↓ to data input time	t_{DSTID}	$(3+2n)t_{CYX}$ − 65		181	ns	No wait states
$\overline{RD}$ ↓ to data input time	t_{DRID}	$(2+2n)t_{CYX}$ − 64		100	ns	No wait states
ASTB ↓ to $\overline{RD}$ ↓ delay time	t_{DSTR}	t_{CYX} − 30	52		ns	
Data hold time from $\overline{RD}$ ↑	t_{HRID}	—	0		ns	
$\overline{RD}$ ↑ to address active time	t_{DRA}	$2t_{CYX}$ − 40	124		ns	
$\overline{RD}$ ↑ to ASTB ↑ delay time	t_{DRST}	$2t_{CYX}$ − 40	124		ns	
$\overline{RD}$ low-level width	t_{WRL}	$(2+2n)t_{CYX}$ − 40	124		ns	No wait states
ASTB high-level width	t_{WSTH}	t_{CYX} − 30	52		ns	
Address to $\overline{WR}$ ↓ delay time	t_{DAW}	$2t_{CYX}$ − 35	129		ns	
$\overline{ASTB}$ ↓ to data output time	t_{DSTOD}	t_{CYX} + 60		142	ns	
$\overline{WR}$ ↓ to data output time	t_{DWOD}	—		60	ns	
ASTB ↓ to $\overline{WR}$ ↓ delay time	t_{DSTW1}	t_{CYX} − 30	52		ns	
	t_{DSTW2}	$2t_{CYX}$ − 35	129		ns	Refresh mode
Data setup time to $\overline{WR}$ ↑	t_{SODWR}	$(3+2n)t_{CYX}$ − 100	146		ns	No wait states
Data setup time to $\overline{WR}$ ↓	t_{SODWF}	t_{CYX} − 60	22		ns	Refresh mode
Data hold time from $\overline{WR}$ ↑ (Note 1)	t_{HWOD}	—	20		ns	
$\overline{WR}$ ↑ to ASTB ↑ delay time	t_{DWST}	t_{CYX} − 40	42		ns	
$\overline{WR}$ low-level width	t_{WWL1}	$(3+2n)t_{CYX}$ − 50	196		ns	No wait states
	t_{WWL2}	$(2+2n)t_{CYX}$ − 50	114		ns	Refresh mode, No wait states
Address to $\overline{WAIT}$ ↓ input time	t_{DAWT}	$3t_{CYX}$ − 100		146	ns	
ASTB ↓ to $\overline{WAIT}$ ↓ input time	t_{DSTWT}	$2t_{CYX}$ − 80		84	ns	
$\overline{WAIT}$ hold time from ASTB ↓	t_{HSTWT}	$2Xt_{CYX}$ + 10	174		ns	One external wait state
ASTB ↓ to $\overline{WAIT}$ ↑ delay time	t_{DSTWTH}	$2(1+X)t_{CYX}$ − 55		273	ns	One external wait state

AC Characteristics—Read/Write Operation (cont)

Item	Symbol	Calculation Formula (Note 2, 3)	Min	Max	Unit	Conditions
$\overline{RD}$ ↓ to $\overline{WAIT}$ input time	t_{DRWTL}	$t_{CYX} - 60$		22	ns	
$\overline{WAIT}$ hold time from $\overline{RD}$ ↓	t_{HRWT}	$(2X-1)t_{CYX} + 5$	87		ns	One external wait state
$\overline{RD}$ ↓ to $\overline{WAIT}$ ↑ delay time	t_{DRWTH}	$(2X+1)t_{CYX} - 60$		186	ns	One external wait state
$\overline{WAIT}$ ↑ to data input time	t_{DWTID}	$t_{CYX} - 20$		62	ns	
$\overline{WAIT}$ ↑ to $\overline{WR}$ ↑ delay time	t_{DWTW}	$2t_{CYX} - 10$	154		ns	
$\overline{WAIT}$ ↑ to $\overline{RD}$ ↑ delay time	t_{DWTR}	$t_{CYX} - 10$	72		ns	
$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ input time	t_{DWWTL}	$t_{CYX} - 60$		22	ns	Refresh disabled
$\overline{WAIT}$ hold time from $\overline{WR}$ ↓	t_{HWWT1}	$(2X-1)t_{CYX} + 5$	87		ns	One external wait state, refresh disabled
	t_{HWWT2}	$2(X-1)t_{CYX} + 5$	5		ns	One external wait state; refresh enabled
$\overline{WR}$ ↓ to $\overline{WAIT}$ ↑ delay time	t_{DWWTH1}	$(2X+1)t_{CYX} - 60$		186	ns	One external wait state, refresh disabled
	t_{DWWTH2}	$2Xt_{CYX} - 60$		104	ns	One external wait state, refresh enabled
$\overline{RD}$ ↑ to $\overline{REFRQ}$ ↓ delay time	t_{DRRFQ}	$2t_{CYX} - 10$	154		ns	
$\overline{WR}$ ↑ to $\overline{REFRQ}$ ↓ delay time	t_{DWRFQ}	$t_{CYX} - 10$	72		ns	
$\overline{REFRQ}$ low-level width	t_{WRFQL}	$2t_{CYX} - 44$	120		ns	
$\overline{REFRQ}$ ↑ to ASTB ↑ delay time	t_{DRFQST}	$4t_{CYX} - 48$	280		ns	

Notes:

(1) The hold time includes the time during which V_{OH} and V_{OL} are retained under the following load conditions: C_L = 100 pF and R_L = 2 kΩ

(2) n indicates the number of internal wait states.

(3) X indicates the number of external wait states (1, 2, 3, ...)

Serial Port Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V; f_{XX} = 12 MHz; C_L = 100 pF

Item	Symbol	Min	Max	Unit	Conditions
Serial clock cycle time	t_{CYSK}	1 0		μs	External clock input
		1 3		μs	Internal clock/16 output
		5.3		μs	Internal clock/64 output
Serial clock low-level width	t_{WSKL}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2 5		μs	Internal clock/64 output
Serial clock high-level width	t_{WSKH}	420		ns	External clock input
		556		ns	Internal clock/16 output
		2.5		μs	Internal clock/64 output
SI, SB0 setup time to $\overline{SCK}$ ↑	t_{SSSK}	150		ns	
SI, SB0 hold time from $\overline{SCK}$ ↑	t_{HSSK}	400		ns	
SO/SB0 output delay time from $\overline{SCK}$ ↓	t_{DSBSK1}	0	300	ns	CMOS push-pull output (3-line serial I/O mode)
	t_{DSBSK2}	0	800	ns	Open-drain output (SBI mode), R_L = 1 kΩ
SB0 high, hold time from $\overline{SCK}$ ↑	t_{HSBSK}	4		t_{CYX}	SBI mode
SB0 low, setup time to $\overline{SCK}$ ↓	t_{SSBSK}	4		t_{CYX}	SBI mode
SB0 low-level width	t_{WSBL}	4		t_{CYX}	
SB0 high-level width	t_{WSBH}	4		t_{CYX}	

A/D Converter Operation

T_A = −40 to +85°C; V_{DD} = AV_{DD} +5 V ±10%, V_{SS} = AV_{SS} = 0 V

Item	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		8			Bit	
Full-scale error (Note 1)				0.4	%	AV_{REF1} = 4 0 V to AV_{DD}; T_A = −10 to +70°C
				0 8	%	AV_{REF1} = 3.4 V to AV_{DD}
				0 6	%	AV_{REF1} = 4 0 V to AV_{DD}
Quantization error				±1/2	LSB	
Conversion time	t_{CONV}	240			t_{CYX}	82 ns ≤ t_{CYX} ≤ 250 ns
Sampling time	t_{SAMP}	48			t_{CYX}	82 ns ≤ t_{CYX} ≤ 250 ns
Analog input voltage	V_{IAN}	−0 3		AV_{REF1} + 0.3	V	
Analog input impedance	R_{AN}		1000		MΩ	
Analog reference voltage	AV_{REF1}	3.4		AV_{DD}	V	
AV_{REF1} current	AI_{REF1}		1 5	3 0	mA	f_{XX} = 12 MHz
			0.7	1.5	mA	Note 2
AV_{DD} current	AI_{DD1}		1 4	3.0	mA	f_{XX} = 12 MHz
	AI_{DD2}		10	20	μA	Note 3

Notes:

(1) Quantization errror is not included. Unit is defined as percent of full-scale value.

(2) When CS bit of the ADM register is set to 0.

(3) When CS bit of the ADM register is set to 0 in the STOP mode

D/A Converter Operation

T_A = −40 to +85°C; AV_{REF2} = V_{DD} = +5 V ±10%; AV_{REF3} = V_{SS} = 0 V

Item	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		8			Bit	
Overall Error				0.4	%	Load conditions: 4 MΩ, 30 pF
				0.6	%	Load conditions: 2 MΩ, 30 pF
				0.6	%	AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD} Load conditions 4 MΩ, 30 pF
				0.8	%	AV_{REF2} = 0.75 V_{DD}; AV_{REF3} = 0.25 V_{DD}; Load conditions 2 MΩ, 30 pF
Setting time	Undefined			10	μs	Load conditions: 2 MΩ, 30 pF
Analog reference voltage 2	V_{AVREF2}	0.75 V_{DD}		V_{DD}	V	
Analog reference voltage 3	V_{AVREF3}	0	0.25 V_{DD}	V		
Reference power input current 2	AI_{REF2}	0	5	mA		
Reference power input current 3	AI_{REF3}	−5.0	0	mA		
Output resistance	R_O		20		kΩ	DACS0, DACS1 set to 7FH

Interrupt Timing Operation

T_A = −40 to +85°C; V_{DD} = +5 V ±10%; V_{SS} = 0 V

Item	Symbol	Min	Max	Unit	Conditions
NMI low-level width	t_{WNIL}	10		μs	
NMI high-level width	t_{WNIH}	10		μs	
INTP0-INTP5 low-level width	t_{WITL}	24		t_{CYX}	
INTP0-INTP5 high-level width	t_{WITH}	24		t_{CYX}	
$\overline{RESET}$ low-level width	t_{WRSL}	10		μs	
$\overline{RESET}$ high-level width	t_{WRSH}	10		μs	

Data Retention Characteristics

T_A = −40 to +85°C

Item	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.5		5.5	V	STOP mode
Data retention current	I_{DDDR}		2	10	μA	V_{DDDR} = 2.5 V
			5	20	μA	V_{DDDR} = 5 V ±10%
V_{DD} rise time	t_{RVD}	200			μs	
V_{DD} fall time	t_{FVD}	200			μs	
V_{DD} retention time (from STOP mode setting)	t_{HVD}	0			ms	
STOP release signal input time	t_{DREL}	0			ms	
Oscillation stabilization wait time	t_{WAIT}	30			ms	Crystal resonator
		5			ms	Ceramic resonator
Low-level input voltage	V_{IL}	0		0.1 V_{DDDR}	V	Specified pins (Note 1)
High-level input voltage	V_{IH}	0.9 V_{DDDR}		V_{DDDR}	V	Specified pins (Note 1)

Note:

(1) $\overline{\text{RESET}}$, $P2_0$/NMI, $P2_1$/INTP0, $P2_2$/INTP1, $P2_3$/INTP2/CI, $P2_4$/INTP3, $P2_5$/INTP4/ASCK, $P2_6$/INTP5, $P2_7$/SI, $P3_2$/SCK, $P3_3$/SO/SB0, and MODE pins.

Recommended Crystal Resonators (μPD78233/234 only)

Manufacturer	Frequency (MHz)	Part Number	C1 (pF)	C2 (pF)
Kinseki	12	HC-49/U	18	18

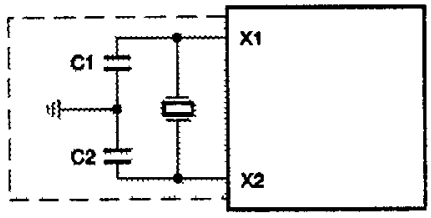
Recommended Ceramic Resonators (μPD78233/234 only)

Manufacturer	Frequency (MHz)	Part Number	C1 (pF)	C2 (pF)
Murata mfg.	12	CSA12.0MT	30	30
		CST12.0MTW	None (1)	None (1)
Kyocera Corp.	12	KBR12.0M	33	33

Notes:

(1) C1 and C2 are contained in the resonator.

Recommended Resonator Circuit



Ceramic or crystal resonator frequency f_{XX} = 4 to 12 MHz
External oscillation circuit should be as close to the X1 and X2 pins as possible
Do not place other signal lines in the shaded area

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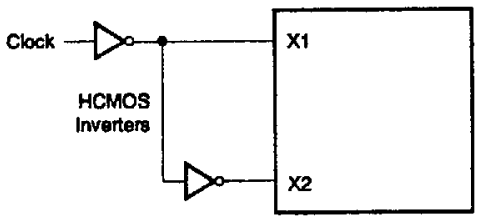
Recommended External Clock Circuit



Clock frequency f_{XX} = 4 to 12 MHz
In STOP mode, X1 is internally shorted to V_{SS} to prevent leakage current. Therefore, STOP mode is not available when using this external clock circuit.

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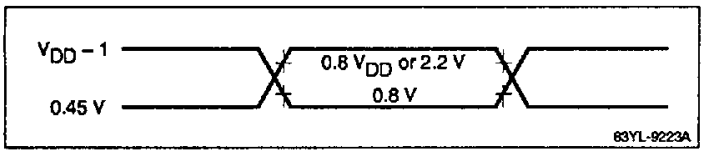
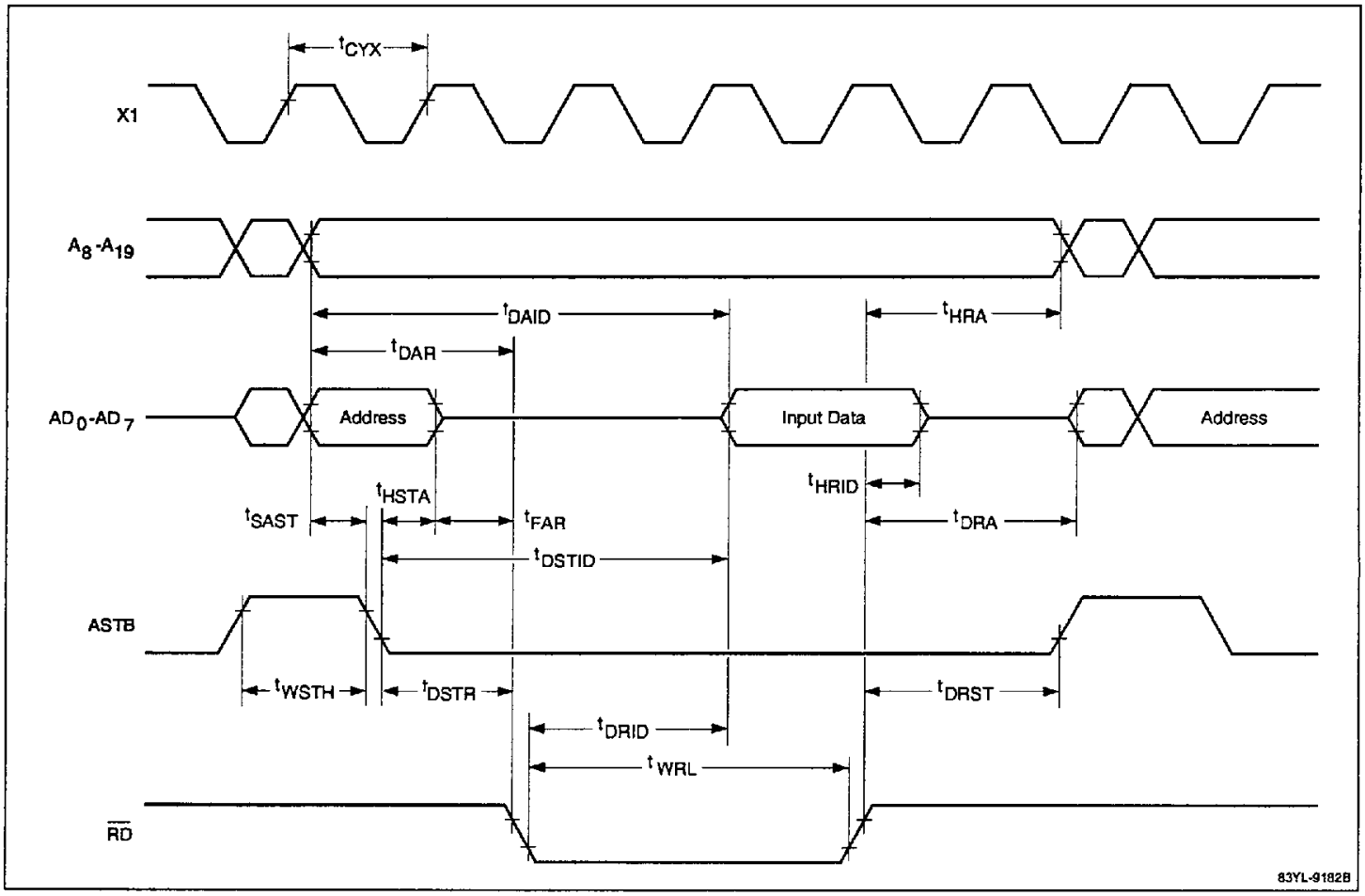
Timing Waveforms

Voltage Thresholds for AC Timing Measurements

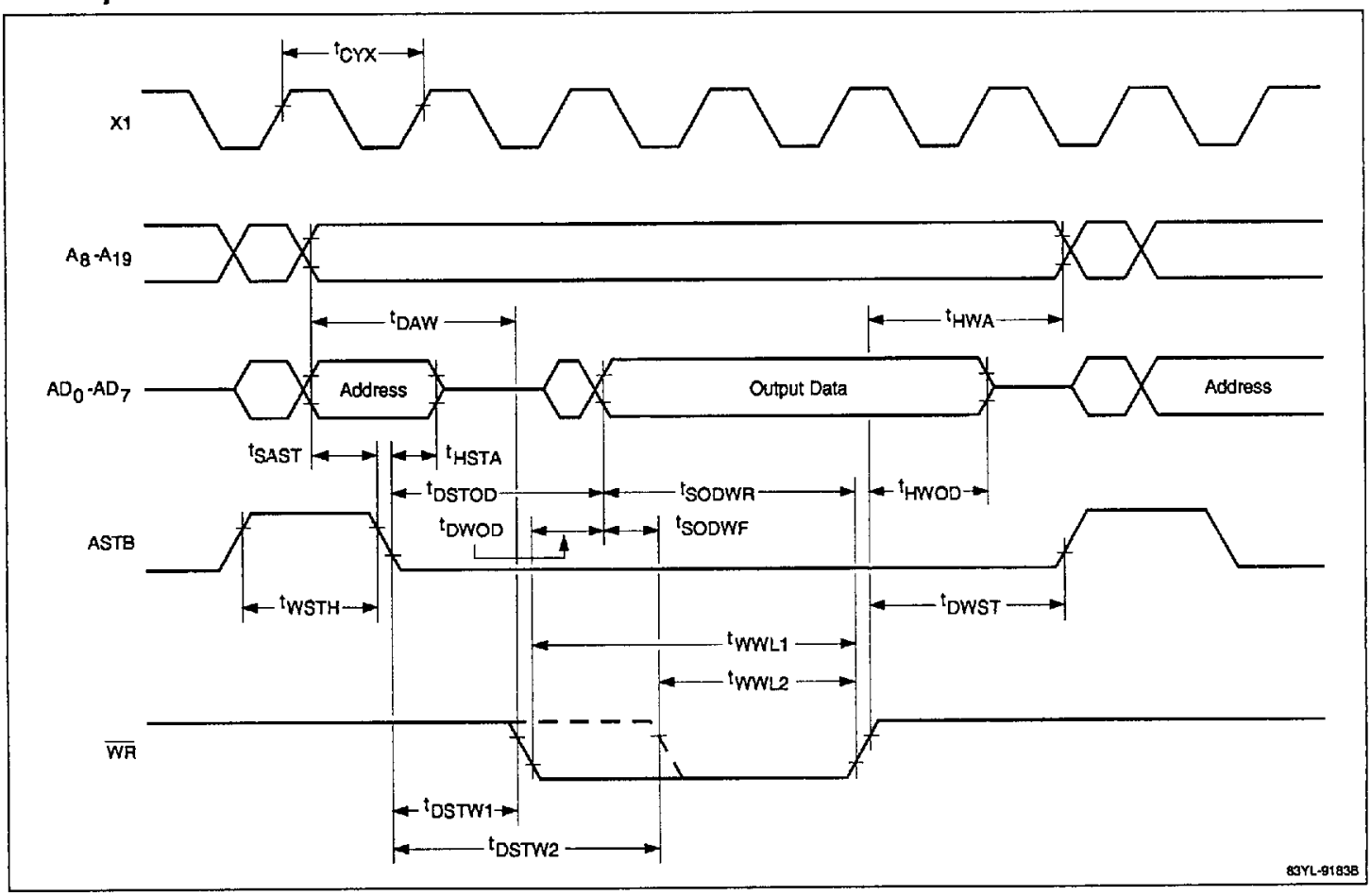


Read Operation



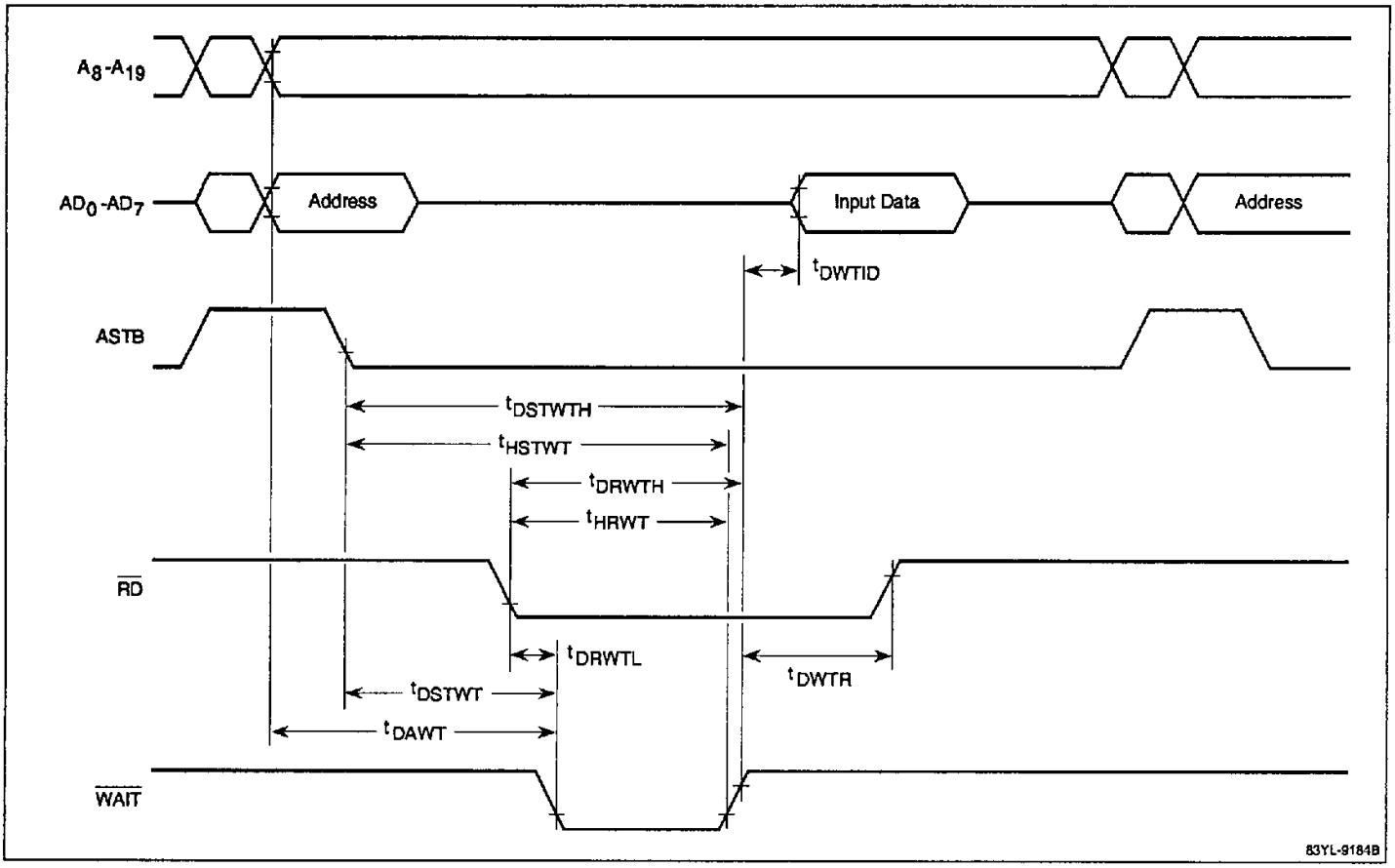
Timing Waveforms (cont)

Write Operation



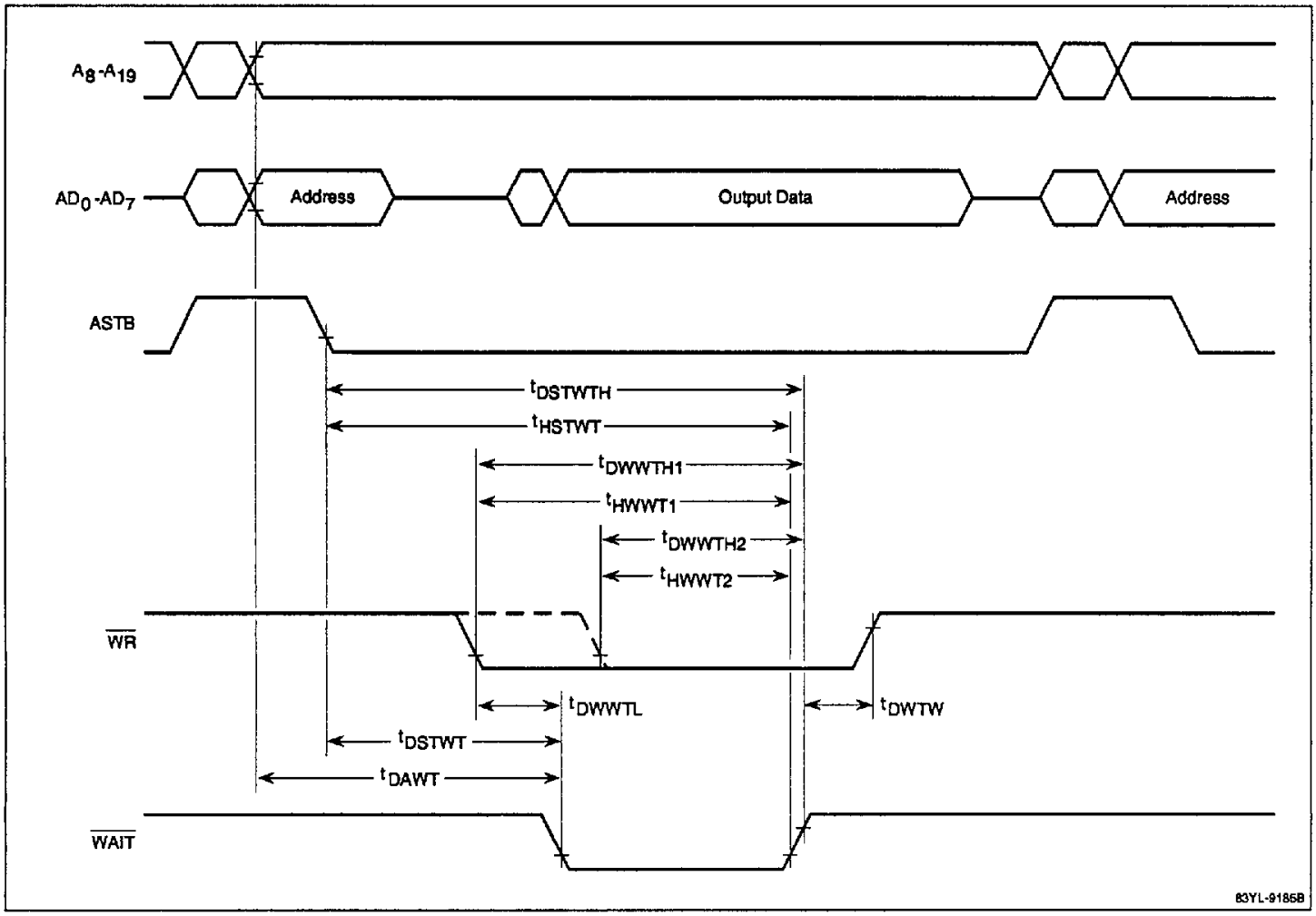
Timing Waveforms (cont)

External $\overline{WAIT}$ Signal Input (Read Operation)



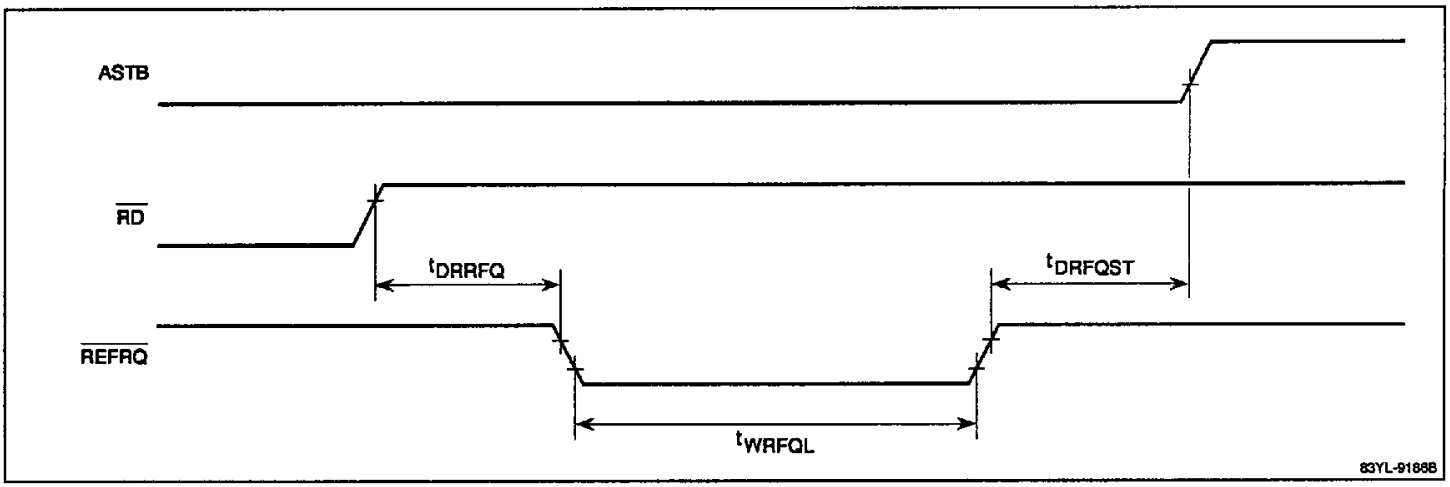
Timing Waveforms (cont)

External $\overline{WAIT}$ Signal Input (Write Operation)

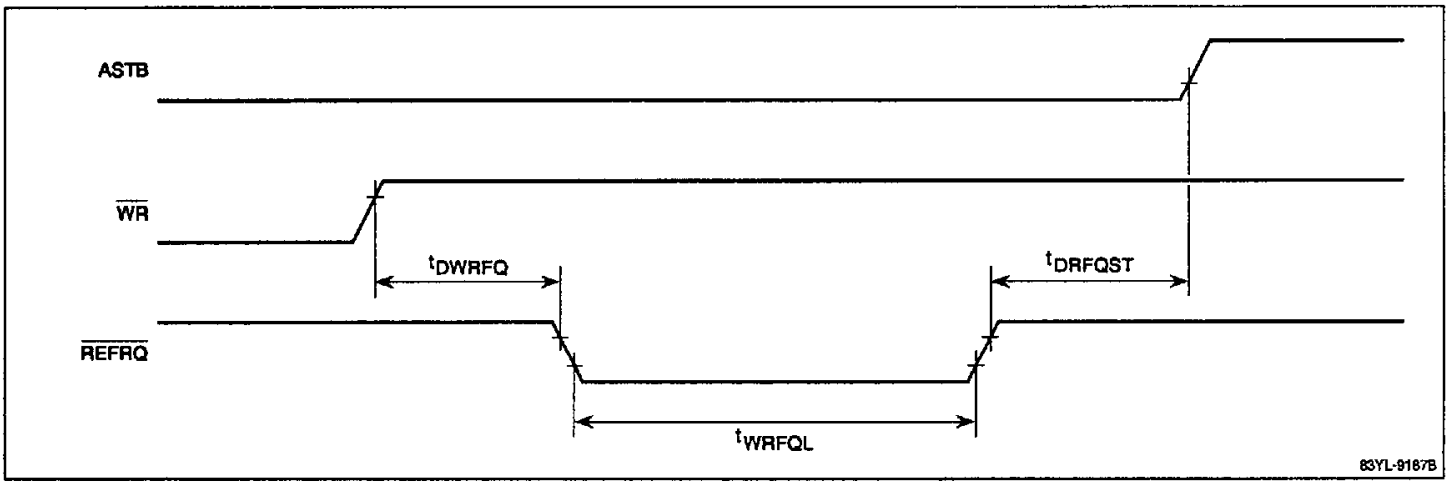


Timing Waveforms (cont)

Refresh After Read



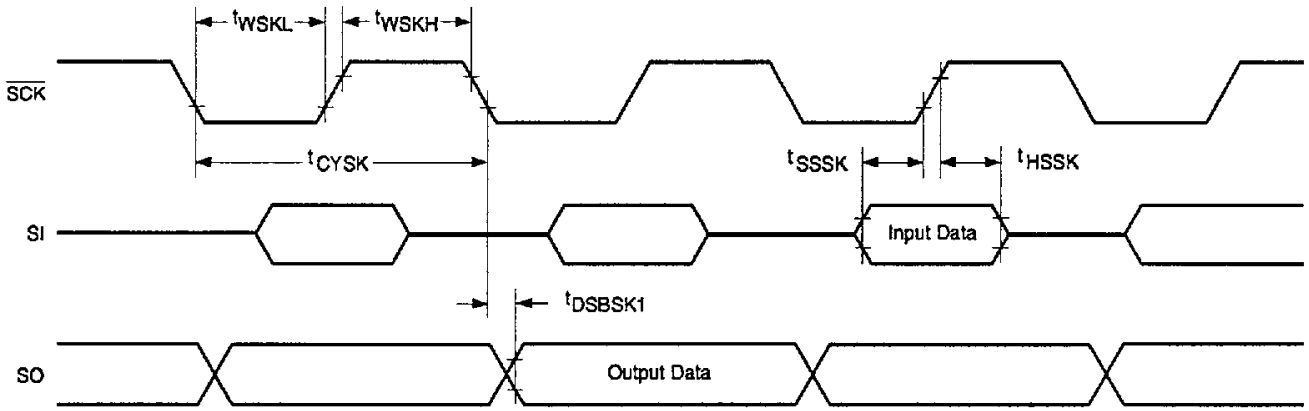
Refresh After Write



Timing Waveforms (cont)

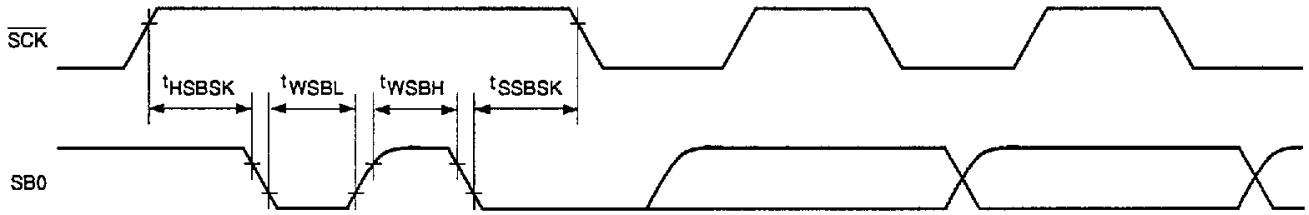
Serial Operation

Three-Line Serial I/O Timing

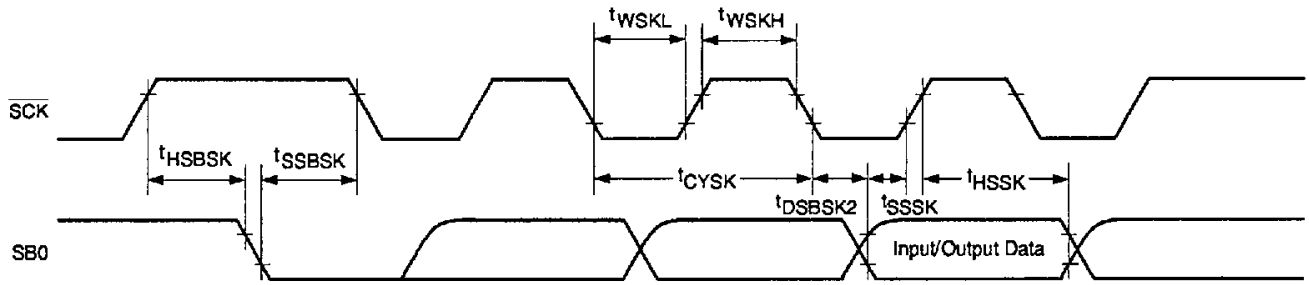


SBI Mode

Bus Release Signal Transfer Timing



Command Signal Transfer Timing



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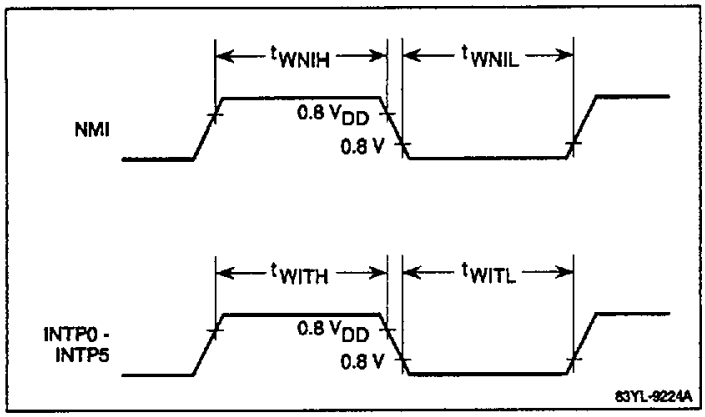
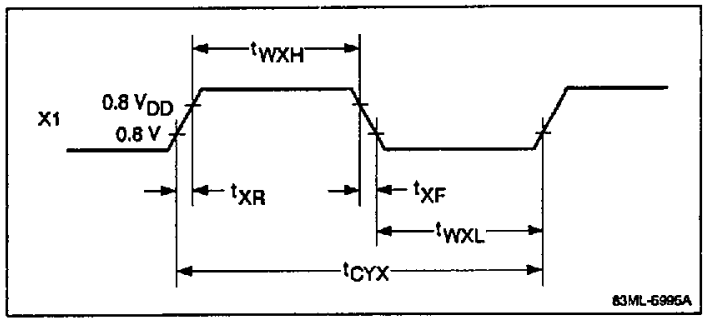
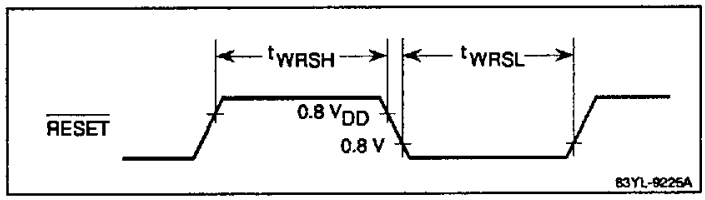
Interrupt Input



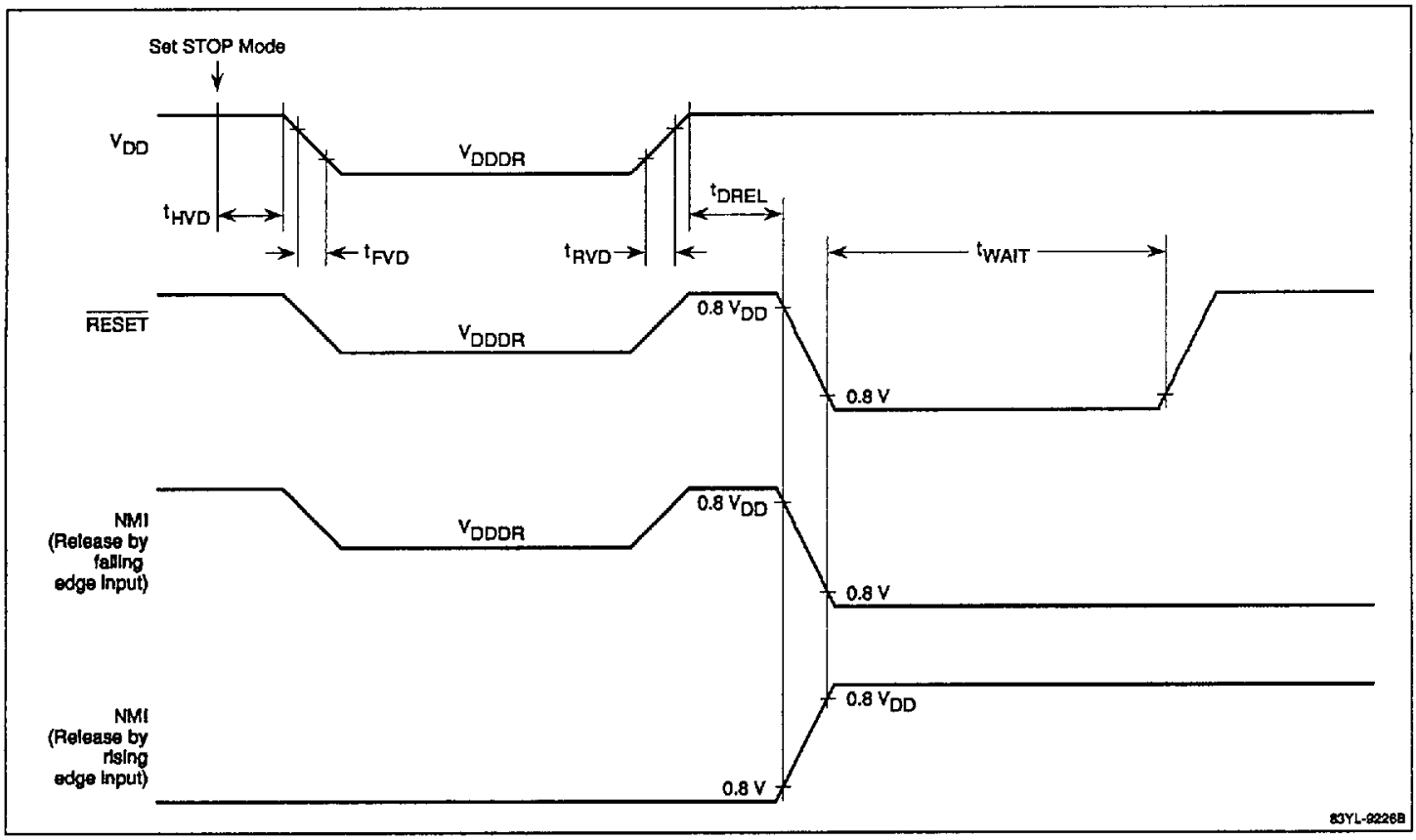
External Clock



Reset Input



Data Retention Characteristics



μPD78P238 PROGRAMMING

In the μPD78P238, the mask ROM of μPD78234 is replaced by a one-time programmable ROM (OTP ROM) or a reprogrammable, ultraviolet erasable ROM (UV EPROM). The ROM is 32K x 8 bits and can be programmed using a general-purpose PROM writer with a μPD27C256A programming mode.

The PA-78P238GC/GJ/LQ/KF are the socket adaptors used for configuring the μPD78P238 to fit a standard PROM socket.

Refer to tables 5 and 6 and figures 17 through 19 for special information applicable to PROM programming.

Table 5. Pin Functions During PROM Programming

Pin	Pin*	Function
$P0_0$ - $P0_7$	A_0 - A_7	Address input pins for PROM operations
$P5_0/A_8$	A_8	Address input pin for PROM operations
$P2_1$/INTP0	A_9	Address input pin for PROM operations
Pin	Pin*	Function

Table 5. Pin Functions During PROM Programming (cont)

Pin	Pin*	Function
Table 5. Pin Functions During PROM Programming		
Pin	Pin*	Function
$P5_2/A_{10}$ - $P5_6/A_{14}$	A_{10} - A_{14}	Address input pins for PROM operations
$P4_0/AD_0$ - $P4_7/AD_7$	D_0 - D_7	Data pins for PROM operations
$P6_5/\overline{WR}$	$\overline{CE}$	Strobes data into the PROM
$P6_4/\overline{RD}$	$\overline{OE}$	Enables a data read from the PROM
$\overline{RESET}$	$\overline{RESET}$	PROM programming mode requires applying a low voltage to this pin
MODE	V_{PP}	High voltage applied to this pin for program write/verify
V_{DD}	V_{DD}	Positive power supply pin
V_{SS}	V_{SS}	Ground

* Pin name in PROM programming mode.

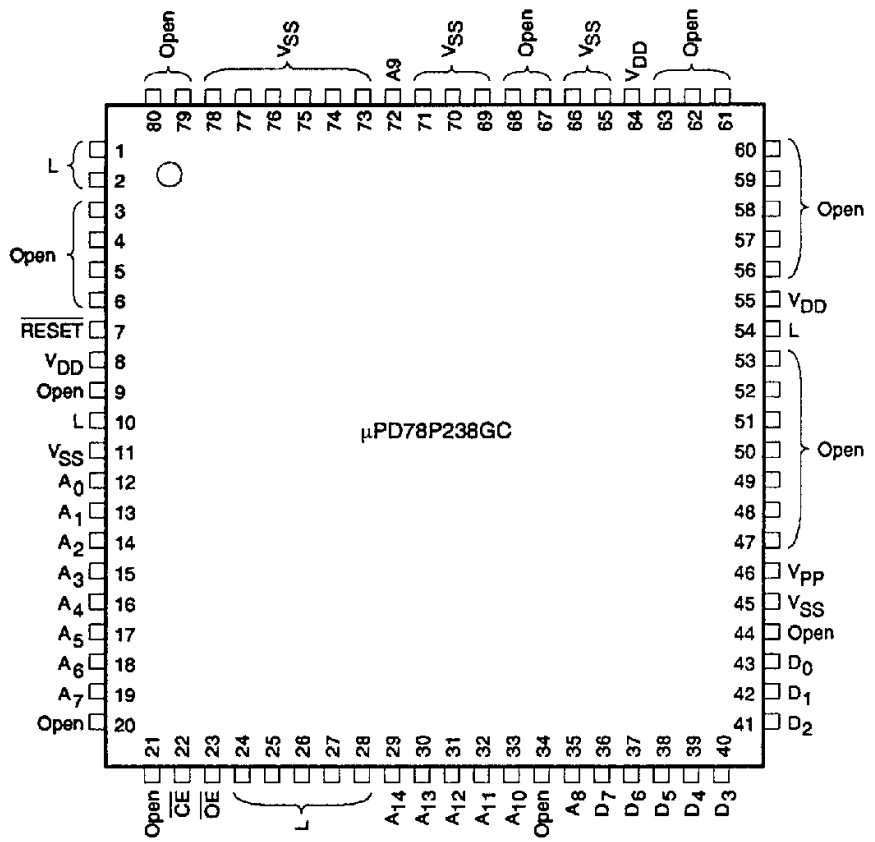
Table 6. Summary of Operation Modes for PROM Programming

Mode	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D_0 - D_7
Program write	L	L	H	+12.5 V	+6 V	Data input
Program verify	L	H	L	+12.5 V	+6 V	Data output
Program inhibit	L	H	H	+12.5 V	+6 V	High Z
Read out	L	L	L	+5 V	+5 V	Data output
Output disable	L	L	H	+5 V	+5 V	High Z
Standby	L	H	L/H	+5 V	+5 V	High Z

Note: When +12.5 V is applied to V_{PP} and +6 V to V_{DD}, both $\overline{CE}$ and $\overline{OE}$ cannot be set to low level (L) simultaneously.

Pin Functions in μPD78P238 PROM Programming Mode

Figure 17. 80-Pin Plastic QFP



Notes:

(1) L: Connect these pins separately to V_{SS} through resistors.

(2) V_{SS}: Connect these pins to V_{SS}.

(3) Open: Do not connect these pins.

(4) $\overline{RESET}$: Set to a low level.

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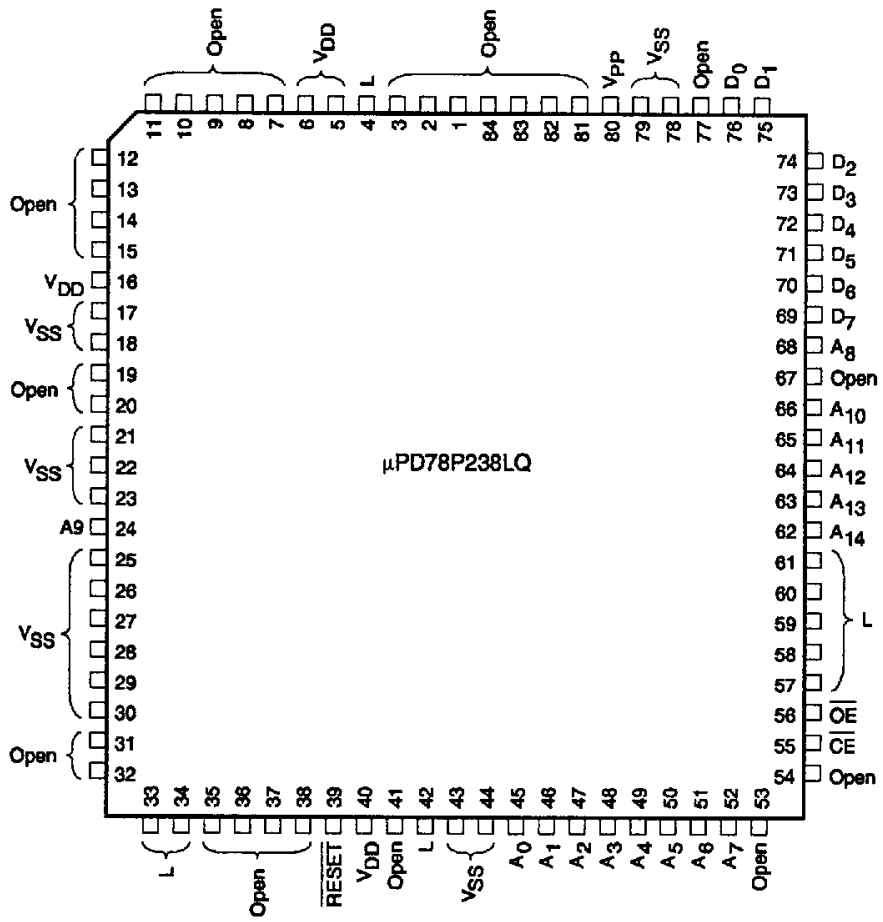
Pin Functions in μPD78P238 PROM Programming Mode (cont)

Figure 18. 84-Pin PLCC



Notes:

(1) L: Connect these pins separately to V_{SS} through resistors.

(2) V_{SS}: Connect these pins to V_{SS}.

(3) Open: Do not connect these pins.

(4) $\overline{RESET}$: Set to a low level.

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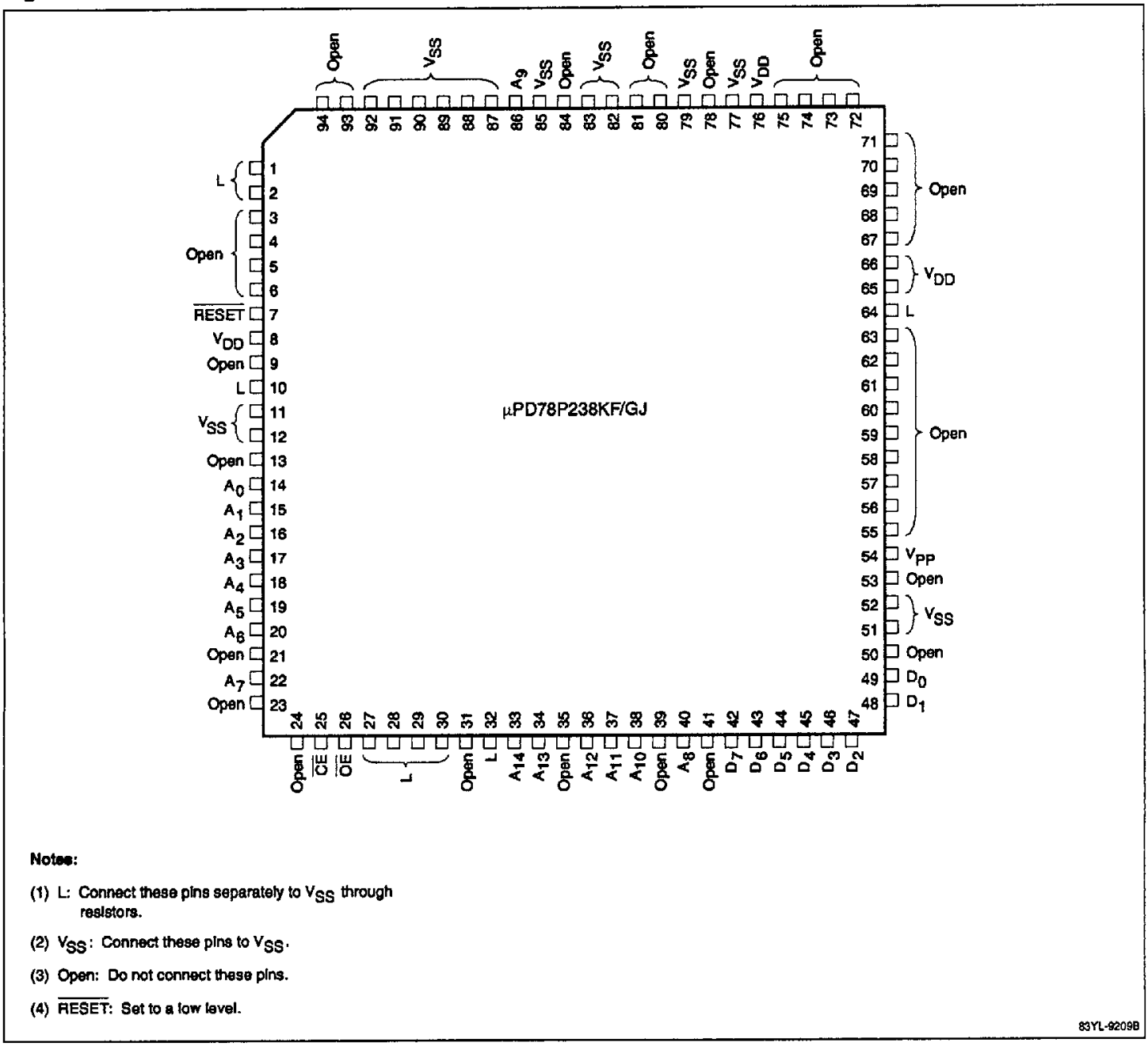
Pin Functions in μPD78P238 PROM Programming Mode (cont)

Figure 19. 94-Pin Plastic QFP 94-Pin Ceramic LCC with Window



Notes:

(1) L: Connect these pins separately to V_{SS} through resistors.

(2) V_{SS}: Connect these pins to V_{SS}.

(3) Open: Do not connect these pins.

(4) $\overline{RESET}$: Set to a low level.

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PROM Write Procedure

(1) Set the pins not used for programming as indicated in figures 17 through 19. Connect the $\overline{RESET}$ pin to a low level and apply +5 V to the V_{DD} and V_{PP} pin. The $\overline{CE}$ and $\overline{OE}$ pins should be high.

(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.

(3) Provide the initial address to the A_0 to A_{14} pins.

(4) Provide write data.

(5) Provide 1-ms program pulse (active low) to the $\overline{CE}$ pin.

(6) This data is now verified with a pulse (active low) to the $\overline{OE}$ pin. If the data has been written, proceed to step 8; if not, repeat steps 4 to 6. If the data cannot be correctly written after 25 attempts, go to step 7.

(7) Classify as defective and stop write operation.

(8) Provide write data and supply program pulse (for additional writing) for 3 ms times the number of writes performed in step 5.

(9) Increment the address.

(10) Repeat steps 4 to 9 until the end address.

PROM Read Procedure

(1) Set the pins not used for programming as indicated in figures 17 through 19. Fix the $\overline{RESET}$ pin to a low level and apply +5 V to the V_{DD} and V_{PP} pin. The $\overline{CE}$ and $\overline{OE}$ pins should be high.

(2) Input the address of the data to be read to pins A_0 - A_{14}.

(3) Read mode is entered with a pulse (active low) on both the $\overline{CE}$ and $\overline{OE}$ pins.

(4) Data is output to the D_0 to D_7 Pins.

EPROM Erasure

Data in an EPROM is erased by exposing the quartz window in the ceramic package to light having a wavelength shorter than 400 nm, including ultraviolet rays, direct sunlight, and fluorescent light. To prevent unintentional erasure, mask the window.

Typically, data is erased by 254-nm ultraviolet rays. A minimum lighting level of 15 Ws/cm² (ultraviolet ray intensity x exposure time) is required to completely erase written data. Erasure by an ultraviolet lamp rated at 12 mW/cm² takes approximately 15 to 20 minutes. Remove any filter on the lamp and place the device within 2.5 cm of the lamp tubes.

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DC Programming Characteristics

T_A = 25 ±5°C; V_{PP} ≥ 4.5 V; V_{SS} = 0 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH}	V_{IH}	2.4		V_{DDP}+0.3	V	
Low-level input voltage	V_{IL}	V_{IL}	-0.3		0.8	V	
Input leakage current	I_{LIP}	I_{LI}			10	μA	$0 \le V_I \le V_{DDP}$
High-level output voltage	V_{OH1}	V_{OH1}	2.4			V	I_{OH} = -400 μA
	V_{OH2}	V_{OH2}	V_{DD}-0.7			V	I_{OH} = -100 μA
Low-level output voltage	V_{OL}	V_{OL}			0.45	V	I_{OH} = 2.1 mA
Output leakage current	I_{LO}				10	μA	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}
V_{DDP} power voltage	V_{DDP}	V_{CC}	5.75	6.0	6.25	V	Program memory write mode
			4.5	5.0	5.5	V	Program memory read mode
V_{PP} power voltage	V_{PP}	V_{PP}	12.2	12.5	12.8	V	Program memory write mode
				V_{PP} = V_{DDP}		V	Program memory read mode
V_{DDP} power current	I_{DDP}	I_{CC}		5	30	mA	Program memory write mode
				5	30	mA	Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}
V_{PP} power current	I_{PP}	I_{PP}		5	30	mA	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}
				1	100	μA	Program memory read mode

* Corresponding symbols of the μPD27C256A.

AC Programming Characteristics (Write Mode)

T_A = 25 ±5°C; V_{PP} ≥ 4.5 V; V_{SS} = 0 V; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Conditions
Address setup time to $\overline{CE}$ ↓	t_{SAC}	t_{AS}	2			μs	
Data input to $\overline{OE}$ ↓ delay time	t_{HOID}	t_{OES}	2			μs	
Input data setup time to $\overline{CE}$ ↓	t_{SIDC}	t_{DS}	2			μs	
Address hold time from $\overline{CE}$ ↑	t_{HCA}	t_{AH}	2			μs	
Input data hold time from $\overline{CE}$ ↑	t_{HCID}	t_{DH}	2			μs	
Output data hold time from $\overline{OE}$ ↑	t_{HOOD}	t_{DF}	0		130	ns	
V_{PP} setup time to $\overline{CE}$ ↓	t_{SVPC}	t_{VPS}	1			ms	
V_{DDP} setup time to $\overline{CE}$ ↓	t_{SVDC}	t_{VCS}	1			ms	
Initial program pulse width	t_{WL1}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{WL2}	t_{OPW}	2.85		78.75	ms	
$\overline{OE}$ ↓ to data output time	t_{DOOD}	t_{OE}			150	ns	

* Corresponding symbols of the μPD27C256A.

AC Programming Characteristics (Read Mode)

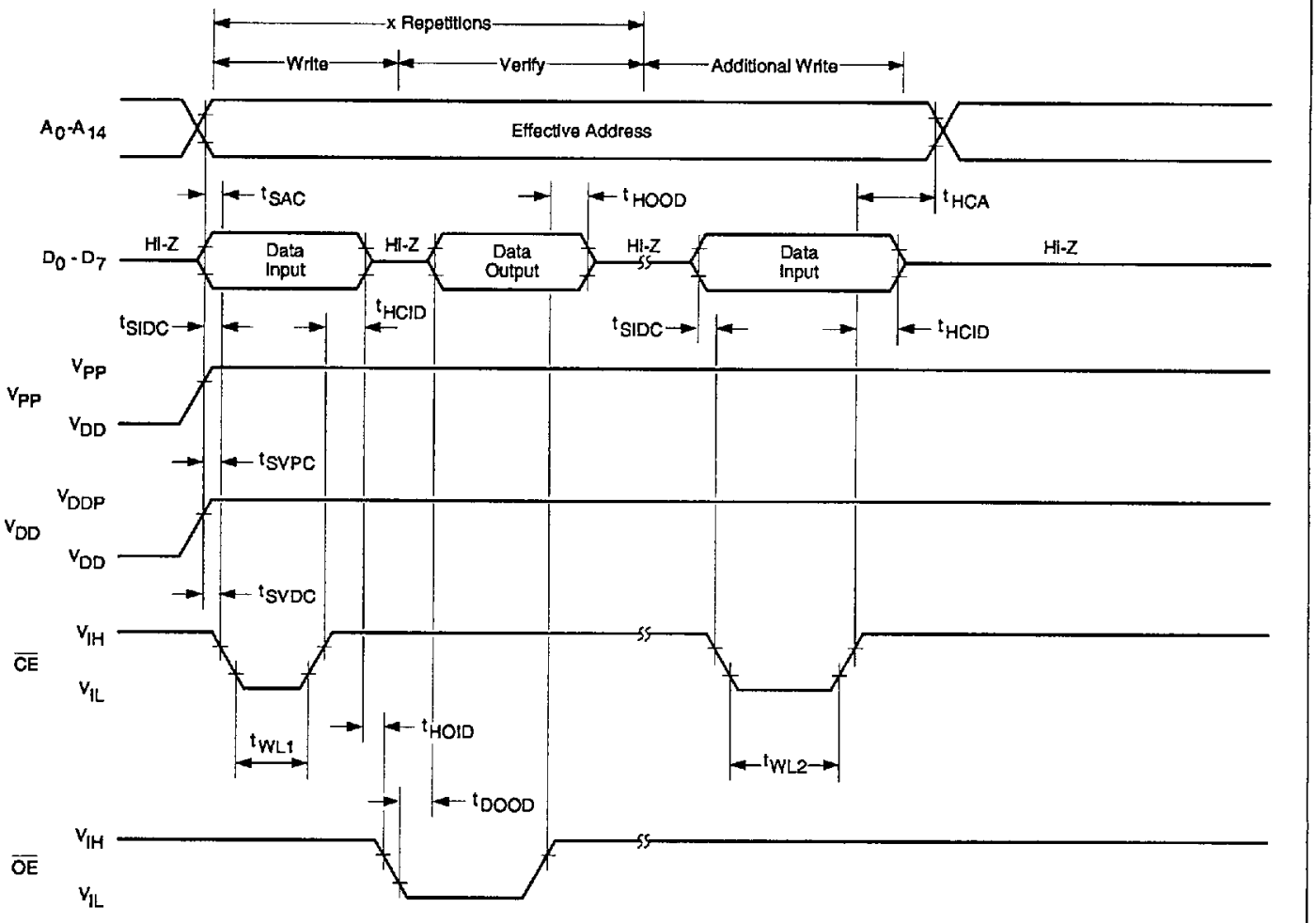
T_A = 25 ±5°C; V_{PP} ≥ 4.5 V; V_{PP} = 5 ±0.5 V; V_{PP} = V_{DDP}; V_{SS} = 0 V

Parameter	Symbol	Symbol*	Min	Typ	Max	Unit	Conditions
Address to data output time	t_{DAOD}	t_{ACC}			200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ ↓ to data output time	t_{DCOD}	t_{CE}			200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ ↓ to data output time	t_{DOOD}	t_{OE}			75	ns	$\overline{CE}$ = V_{IL}
Data hold time from $\overline{OE}$ ↑	t_{HCOD}	t_{DF}	0		60	ns	$\overline{CE}$ = V_{IL}
Data hold time from address	t_{HAOD}	t_{OH}	0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

* Corresponding symbols of the μPD27C256A.

PROM Timing Diagrams

PROM Write/Verify Mode



Notes:

(1) V_{DD} must be applied before applying V_{PP}. It should be removed after removing V_{PP}.

(2) V_{PP} must not exceed +13V, including overshoot.

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PROM Timing Diagrams (cont)

PROM Read Mode