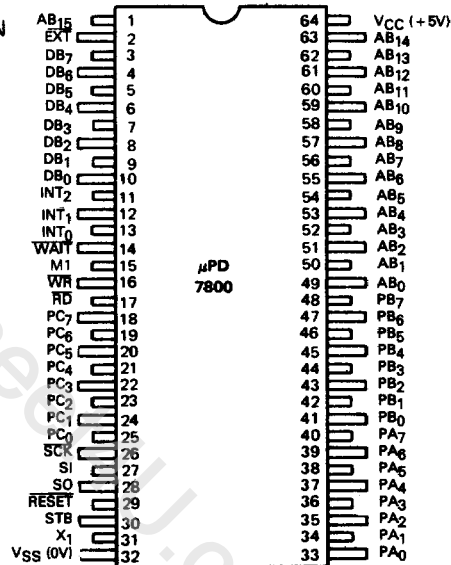


## HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

**DESCRIPTION** The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

- FEATURES**
- NMOS Silicon Gate Technology Requiring Single +5V Supply.
  - Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
    - 128 Bytes RAM
    - 32 I/O Lines
  - Internal 12-Bit Programmable Timer
  - On-Chip 1 MHz Serial Port
  - Five-Level Vectored, Prioritized Interrupt Structure
    - Serial Port
    - Timer
    - 3 External Interrupts
  - Bus Expansion Capabilities
    - Fully 8080A Bus Compatible
    - 64K Byte Memory Address Range
  - Wait State Capability
  - Alternate Z80™ Type Register Set
  - Powerful 140 Instruction Set
  - 8 Address Modes; Including Auto-Increment/Decrement
  - Multi-Level Stack Capabilities
  - Fast 2 μs Cycle Time
  - Bus Sharing Capabilities

PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

PIN NO	DESIGNATION	FUNCTION
1, 49-63	AB <sub>0</sub> -AB <sub>15</sub>	(Tri-State, Output) 16-bit address bus.
2	$\overline{\text{EXT}}$	(Output) $\overline{\text{EXT}}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{\text{EXT}}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB <sub>0</sub> -DB <sub>7</sub>	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT <sub>0</sub>	(Input, active high) Level-sensitive interrupt input.
12	INT <sub>1</sub>	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT <sub>2</sub>	(Input) INT <sub>2</sub> is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT <sub>2</sub> is rising edge sensitive. When ES is set to 0, INT <sub>2</sub> is falling edge sensitive.
14	$\overline{\text{WAIT}}$	(Input, active low) $\overline{\text{WAIT}}$ , when active, extends read or write timing to interface with slower external memory or I/O. $\overline{\text{WAIT}}$ is sampled at the end of T <sub>2</sub> , if active processor enters a wait state TW and remains in that state as long as $\overline{\text{WAIT}}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{\text{WR}}$	(Tri-State Output, active low) $\overline{\text{WR}}$ , when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{\text{WR}}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{\text{RD}}$	(Tri-State Output, active low) $\overline{\text{RD}}$ is used as a strobe to gate data from external devices on the data bus. $\overline{\text{RD}}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC <sub>0</sub> -PC <sub>7</sub>	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{\text{SCK}}$	(Input/Output) $\overline{\text{SCK}}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{\text{SCK}}$ .
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{\text{SCK}}$ , MSB to LSB.
29	$\overline{\text{RESET}}$	(Input, active low) $\overline{\text{RESET}}$ initializes the μPD 7800.
30	STB	(Output) Used to simulate μPD7801/7802 Port E operation, indicating that a Port E operation is being performed when active.
31	X <sub>1</sub>	(Input) Clock Input
33-40	PA <sub>0</sub> -PA <sub>7</sub>	(Output) 8-bit output port with latch capability.
41-48	PB <sub>0</sub> -PB <sub>7</sub>	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.



# μPD7800

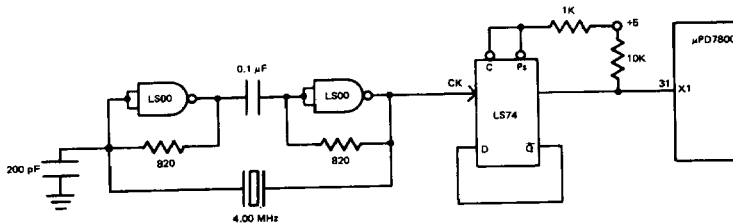
Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

## FUNCTIONAL DESCRIPTION

### μPD7800/7801 Functional Differences

1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB<sub>0</sub>-AB<sub>15</sub> is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.  
*PEX Instruction* — The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.  
*PEN Instruction* — B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.  
*PER Instruction* — The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X<sub>1</sub> input.
4. PIN 30. This pin functions as the X<sub>2</sub> crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation — indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. EXT is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

### RECOMMENDED CLOCK DRIVE CIRCUIT



**ABSOLUTE MAXIMUM RATINGS\***

Operating Temperature . . . . . **-10°C to +70°C**  
 Storage Temperature . . . . . **-65°C to +150°C**  
 Voltage On Any Pin . . . . . **-0.3V to +7.0V**

$T_a = 25^\circ\text{C}$

\*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC CHARACTERISTICS**

$T_a = -10^\circ\text{C} \sim +70^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 10\%$

PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V <sub>IL</sub>	0		0.8	V	
Input High Voltage	V <sub>IH1</sub>	2.0		V <sub>CC</sub>	V	Except SCK, X1
	V <sub>IH2</sub>	3.8		V <sub>CC</sub>	V	SCK, X1
Output Low Voltage	V <sub>OL</sub>			0.45	V	I <sub>OL</sub> = 2.0 mA
Output High Voltage	V <sub>OH1</sub>	2.4			V	I <sub>OH</sub> = -100 μA
	V <sub>OH2</sub>	2.0			V	I <sub>OH</sub> = -500 μA
Low Level Input Leakage Current	I <sub>LIL</sub>			-10	μA	V <sub>IN</sub> = 0V
High Level Input Leakage Current	I <sub>LIH</sub>			10	μA	V <sub>IN</sub> = V <sub>CC</sub>
Low Level Output Leakage Current	I <sub>LOL</sub>			-10	μA	V <sub>OUT</sub> = 0.45V
High Level Output Leakage Current	I <sub>LOH</sub>			10	μA	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>CC</sub> Power Supply Current	I <sub>CC</sub>		110	200	mA	



**CAPACITANCE**

$T_a = 25^\circ\text{C}$ ,  $V_{CC} = \text{GND} = 0\text{V}$

PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C <sub>I</sub>			10	pF	f <sub>c</sub> = 1 MHz All pins not under test at 0V
Output Capacitance	C <sub>O</sub>			20	pF	
Input/Output Capacitance	C <sub>IO</sub>			20	pF	

T<sub>a</sub> = -10°C to +70°C, V<sub>CC</sub> = +5.0V ± 10%

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
X <sub>OUT</sub> Cycle Time	t <sub>CYX</sub>	454	2000	ns	t <sub>CYX</sub>
X <sub>OUT</sub> Low Level Width	t <sub>XXL</sub>	212		ns	t <sub>XXL</sub>
X <sub>OUT</sub> High Level Width	t <sub>XXH</sub>	212		ns	t <sub>XXH</sub>

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
RD L.E. → X <sub>OUT</sub> L.E.	t <sub>RX</sub>	20		ns	t <sub>CYX</sub> = 500 ns
Address (PE <sub>0-15</sub> ) → Data Input	t <sub>AD1</sub>		550 + 500 x N	ns	
RD T.E. → Address	t <sub>RA</sub>	200(T3); 700(T4)		ns	
RD L.E. → Data Input	t <sub>RD</sub>		350 + 500 x N	ns	
RD T.E. → Data Hold Time	t <sub>RDH</sub>	0		ns	
RD Low Level Width	t <sub>RR</sub>	850 + 500 x N		ns	
RD L.E. → WAIT L.E.	t <sub>RWT</sub>		450	ns	
Address (PE <sub>0-15</sub> ) → WAIT L.E.	t <sub>AWT1</sub>		650	ns	
WAIT Set Up Time (Referenced from X <sub>OUT</sub> L.E.)	t <sub>WTS</sub>	180		ns	
WAIT Hold Time (Referenced from X <sub>OUT</sub> L.E.)	t <sub>WTH</sub>	0	120	ns	
M1 → RD L.E.	t <sub>MR</sub>	200		ns	
RD T.E. → M1	t <sub>RM</sub>	200		ns	
IO/M → RD L.E.	t <sub>IR</sub>	200		ns	
RD T.E. → IO/M	t <sub>RI</sub>	200		ns	
X <sub>OUT</sub> L.E. → WR L.E.	t <sub>XW</sub>		270	ns	
Address (PE <sub>0-15</sub> ) → X <sub>OUT</sub> T.E.	t <sub>AX</sub>		300	ns	
Address (PE <sub>0-15</sub> ) → Data Output	t <sub>AD2</sub>	450		ns	
Data Output → WR T.E.	t <sub>DW</sub>	600 + 500 x N		ns	
WR T.E. → Data Stabilization Time	t <sub>WD</sub>	150		ns	
Address (PE <sub>0-15</sub> ) → WR L.E.	t <sub>AW</sub>	400		ns	
WR T.E. → Address Stabilization Time	t <sub>WA</sub>	200		ns	
WR Low Level Width	t <sub>WW</sub>	600 + 500 x N		ns	
IO/M → WR L.E.	t <sub>IW</sub>	500		ns	
WR T.E. → IO/M	t <sub>WI</sub>	250		ns	

AC CHARACTERISTICS  
(CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
SCK Cycle Time	t <sub>CYK</sub>	800		ns	SCK Input
		900	4000	ns	SCK Output
SCK Low Level Width	t <sub>KKL</sub>	350		ns	SCK Input
		400		ns	SCK Output
SCK High Level Width	t <sub>KKH</sub>	350		ns	SCK Input
		400		ns	SCK Output
SI Set-Up Time (referenced from SCK T.E.)	t <sub>SIS</sub>	80		ns	
SI Hold Time (referenced from SCK T.E.)	t <sub>SIH</sub>	260		ns	
SCK L.E. → SO Delay Time	t <sub>KO</sub>		180	ns	
SCS High → SCK L.E.	t <sub>CSK</sub>	100		ns	
SCK T.E. → SCS Low	t <sub>KCS</sub>	100		ns	
SCK T.E. → SAK Low	t <sub>KSA</sub>		260	ns	

PEN, PEX, PER OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X <sub>1</sub> L.E. → EXT	t <sub>XE</sub>		250	ns	t <sub>CYX</sub> = 500 ns
Address (AB <sub>0-15</sub> ) → STB L.E.	t <sub>AST</sub>	200			
Data (DB <sub>0-7</sub> ) → STB L.E.	t <sub>DST</sub>	200			
STB Hold Time	t <sub>STST</sub>	300			
STB → Data	t <sub>STD</sub>	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X <sub>OUT</sub> L.E.)	t <sub>HDS<sub>1</sub></sub>	100		ns	
	t <sub>HDS<sub>2</sub></sub>	100		ns	
HOLD Hold Time (referenced from Ø <sub>OUT</sub> L.E.)	t <sub>HDH</sub>	100		ns	
X <sub>OUT</sub> L.E. → HLDA	t <sub>XHA</sub>		100	ns	
HLDA High → Bus Floating (High Z State)	t <sub>HABF</sub>	-150	150	ns	
HLDA Low → Bus Enable	t <sub>HABE</sub>		350	ns	

Notes:

- ① AC Signal waveform (unless otherwise specified)



- ② Output Timing is measured with 1 TTL + 200 pF measuring points are V<sub>OH</sub> = 2.0V  
V<sub>OL</sub> = 0.8V
- ③ L.E. = Leading Edge, T.E. = Trailing Edge

**t<sub>CYX</sub> DEPENDENT AC PARAMETERS**

**AC CHARACTERISTICS  
(CONT.)**

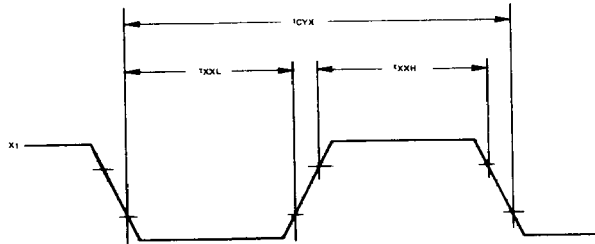
PARAMETER	EQUATION	MIN/MAX	UNIT
t <sub>RX</sub>	(1/25) T	MIN	ns
t <sub>AD1</sub>	(3/2 + N) T - 200	MAX	ns
t <sub>RA (T3)</sub>	(1/2) T - 50	MIN	ns
t <sub>RA (T4)</sub>	(3/2) T - 50	MIN	ns
t <sub>RD</sub>	(1 + N) T - 150	MAX	ns
t <sub>RR</sub>	(2 + N) T - 150	MIN	ns
t <sub>RWT</sub>	(3/2) T - 300	MAX	ns
t <sub>AWT1</sub>	(2) T - 350	MIN	ns
t <sub>MR</sub>	(1/2) T - 50	MIN	ns
t <sub>RM</sub>	(1/2) T - 50	MIN	ns
t <sub>IR</sub>	(1/2) T - 50	MIN	ns
t <sub>RI</sub>	(1/2) T - 50	MIN	ns
t <sub>XW</sub>	(27/50) T	MAX	ns
t <sub>AD2</sub>	T - 50	MIN	ns
t <sub>DW</sub>	(3/2 + N) T - 150	MIN	ns
t <sub>WD</sub>	(1/2) T - 100	MIN	ns
t <sub>AW</sub>	T - 100	MIN	ns
t <sub>WA</sub>	(1/2) T - 50	MIN	ns
t <sub>WW</sub>	(3/2 + N) T - 150	MIN	ns
t <sub>IW</sub>	T	MIN	ns
t <sub>WI</sub>	(1/2) T	MIN	ns
t <sub>HABE</sub>	(1/2) T - 150	MAX	ns
t <sub>AST</sub>	(2/5) T	MIN	ns
t <sub>DST</sub>	(2/5) T	MIN	ns
t <sub>STST</sub>	(3/5) T	MIN	ns
t <sub>STD</sub>	(4/5) T	MIN	ns

- Notes: ① N = Number of Wait States  
 ② T = t<sub>CYX</sub>  
 ③ Only above parameters are t<sub>CYX</sub> dependent  
 ④ When a crystal frequency other than 4 MHz is used (t<sub>CYX</sub> = 500 ns) the above equations can be used to calculate AC parameter values.

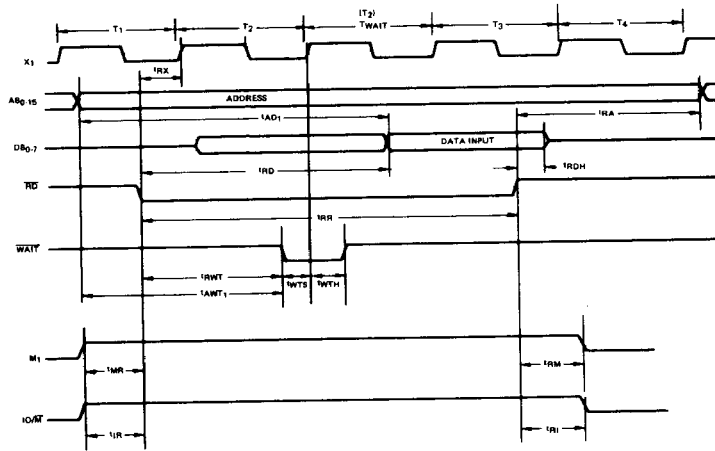


TIMING WAVEFORMS

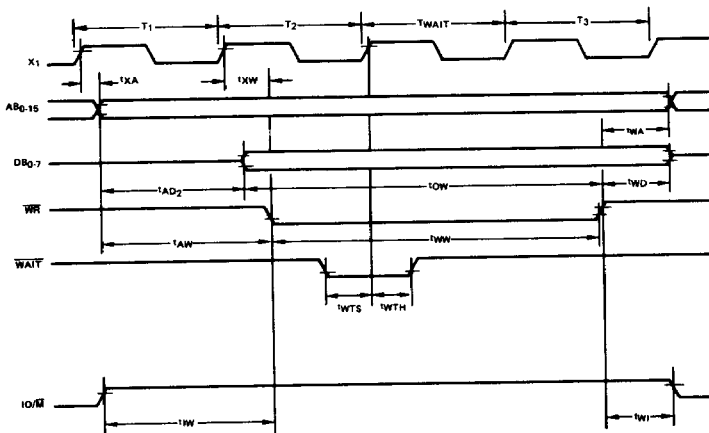
CLOCK TIMING



READ OPERATION

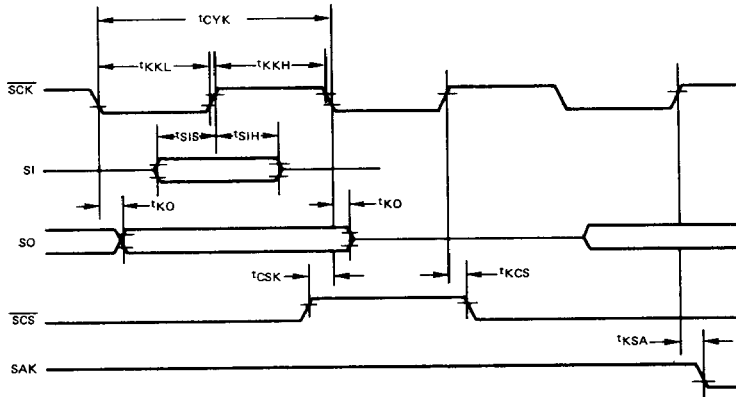


WRITE OPERATION

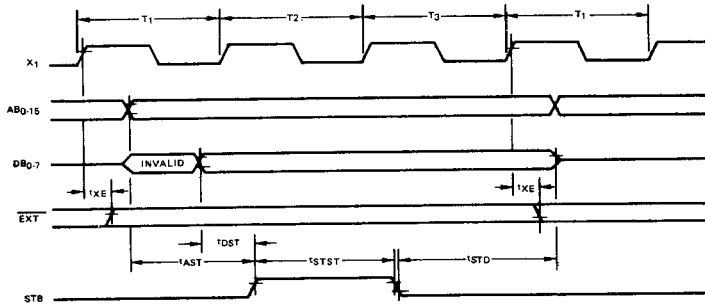


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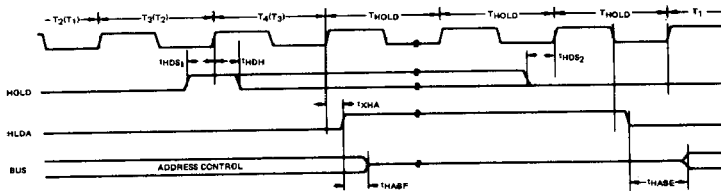
**SERIAL I/O OPERATION**



**PEN, PEX, PER OPERATION**



**HOLD OPERATION**



**Package Outlines**

For information, see Package Outline Section 7.

Plastic Quill, μPD7800G