



## STA013 MPEG 2.5 LAYER III SOURCE DECODER

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*This Application Note helps the user to work with STA013 Evaluation Board, installing the PC Software Driver, understanding how STA013 MPEG 2.5 Layer III Source Decoder works, and explaining how to control the device functions.*

*The document is composed by 5 main points:*

- **MPEG 2.5 Layer III Technical Introduction**
- **STA013 Device Description**
- **STA013 Evaluation Board Description**
- **STA013 PC Software Driver Description**
- **General Information on STA013 Evaluation Environment**

### MPEG 2.5 LAYER III TECHNICAL INTRODUCTION

#### An Overview

Since 1988 MPEG group has been working on the standardisation of high-quality low-bitrate audio coding techniques. Two standards have been completed: MPEG 1 (coding of mono and stereo signals at sampling rates of 32, 44.1, and 48 KHz) and MPEG 2 (backward-compatible coding of 5+1 multichannel sound signals and low-bitrate coding of mono and stereo at sampling rates of 16, 22.05, 24 KHz).

A non standardized evolution of MPEG 2 has been developed by industry, called MPEG 2.5.

It is practically the extension to the sampling rates 8, 11.025, and 12 KHz, of the current MPEG 2 standard.

The basic idea behind perceptual coding, the general audio coding theory implemented by MPEG, is to hide the quantisation noise below the signal-dependent thresholds of hearing. In this view, the most important question in perceptual coding is: "how much noise can be introduced to the signal without being audible?". The most prominent feature in psychoacoustics is masking in the frequency domain. A fainter signal is completely masked by a masker that is louder and has a similar frequency content.

The overall processing chain of an MPEG encoder can be summarised in the following four steps:

- A filter bank is used to decompose the input signal into subsampled spectral components (time to frequency domain). Together with the corresponding filter bank in the decoder it forms an analysis-synthesis system.
- Using either the time-domain input signal or the output of the analysis filter bank, an estimate of the actual (time-dependent) masked threshold is computed using rules known from psychoacoustic. This is called the perceptual encoding system.
- The spectral components are quantized and coded with the aim of keeping the noise, which is introduced by quantizing, below the masking threshold. Depending on the algorithm, this step is done in different ways, from simple block companding to analysis-by-synthesis system using additional noiseless compression.
- A bitstream formatter is used to assemble the bitstream, which typically consists of the quantized and coded spectral coefficients and some side information, such as bit allocation information.

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### The Layers

Recognizing a variety of application needs, the concept of a generic coding system was envisaged. Depending on the application, one of the three layers of the coding system with increasing complexity and performances is chosen. In all the three layers the input PCM audio signal is converted from the time into a time-frequency domain.

This is done by a poliphase filter bank consisting of 32 subbands.

In Layer I and II, a filter bank creates 32 subbands representation of the input audio stream, which are then quantized and coded under control of the psychoacoustic model from which a blockwise adaptive bit allocation is derived.

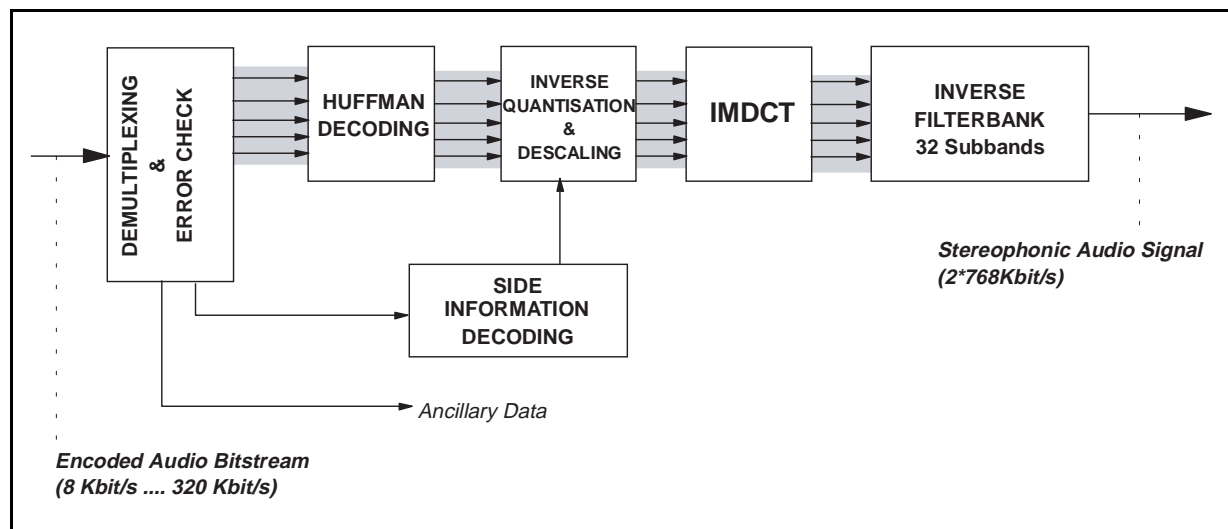
Layer I is a simplified version of the MUSICAM coding scheme, most appropriate for consumer applications, where the very low bitrate is not mandatory.

Layer II introduces further compression with respect to Layer I, by redundancy and irrelevance removal on the scale factors, and it uses more precise quantisation.

Layer III consists of a combination of the most effective modules of the ASPEC and MUSICAM coding schemes. Additional frequency resolution is provided by the use of a hybrid filter bank. Every subband is thereby further split into higher resolution frequency lines by a MDCT that operates on 18 subband samples in each subband. The frame length is 24 ms, identical to Layer II. In Layer III, nonuniform quantisation, adaptive segmentation, and entropy coding of the quantized values are employed for better coding efficiency. The basic block diagram of a Layer III Decoder is described in Fig. 1.

Layer III uses a short-term buffer to help the system cope with the short term difference in the bit rate demand. Only Layer III may operate in a variable rate mode, without violating the minimum requirements of the standard. This layer is most useful in telecommunication, in particular with narrow band ISDN, satellite links, and in all cases where the best quality at low bitrates is mandatory.

**Figure 1: STA013 Block Diagram**

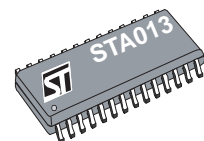


### STA013 DEVICE DESCRIPTION

The STA013 is an MPEG 2.5 Layer III Audio Decoder capable of decoding elementary streams from 8 up to 320 Kbit/sec.

The full sampling frequencies range is supported, from 8 up to 48 KHz. For this reason we use the name "MPEG 2.5".

- Supports all ISO Layer III Functionalities and WorldSpace Extensions.
- Programmable Input Data Interface.
- Programmable Audio Data Interface.
- Automatic Output Sampling Rate Generation.
- Programmable Oversampling Clock Frequency for DAC.



- Automatic MPEG Synchronisation, Sync Error Detection and Bistream Error Detection.
- Automatic Error Cancelment Techniques.
- Automatic DSP Speed Regulation for Power Consumption Optimisation.
- Low Power 3.0V and CMOS Technology.
- 10, 14.31818, 14.7456 MHz Input Clock.

STA013 can decode Layer III compressed streams only, because the lower layers I and II are not supported by this device.

It is particularly suitable for Multimedia application, because it can drive the data demand by a dedicated pin. This signal can be used by the system controller to synchronize the data to STA013 input port.

It can work with three different standard commercial crystals, 10.00, 14.31818, and 14,7456 MHz.

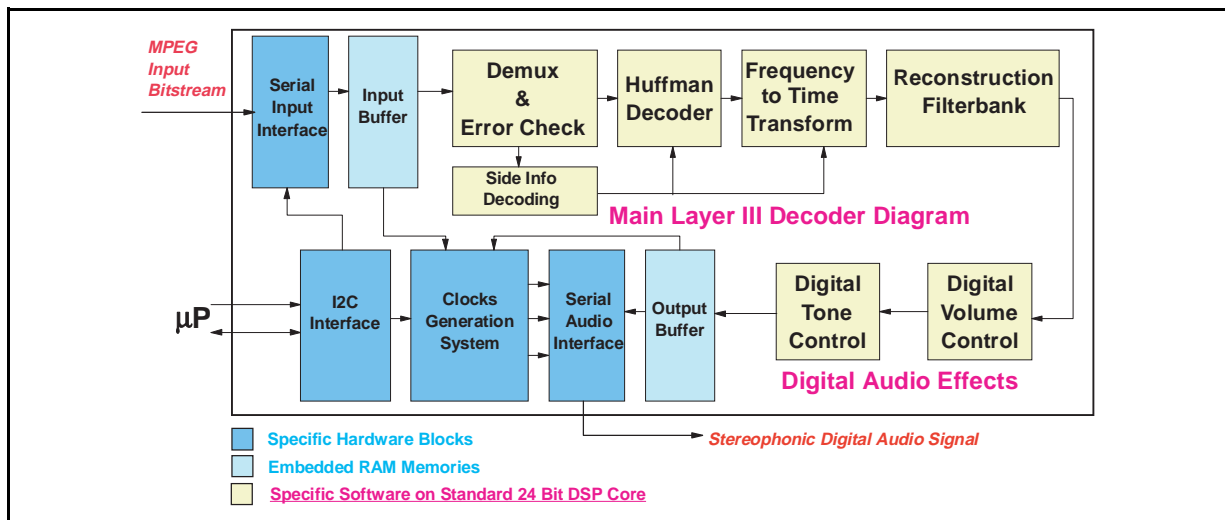
The device can perform both digital Volume and Tone Control, avoiding the use of the correspondent analog components on the application.

The most important DAC data format (I2S, etc.) are supported.

The Figure 2 describes the STA013 chip partitioning.

For any other technical information, refer to STA013 data sheet.

**Figure 2. STA013 Chip Partitioning**



**STA013 EVALUATION BOARD DESCRIPTION**

(see Figure 4 Electrical Schematic and Figure 3 Functional Diagram)

The STA013 Evaluation Board (STA013EVB) is useful to perform functional verification of the device operation.

The board is connected to an external data source by means of the **Input Connector** which provides to the user the connection points in order to input the serial data to STA013 and to control the input data flow speed. The **Input Connector** is indicated on STA013EVB with J6. The Serial Input Clock line for STA013 has to be connected to pin no. 1 of J6. On the STA013EVB, it is connected to pin no. 6 of STA013 (SCKR). The polarity of the STA013 receiver clock can be programmed, as described in the data sheet.

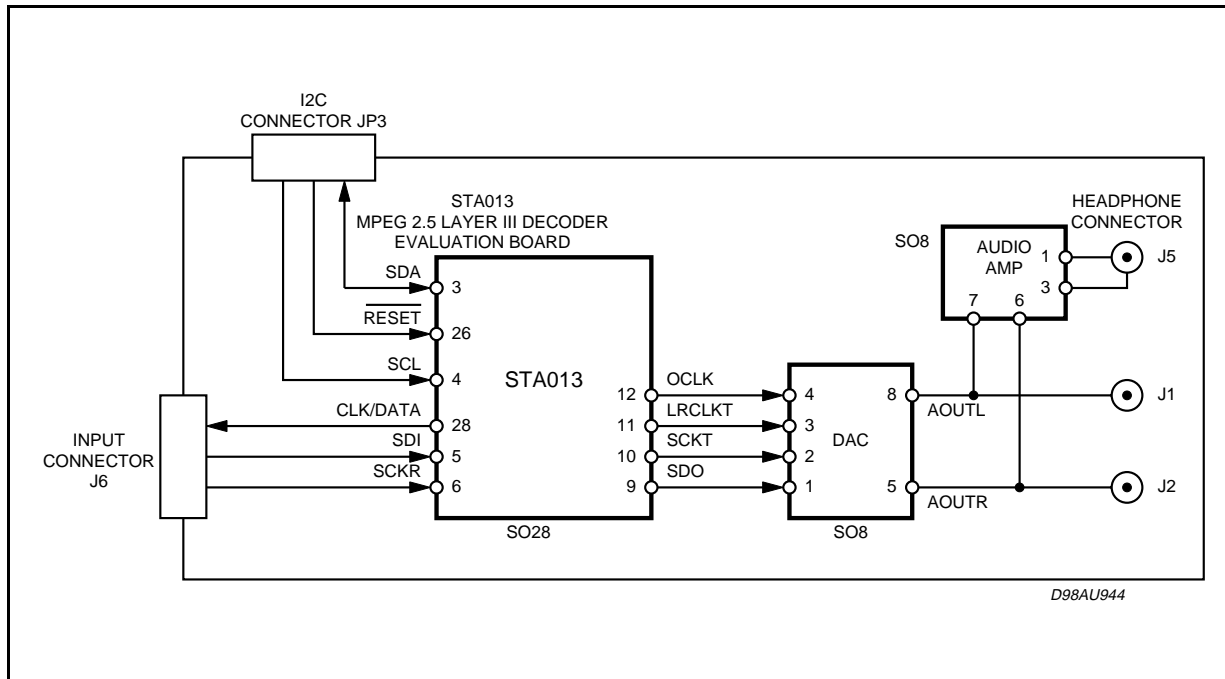
The Serial Input Data line for STA013 has to be connected pin 2 of J6. The speed of input data can be controlled by the DATA\_REQ signal of STA013 (pin no. 28) and it is connected on STA013EVB to pin 4 of J6.

The STA013EVB **I2C Connector** (JP3) is used to interface the PC interface board to STA013. The JP3 connection point no. 2 is connected to pin 4 of STA013 and is the I2C Serial Clock line (SCL). The maximum speed for this clock is 400 KHz, as specified by I2C standard.

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The JP3 connection point no. 3 is connected to pin no. 3 of STA013 and is the I2C Serial Data line (SDA). The STA013 I2C interface is used to:

**Figure 3. STA013EVB Functional Diagram**



- Bootstrap the device by downloading the appropriate configuration file. This is done to program STA013 working with one of the three possible crystal frequencies, to select the appropriate output data format depending on the DAC used in the other application.
- Monitor STA013 decoding operation. It is possible to read in real time all the audio program information, as sampling frequency, channels configuration, input bitstream speed, device interface configuration, and ancillary data.
- Control STA013 operation. The device implements a fully Digital Volume and Tone Control with parameters programmable via I2C interface. A microcontroller, connected to STA013 I2C interface, can change the parameters to control the volume level, the tones configurations, and the output data format.

The STA013EVB can be used by connecting the I2C port to the Parallel Port of a commercial PC. The I2C protocol is emulated by a dedicated PC Software Driver (STA013SDR) allowing the user to have on STA013 a full control. STA013SDR has a graphical user interface for an easy control of the device functions.

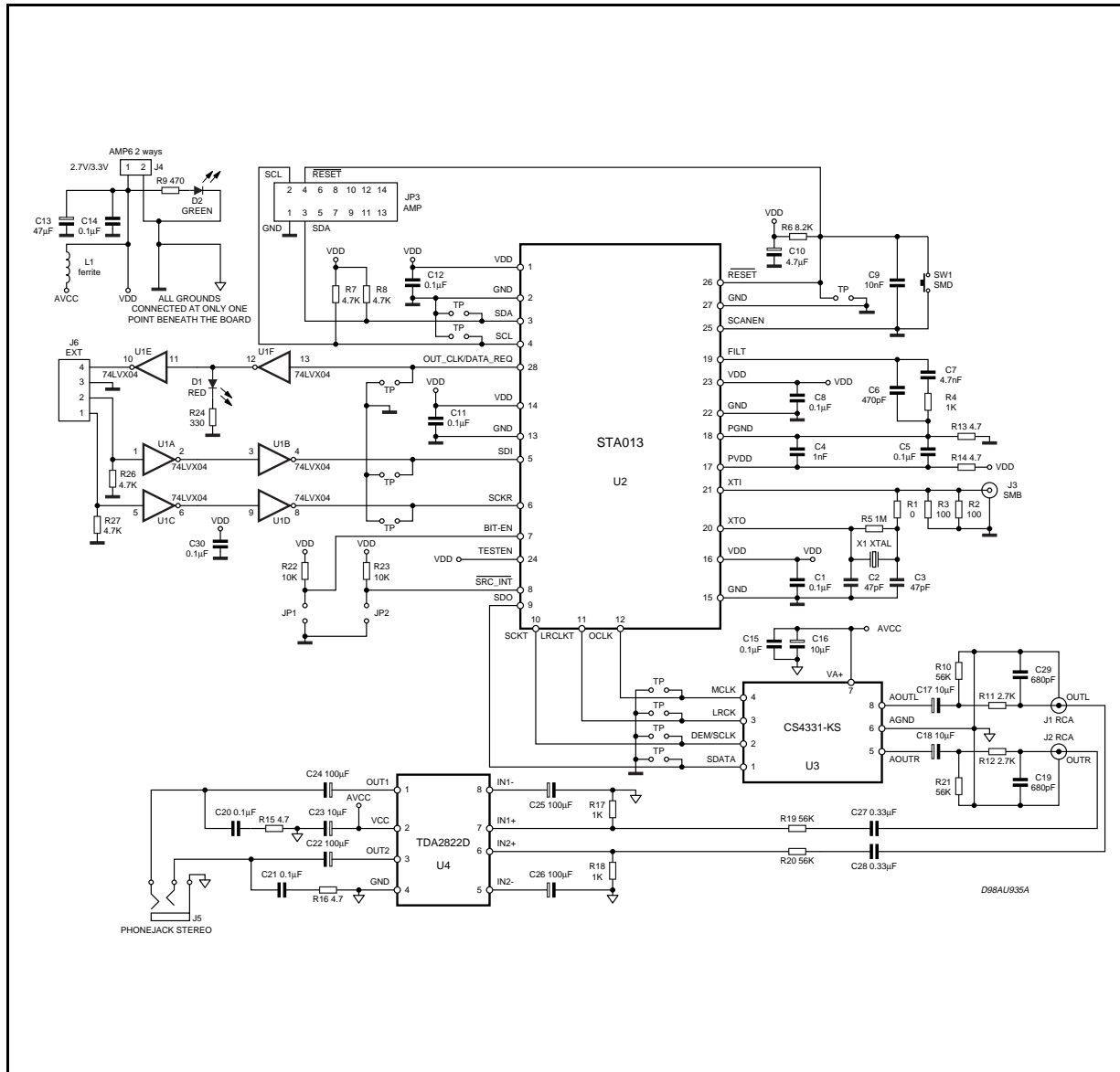
The pin no. 4 of STA013EVB I2C Connector is connected to the pin 26 of STA013, System Reset, to reset the device even by using a STA013SDR button.

The output of STA013 is a digital audio signal in standard format (as described in the data sheet at page no. 6/30). The pins no. 9, 10, 11, 12 STA013 are connected to the correspondent DAC pins no. 1, 2, 3, and 4. The DAC used on the STA013EVB is a Sigma-Delta 18 bit architecture (CS4331-KS).

The analog output of the converter is sent to the active **Speakers Connectors J1 (RCA-OUTL) and J2 (RCA-OUTR)**. The amplified analog outputs are even sent to the J5 **Headphone Connector**. The amplification is produced by means of an audio amplifier (TDA 2822).

On STA013EVB all the MPEG Decoder input and output digital signals can be monitored by the following test points:

Figure 4. STA013EVB Electrical Schematic



TEST POINT NAME(TP)	DESCRIPTION	REFERENCE PIN of U2
RESET	I2C Data	Pin 26
SDA	I2C Data	Pin 3
SCL	I2C Clock	Pin 4
DATA_REQ	Data Request Line Input	Pin 28
SDI	Serial Data Input	Pin 5
SCKR	Serial Clock Input	Pin 6
SDO1	Serial Data Output	Pin 9
SCKT	Serial Clock Output	Pin 10
LRCLK	Left/Right Clock Output	Pin 11
OCLK	DAC Oversampling Clock Output	Pin 12

(see figure 4 for details)

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### STA013 MASTER CLOCK

The STA013 can use three different Master Clock frequencies, each one obtained by an external crystal oscillator X1. The user can even evaluate these three different input frequencies by connecting a function generator to J3-SMB connector.

On STA013EVB the mounted crystal is a standard SMD SXA Packaged commercial one.

### STA013EVB SIGNAL LEVELS

The STA013 and all the components on the board work at 3V of power supply. The STA013 EVB Input Connector is buffered by an interface IC stage (U1A - U1F are six inverters included an 74IVX04 IC) by allowing the user to use directly a data source with signals level up to 5V without further stages.

### POWER SUPPLY

STA013EVB has to be supplied by the J4 connector. This board uses a particular layout technique to minimizing digital and analog noise, including grounding and power supply decoupling.. The allowed supply voltage range is 2.7V - 3.3V.

Figure 5. STA013EVB Component Side Silkscreen (not in scale)

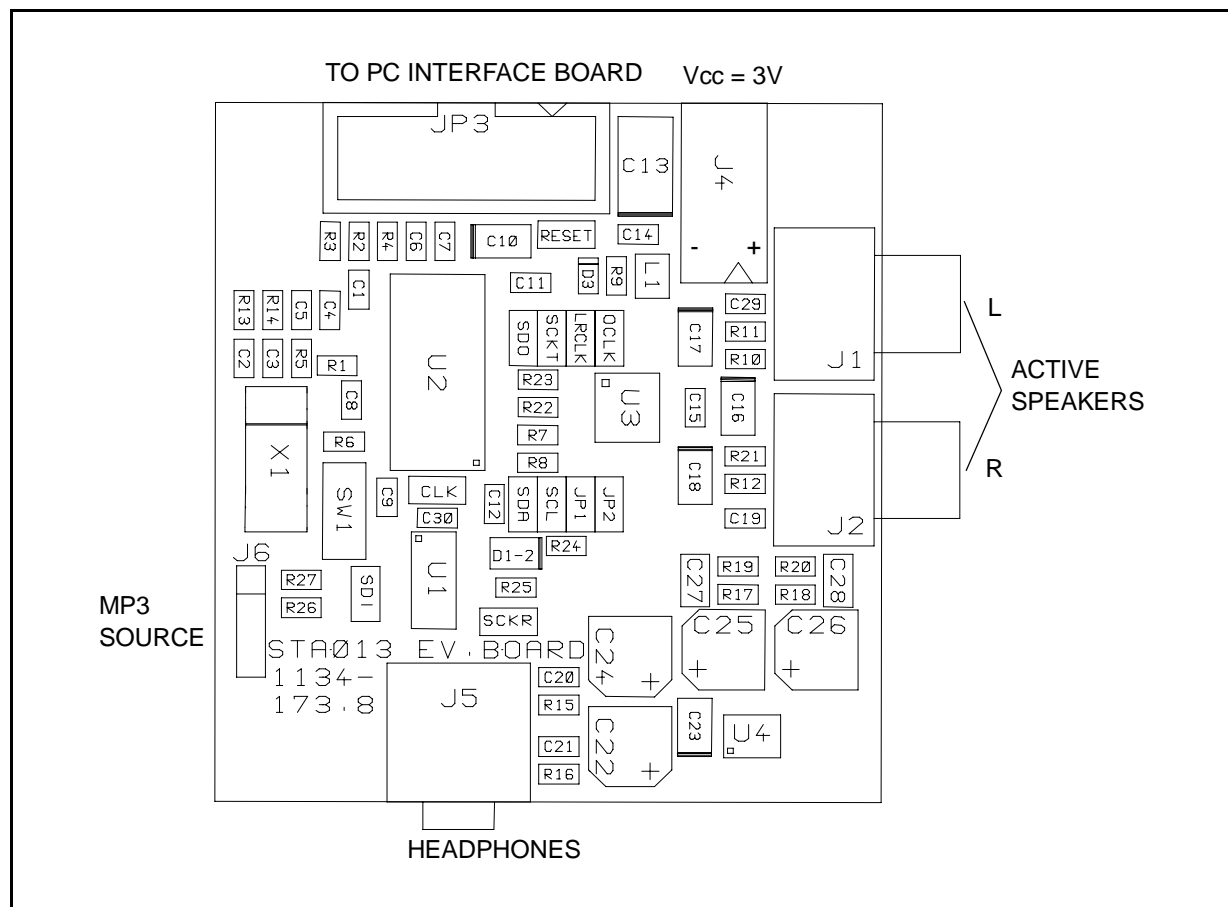
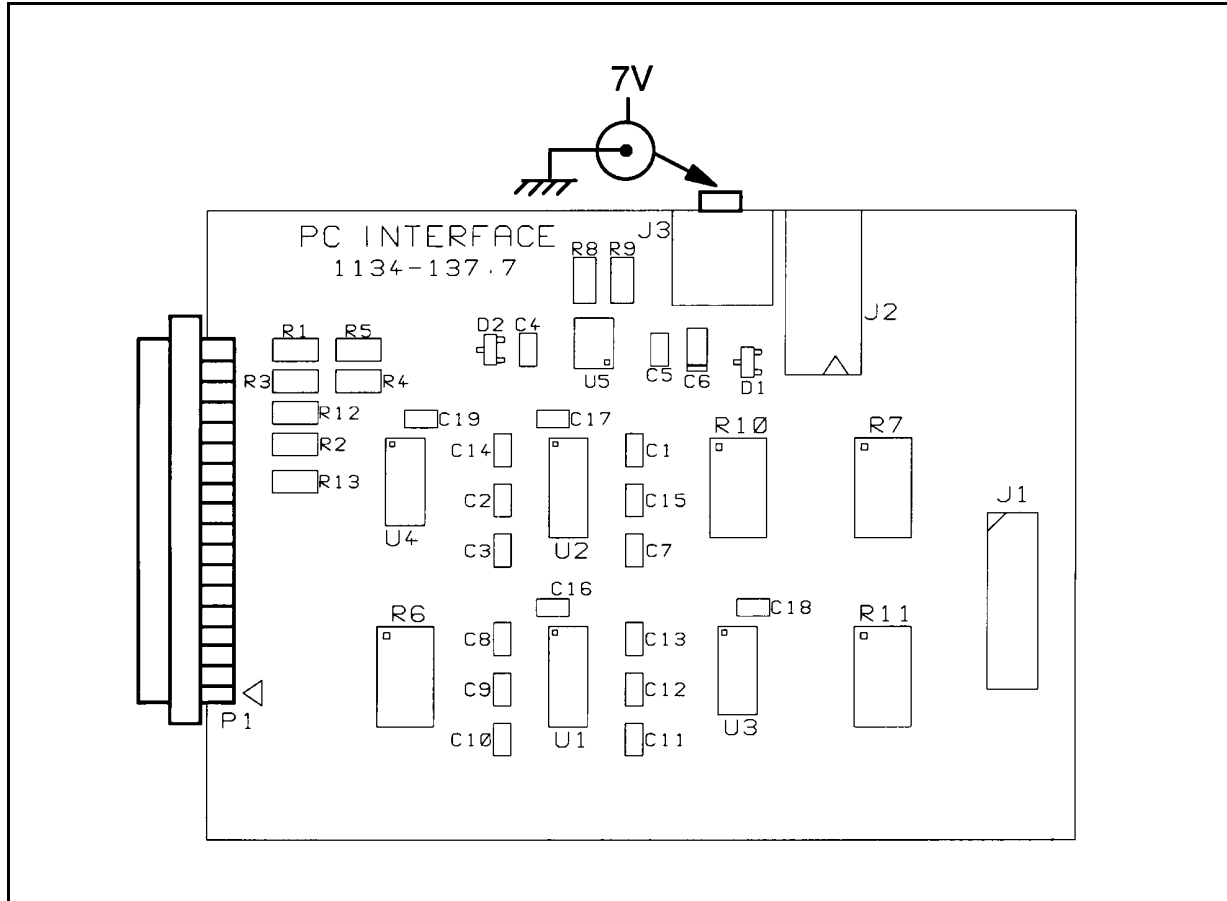
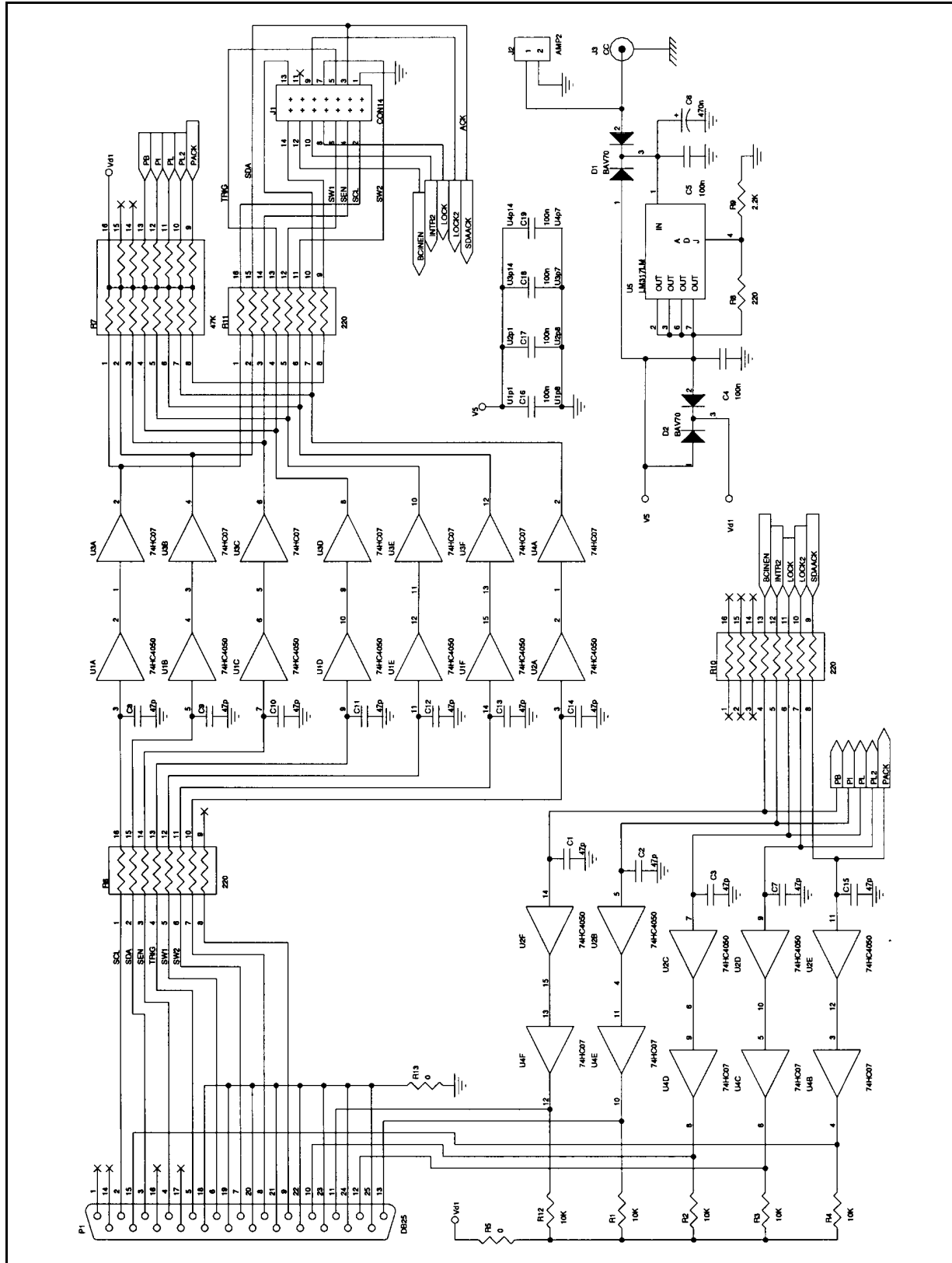


Figure 6. 1134-137.7 PC INTERFACE BOARD (not in scale)



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## Figure 7. PC Interface Schematic.

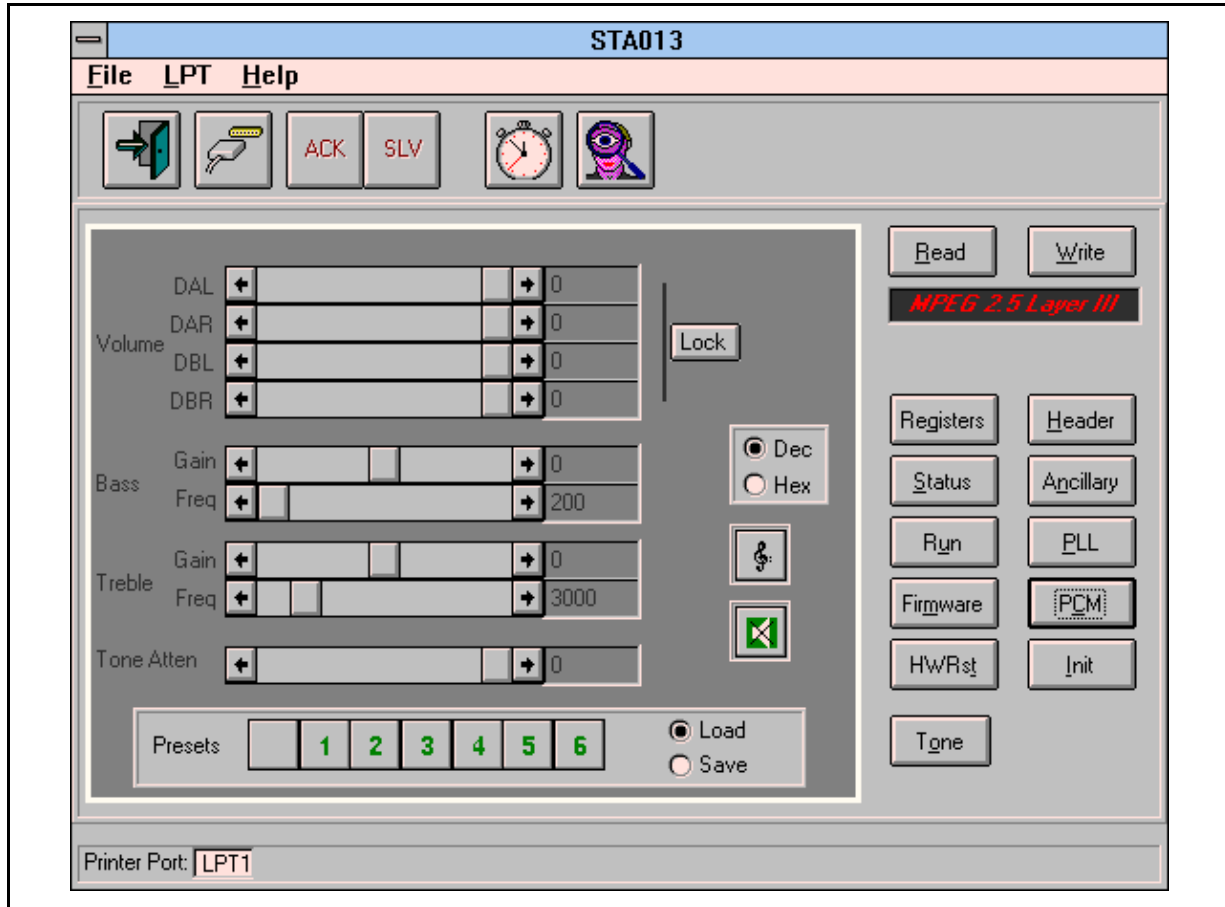




**STA013 PC CONTROL SOFTWARE**

The STA013EVB is provided with a PC Control Software Driver (STA013SDR), allowing the user evaluating all the device functions and controlling the device operation. The STA013SDR is a Win3.x / Win 95 software that can be installed directly by the user on a standard PC. (see Installation Procedure Section)

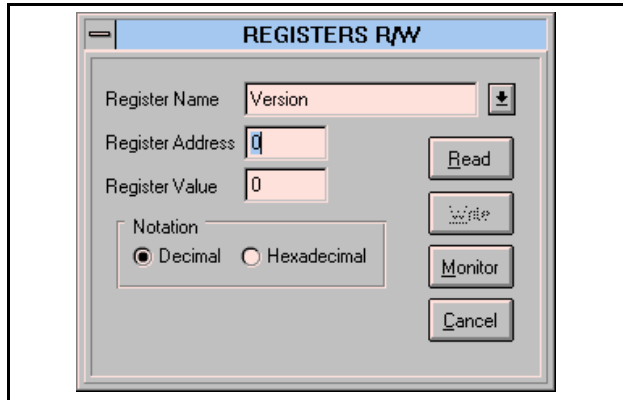
**STA013SDR Panel**



The graphical user interface of STA013SDR is composed by:

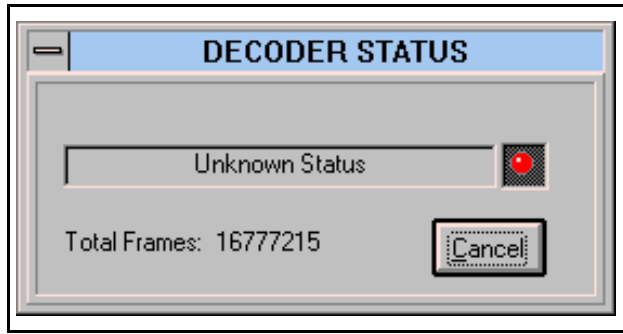
- Volume Control Bars** called DAL, DAR, DBL, and DBR. The function implemented is the same than the corresponding Volume Control I<sup>2</sup>C registers.
- Tone Control Bars** called Bass Gain, Bass Freq, Treble Gain, and Treble Freq. The functions implemented are equivalent to the corresponding Tone Control I<sup>2</sup>C Registers.
- Tone Atten Bar** it has equivalent function than the Tone\_Atten I<sup>2</sup>C register.
- Read Button** it is used to read the current I<sup>2</sup>C registers status, corresponding to the Panel Functions. By pressing this button the Panel will show the status of all the displayed registers.
- Write Button** it is used to write the current I<sup>2</sup>C registers status, corresponding to the Panel Functions. By pressing this button the software will update the status of all the displayed registers.

**Registers Button**



this function allow the read and/or the write operation on all the STA013 registers. To write the registers the user has to update the register setting before pressing the write button.

**Status Button**



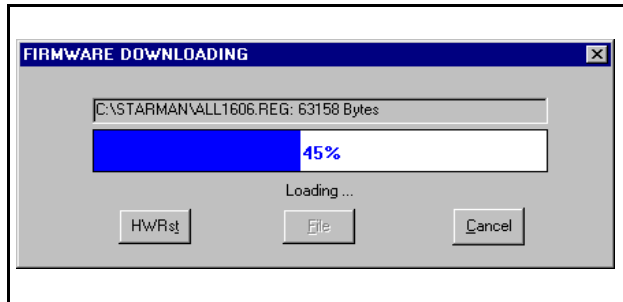
by pressing this button the user open a window displaying the status of STA013. The possible status are described in the STATUS register description.

In the lower part of the Status window the MPEG Frame Counter value is displayed.

**Run Button**

the function implemented by this button is equivalent to the RUN I<sup>2</sup>C register.

**Firmware Button**



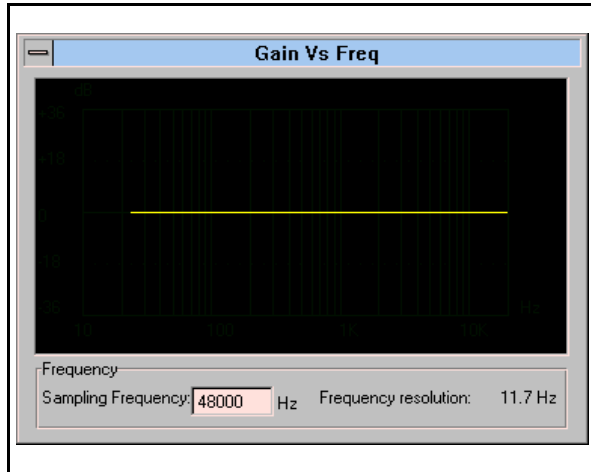
by pressing this button the user opens a window to download the STA013 Patch File (if needed).

This action is suggested to be preceded by an HW Reset (by the software or by the button on the STA013EVB).

**HW Reset**

This button implemet a System Reset. The output of the PC is, in this case, connected to the STA013 pin no. 26. The reset performed by the software and by the hardware button on the STA013 are equivalent.

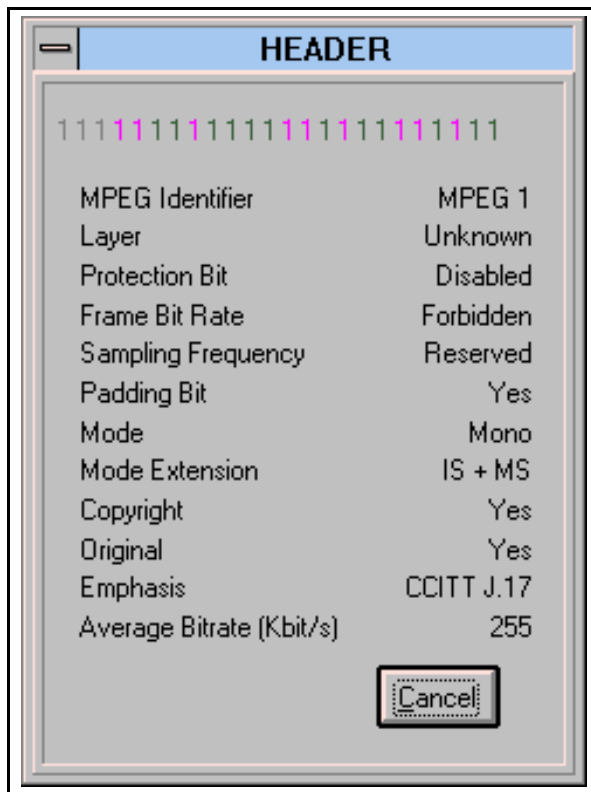
**Tone Button**



by selecting this function, the user opens a window describing the ideal frequency response of the Tone Control function.

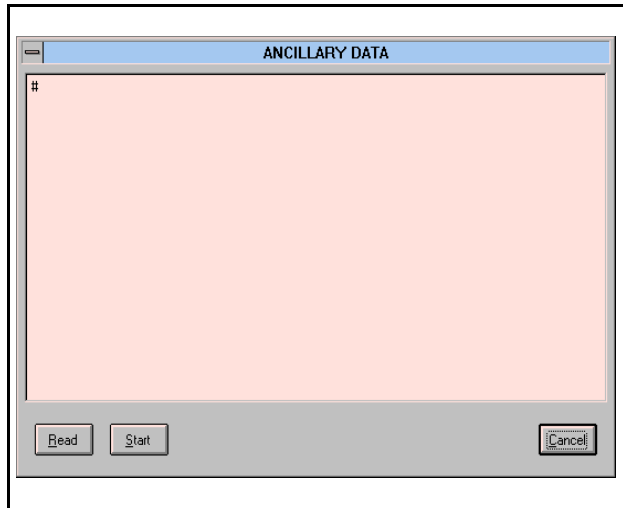
The window is updated when the Tone Control parameters are modified by the users.

**Header Button**



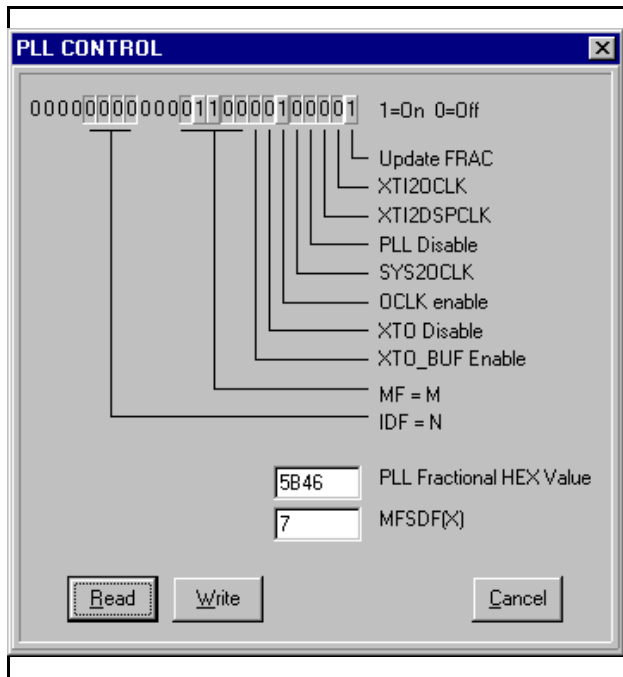
by pressing this button the STA013SDR displays all the relevant information contained in the MPEG Frame Headers of the incoming compressed bit-stream.

Ancillary Button



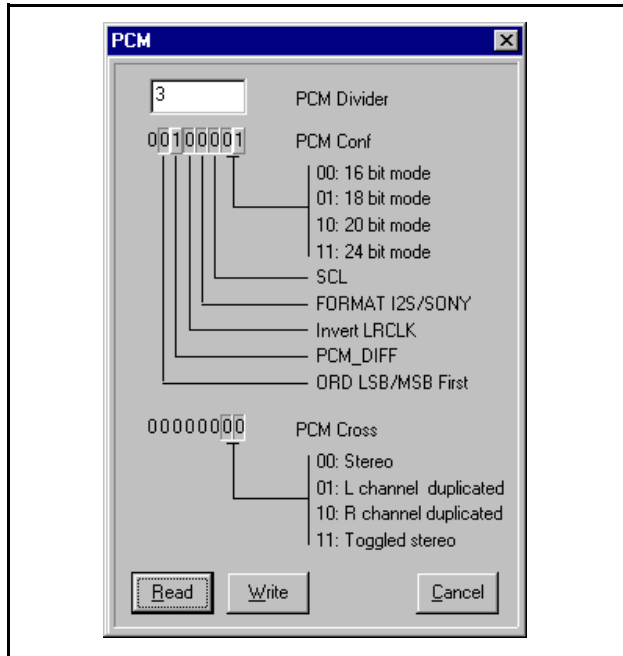
this function allow the user to read the Ancillary Data coded in the MPEG stream. The Ancillary Data are displayed as ASCII characters.

PLL Button



by pressing this button, all the PLL configuration register become visible and can be read or written.

**PCM Button**



this button, if selected, opens a window to read or change the PCM audio interface configuration.

**Init Button**

by pressing this button the user download the initialisation file to bootstrap the STA013 on the application board. The initialisation file must be called sta013.ini and must be placed in the directory where the STA013SDR is installed

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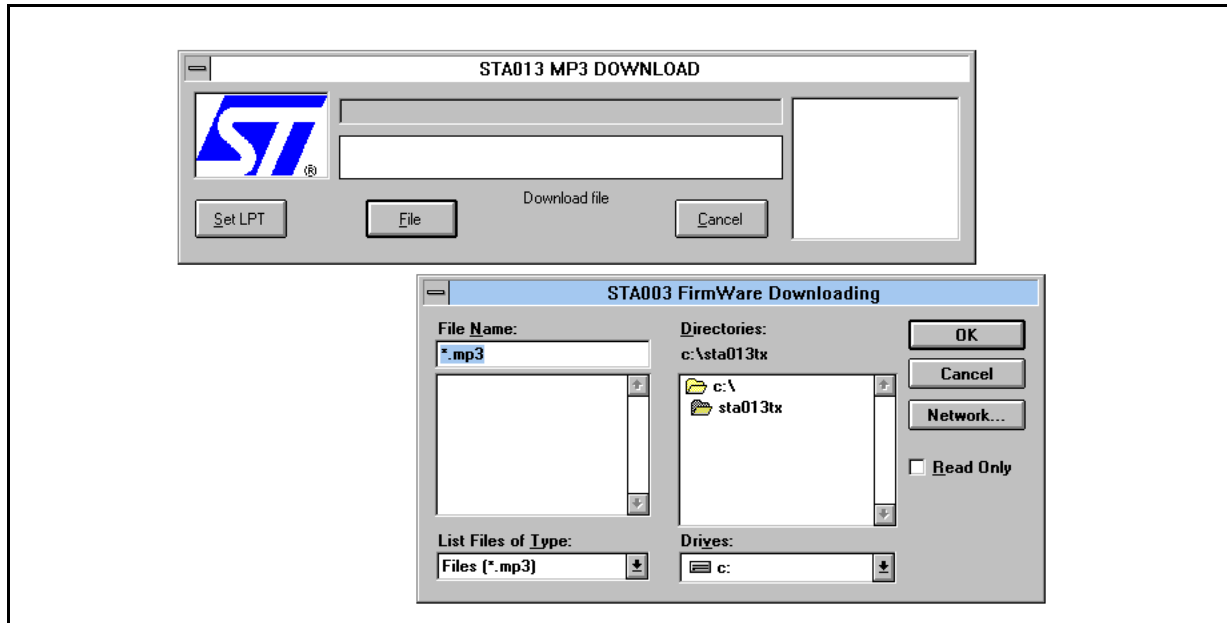
### STA013 PC TRANSMISSION SOFTWARE DRIVER DESCRIPTION

The STA013EVb is provided with the PC Software Transmission Driver (STA013TXD), allowing the user to send the MPEG bitstream to the device.

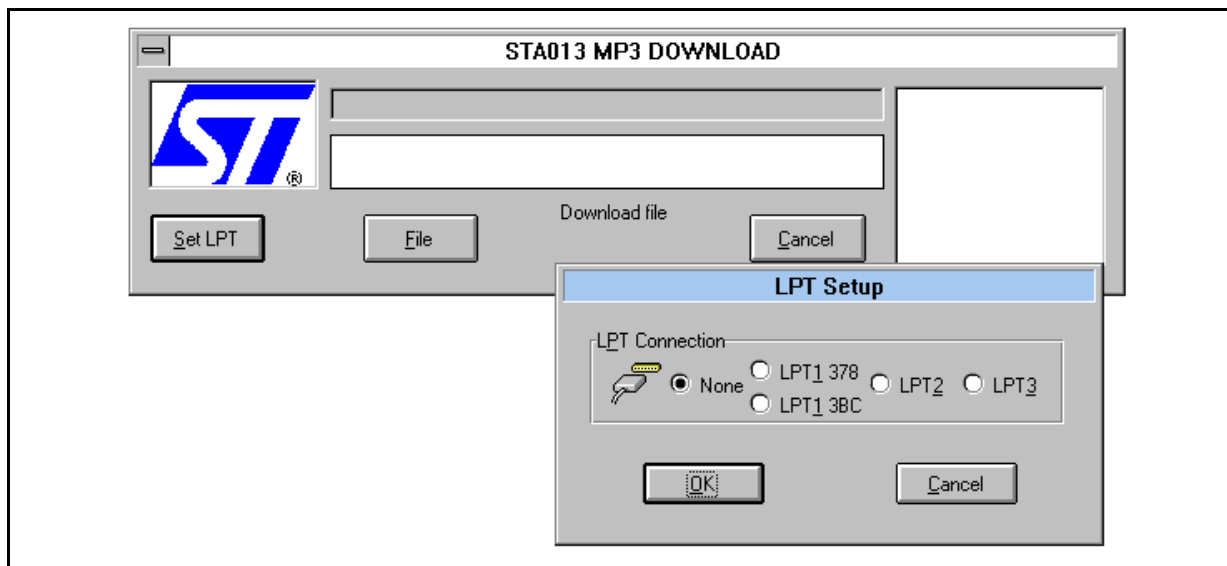
The STA013TXD is a Win 3xx/Win95 software and can be installed by the user on a standard PC (see Installation Procedure Section)

### STA013TXD Panel

The STA013TXD user interface is composed by a graphical panel. The File button is used to select the .MP3 file to be transmitted to STA013EVb.



### Set LPT Button



this panel is used to configure the PC Parallel Port address.

NOTE:

Before start working with STA013TXD it is suggested to configure the PC Parallel Port to EPP 1.9 Mode by BIOS setup. This is possible only for new versions of Pentium PCs.

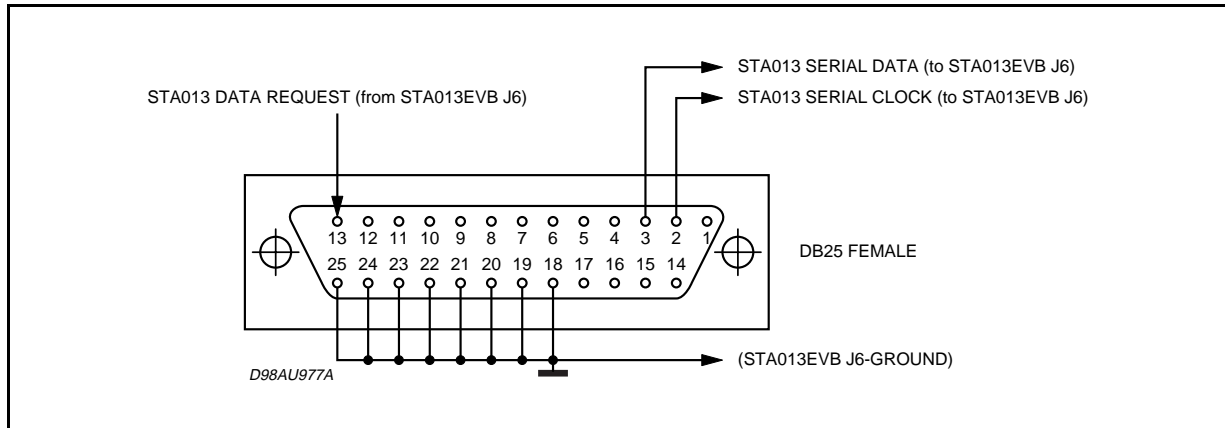
This configuration enables a DMA channel from the PC HDD to the Parallel Port hardware, improving the performances.

Even with this configuration the user may note audio dropouts, due to the Parallel Port performance.

To minimise the effect, it is suggested to copy the mp3 files on the P.C. HDD and run a de fragmentation tool.

The STA013TXD can handle data rates up to 128Kbit/sec.

**PC Parallel Port Pinout for STA013TXD**



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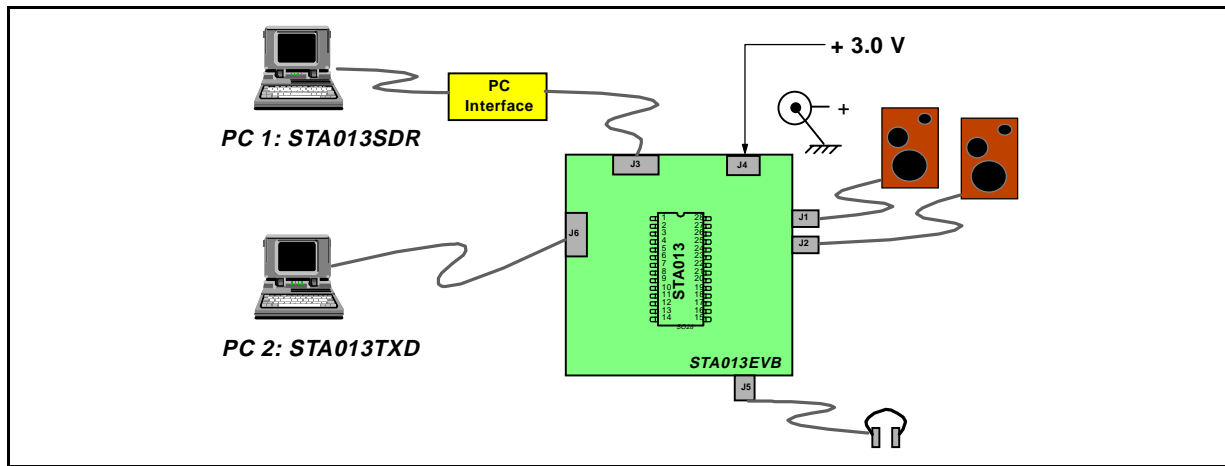
### GENERAL INFORMATION ON STA013 EVALUATION ENVIRONMENT

The STA013 Evaluation toolkit is composed by a set of components, as follows:

<b>STA013EVB</b>	<b>STA013 Evaluation Board</b> (already described in the previous section).
<b>STA013TXD</b>	<b>STA013 Software Transmission Driver</b> (already described in the previous section).
<b>STA013SDR</b>	<b>STA013 Software Driver</b> (already described in the previous section).
<b>PC Interface Board</b>	useful to avoid electrical shocks due to the operating voltage difference between the PC Parallel Port and the STA013EVB.

All the kit components are provided with flat cables to connect the different units.

### Evaluation Environment



### DEMOBOARD SET-UP SEQUENCE

Note: Supply voltage of the I2C board is 7 V  
Supply voltage of STA013EVB is 3.3 V

1. Run "setup.exe" program from STA013SDR software
2. Click on "HWRst" button
3. Click on "Registers" button
4. Select "Ident" register
5. Click on "Read" button and verify that the read value is "172"
6. From the control panel, click on "Firmware" button
7. Click on "HWRst" button
8. Click on "File" button to load the configuration file .reg into the PATCH Ram;
9. Wait until the whole file is downloaded
10. Click on "Cancel" button to exit from the menu
11. Click on "Run" button: now the red led on the board should be switched off
12. Run "STA013TXD" software and, clicking on "File" button, select the mp3 file to be tested.  
The red led must be now switched on and the music start to play.



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