NEC

NEC Electronics Inc.

μPD7516H
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH FIP® CONTROLLER/DRIVER

Description

The μPD7516H and 75CG16H are 4-bit, single-chip CMOS microcomputers with the μPD7500 series architecture and a FIP controller/driver. On-board peripheral functions include an 8-bit timer/event counter, an 8-bit serial interface, a 14-bit programmable pulse generator, and a display controller/driver that supervises all of the timing requirements by the 24-port S segment drivers either for a 16-character, 7-segment FIP, or an 8-character, 14-segment FIP. The μPD7516H is functionally equivalent to the μPD7519H except for ROM size.

Twenty-eight I/O lines are organized into seven 4-bit ports: the input/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, and 6.

The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values.

The μPD7516H/75CG16H has a 2.44 μs instruction cycle time at $f_{XX} = 6.55$ MHz.

For the μPD7516H, current consumption is less than 6 mA for normal operation ($V_{DD} = 5\,V \pm 10\%$, $f_{XX} = 6.55$ MHz, high speed mode).

The μPD75CG16H, a piggyback EPROM version, is available for prototyping and program development. It is pin-compatible and functionally equivalent to the masked version.

Features

- ☐ 6144 × 8-bit program memory (ROM)
- ☐ 256 × 4-bit data memory (RAM)
- ☐ 28 I/O lines
- ☐ Programmable FIP controller/driver
  - — 24 high-voltage output lines
- ☐ 8-bit serial interface
- ☐ 8-bit timer/event counter
- ☐ Programmable pulse generator (PPG)
  - — Variable duty port (D/A converter)
  - — Signal generator port
  - — 1-bit output port
- ☐ Vectored, prioritized interrupts
  - — Two external: INT0, INT1
  - — Two internal: timer (INTT) and serial (INTS)
- ☐ Four 4-bit general purpose registers
- ☐ 107 instructions; subset of μPD7500 series instruction set A
  - — Look-up-table capability
  - — Indirect indexed addressing
- ☐ Instruction cycle
  - — μPD7516H low speed mode: 15.26 μs/4.19 MHz
  - — μPD7516H low speed mode: 9.77 μs/6.55 MHz
  - — μPD7516H high speed mode: 3.81 μs/4.19 MHz
  - — μPD7516H high speed mode: 2.44 μs/6.55 MHz
- ☐ Two power-down modes
- ☐ Single power supply (2.5 V to 6 V)

* FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Applications

The μPD7516H has a variety of flexible powerful functions and is best suited for the following applications:

- Video tape recorders
- Plain paper copiers
- Electronic cash registers
- Telephone sets
- Electronic scales
- Automobiles

Figures 1-4 show how to apply the device to a digital tuning system, a telephone, an ECR, and automotive equipment.

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7516HG-12	64-pin plastic miniflat	6.55 MHz
μPD7516HG-36	64-pin plastic QUIP	6.55 MHz
μPD7516HCW	64-pin plastic shrink DIP	6.55 MHz
μPD75CG16HE	64-pin ceramic piggyback QUIP	6.55 MHz

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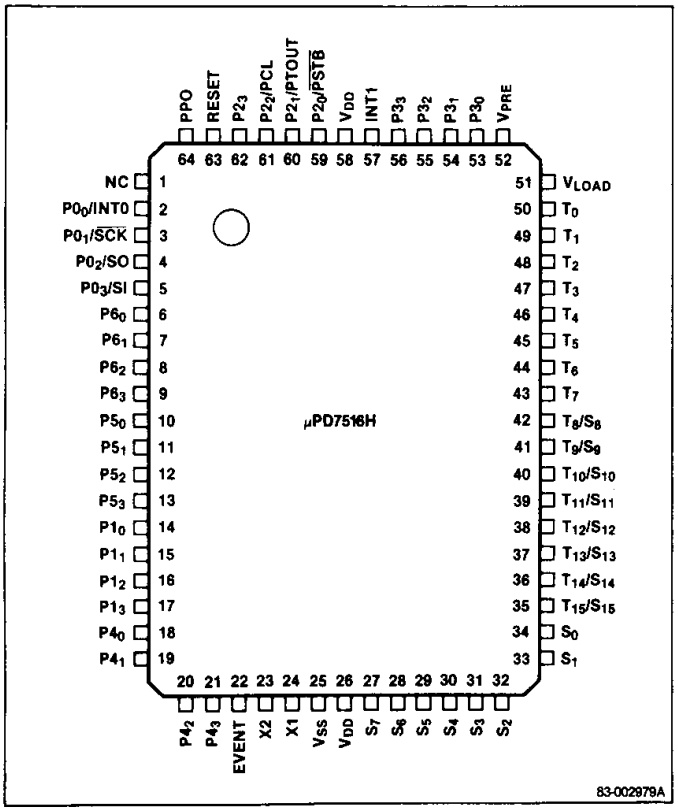
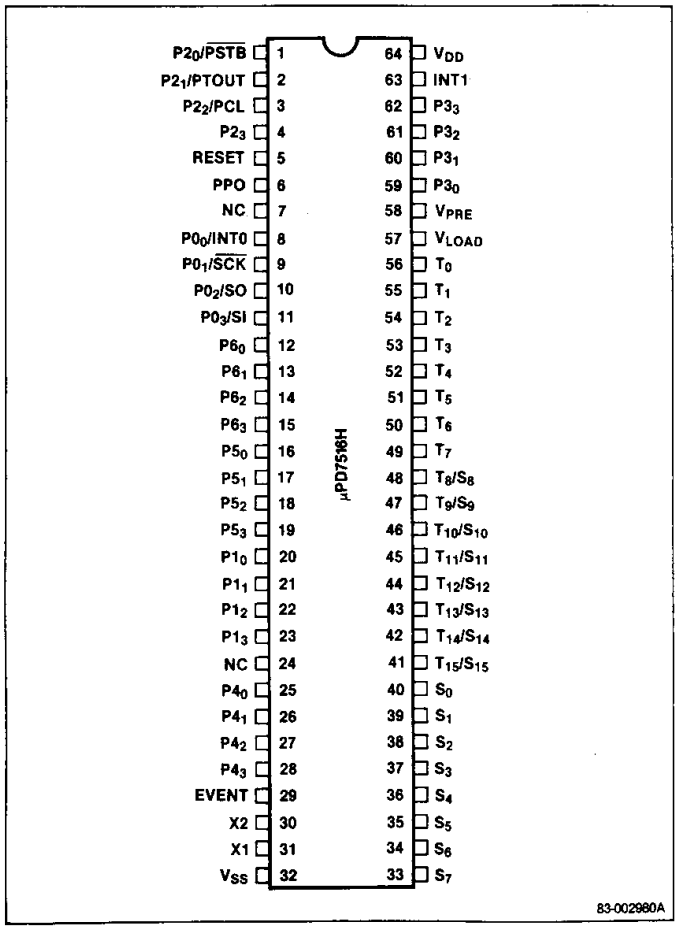
Pin Configurations

64-Pin Plastic Miniflat



64-Pin Plastic QUIP, and Shrink DIP



Pin Identification

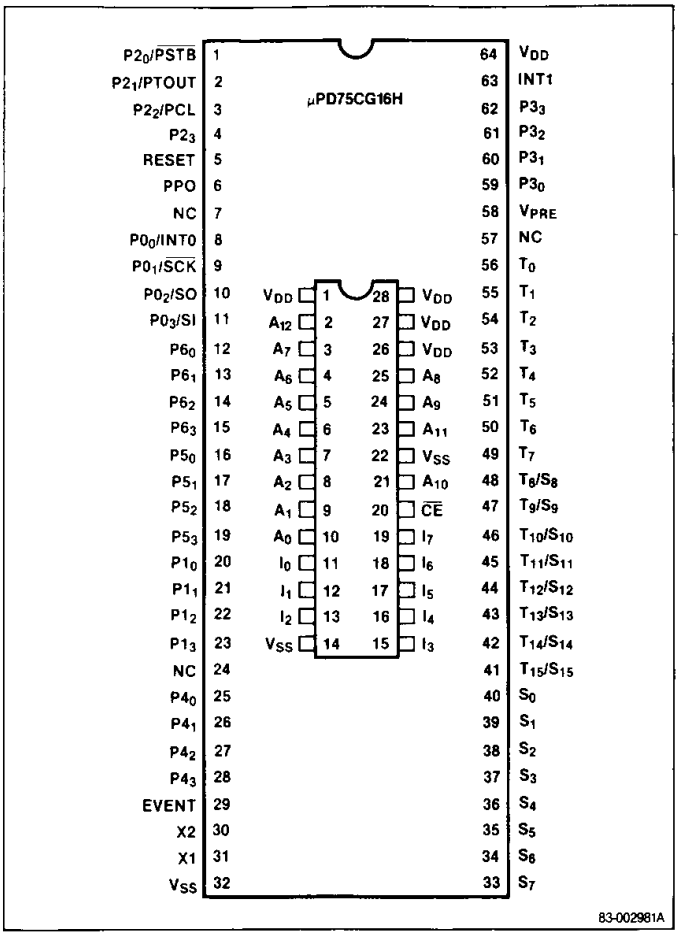
Plastic Miniflat, QUIP, and Shrink DIP

Flat	QUIP(1)	Symbol	Function
1	7, 24	NC	No connection
2	8	$P0_0$ / INT0	Port 0, or external interrupt INT0 and the serial I / O interface
3	9	$P0_1$ / $\overline{SCK}$	
4	10	$P0_2$ / SO	
5	11	$P0_3$ / SI	
6–9	12–15	$P6_0$–$P6_3$	Port 6
10–13	16–19	$P5_0$–$P5_3$	Port 5
14–17	20–23	$P1_0$–$P1_3$	Port 1
18–21	25–28	$P4_0$–$P4_3$	Port 4
22	29	EVENT	Timer / event counter input
23, 24	30, 31	X2, X1	Crystal clock input
25	32	V_{SS}	Ground
26, 58	64	V_{DD}	Power supply positive
27–34	33–40	S_0–S_7	Segment outputs
35–42	41–48	T_8 / S_8–T_{15} / S_{15}	Timing / segment outputs
43–50	49–56	T_0–T_7	Timing outputs
51	57	V_{LOAD}	High voltage option resistor supply negative. This pin is not used (NC) in the μPD75CG16H.
52	58	V_{PRE}	High voltage predriver supply negative
53–56	59–62	$P3_0$–$P3_3$	Port 3
57	63	INT1	External interrupt
59	1	$P2_0$ / $\overline{PSTB}$	Port 2, or port 1 STB signal, timer F / F output, internal CL output, and general purpose output
60	2	$P2_1$ / PTOUT	
61	3	$P2_2$ / PCL	
62	4	$P2_3$	
63	5	RESET	RESET input
64	6	PPO	PPG output

Note:
(1) This QUIP pin identification is also true for the shrink DIP and piggy-back packages.

Pin Configurations (cont)

64-Pin Ceramic Piggyback QUIP



Pin Identification (cont)

μPD75CG16H, Piggyback EPROM

No.	Symbol	Function
1	V_{DD}	Unused
2–10, 21, 23–25	A_0–A_{12}	Program counter output
11–13, 15–19	I_0–I_7	Data input from the 2764
14	V_{SS}	Same as bottom pin 32; connected to 2764 GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Same as bottom pin 32; supplies OE signal to the 2764
26	V_{DD}	Same as bottom pin 64; supplies V_{CC} to the 2764
27, 28	V_{DD}	Unused

Pin Functions

(Except EPROM)

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI (Port 0)

This port can be configured as the 4-bit, parallel input port 0, or as the 8-bit serial I/O interface under control of the serial mode select register. The 8-bit serial I/O interface consists of the serial input (SI), the serial output (SO), and a serial clock ($\overline{SCK}$) used for synchronizing data transfer. Line $P0_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P1_0$–$P1_3$ (Port 1)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 1 mode select register.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$/PCL, $P2_3$

$P2_0$–$P2_3$ are the 4-bit latched output port 2. $\overline{PSTB}$ is the port 1 output strobe pulse. PTOUT is the timer-out F/F signal. PCL is the internal system clock output. $P2_3$ is a general purpose output.

$P3_0$–$P3_3$ (Port 3)

4-bit, latched three-state output port 3.

$P4_0$–$P4_3$ (Port 4)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 5.

$P5_0$–$P5_3$ (Port 5)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 4.

$P6_0$–$P6_3$ (Port 6)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 6 mode select register.

EVENT

1-bit external event input for the timer/event counter.

S_0–S_7, T_8/S_8–T_{15}/S_{15}, T_0–T_7

High voltage outputs. S_0–S_7 are segment driver outputs, and T_0–T_7 are digit driver outputs. T_8/S_8–T_{15}/S_{15} can be configured as either segment or digit driver outputs under control of the display mode select register.

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INT1

External, rising edge triggered interrupt.

PPO

1-bit programmable pulse generator output. PPO can operate as the pulse width modulation output, signal generator port, or 1-bit output port, as dictated by the PPG mode select register.

RESET

RESET input. R/C circuit or pulse initializes μPD7516H and also releases stop or halt mode.

X1, X2

Crystal clock connection. A crystal oscillator circuit is connected to X1 and X2 for system clock operation, or an external clock may be connected to X1 and an inverted clock to X2.

V_{PRE}

High voltage predriver supply. Apply single voltage from V_{DD} – 12 V to V_{DD} for proper display operation.

V_{LOAD}

High voltage option resistor supply negative. Apply single voltage from V_{DD} – 40 V to V_{DD} for proper display operation. This pin is not used (NC) in the μPD75CG16H.

V_{DD}

Power supply positive. Apply single voltage ranging from 2.5 V to 6.0 V for proper operation.

V_{SS}

Ground.

EPROM Pin Functions

Piggyback EPROM

A_0-A_{12} (Address)

Output the 13 bits of the program counter (PC_0-PC_{11}), which are the address signals of EPROM 2764.

I_0-I_7 (Data Input)

Input data from the 2764.

$\overline{CE}$ (Chip Enable)

Outputs the chip enable signal to the 2764.

V_{DD} (Pin 1)

Electrically equivalent to V_{DD} of the bottom pins. Provided for future devices. Use in the open condition.

V_{DD} (Pin 26)

Electrically equivalent to V_{DD} of the bottom pins. Supplies V_{CC} to 2764.

V_{DD} (Pins 27, 28)

Electrically equivalent to V_{DD} of the bottom pins. Do not use these pins.

V_{SS} (Pin 22)

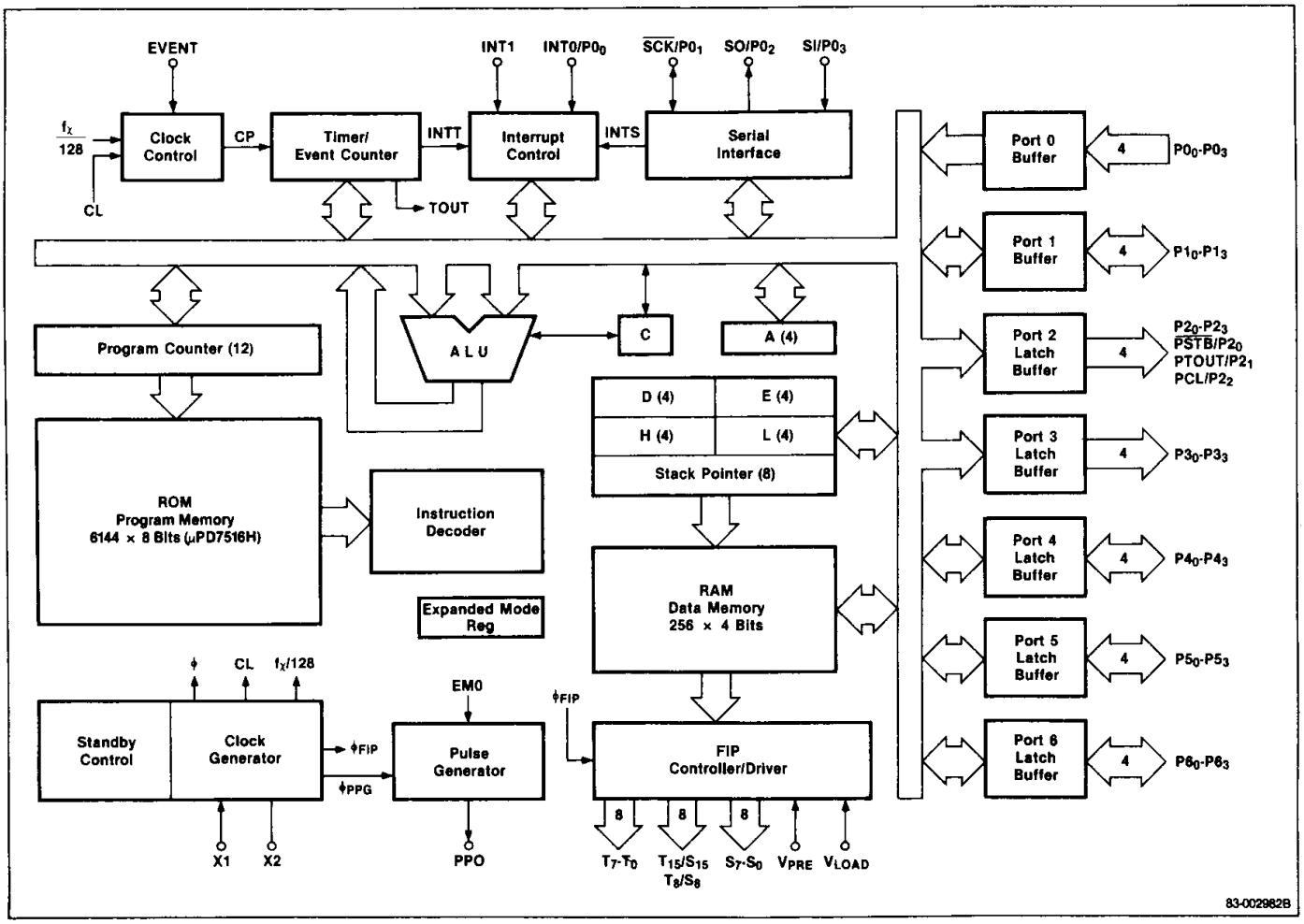
Electrically equivalent to VSS of the bottom pins. Supplies $\overline{OE}$ signal to the 2764.

V_{SS} (Pin 14)

Electrically equivalent to V_{SS} of the bottom pins. Connected to 2764 GND pin.

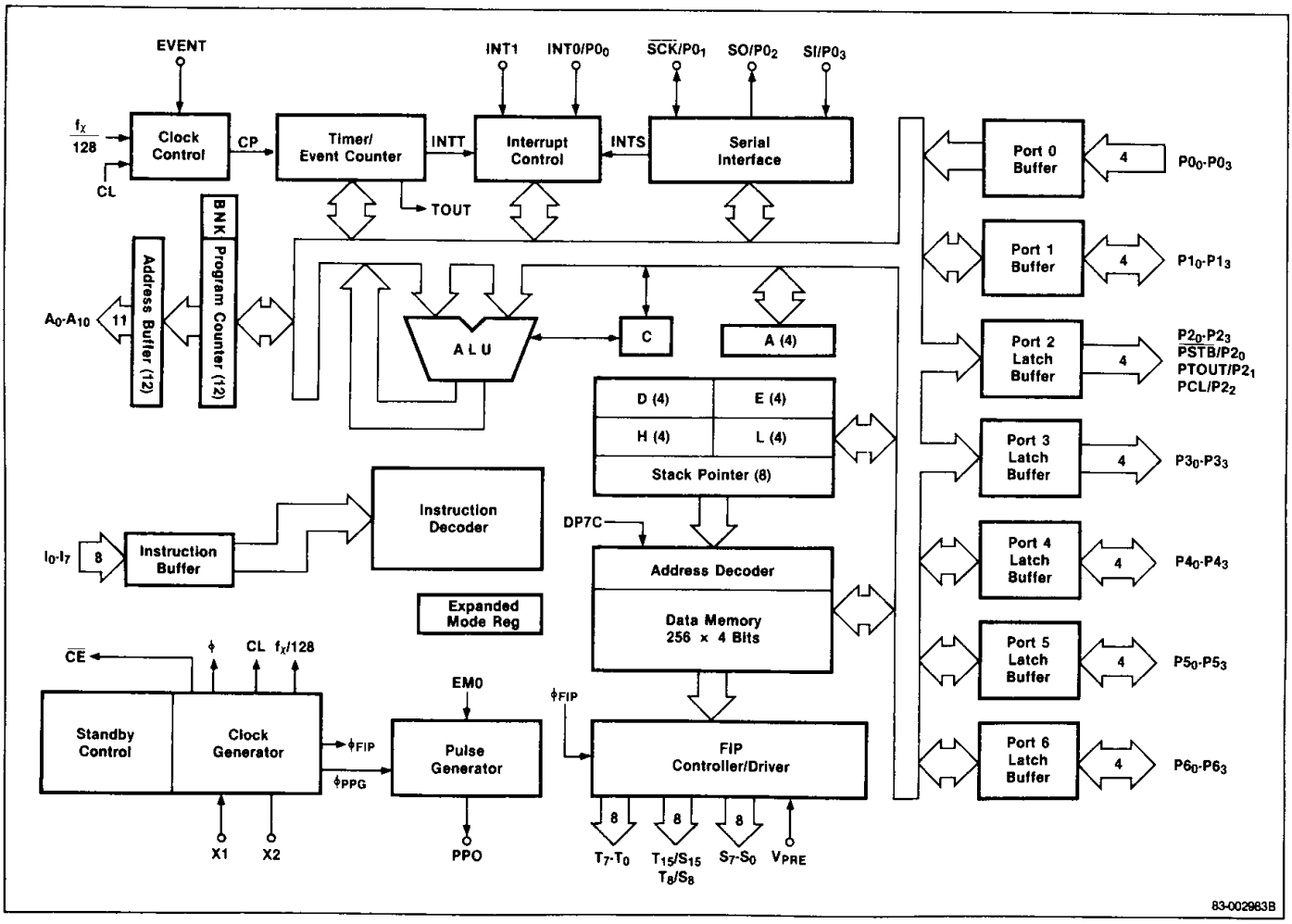
Block Diagrams

μPD7516H



Block Diagrams (cont)

μPD75CG16H



Absolute Maximum Ratings

$T_A = 25°C$

Supply voltages	
V_{DD}	−0.3 V to +7 V
V_{LOAD} (μPD7516H)	V_{DD} −40 V to +V_{DD} +0.3 V
V_{PRE}	V_{DD} −12 V to +V_{DD} +0.3 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	
Display outputs, V_O	V_{DD} −40 V to V_{DD} +0.3 V
Other outputs, V_{OD}	−0.3 V to V_{DD} +0.3 V
Output current high, I_{OH}	
Per pin, other than display outputs	−15 mA
Per pin, S_0–S_7	−15 mA
Per pin, T_0–T_7, T_8 / S_8–T_{15} / S_{15}	−30 mA
Total, display outputs, μPD7516H	−120 mA
display outputs, μPD75CG16H	−90 mA
Total, other than display outputs	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, all output ports	60 mA
Total power consumption (Note 1), PT	
Plastic flat package (μPD7516H)	400 mW
Plastic QUIP, (μPD7516H)	600 mW
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

(1) Calculation of PT: there are three kinds of power consumption, the total of which should be less than the total power consumption (PT) in this specification. Use of less than 80% of PT is recommended. The three different power consumptions are as follows:
1. CPU power consumption. V_{DD}(max) × I_{DD1}(max)
2. Power consumption of output pins. This includes both normal output and display output. Calculate the total consumption of each output pin to which the maximum current flows.
3. Power consumption of on-chip pull-down resistors (mask option).

Example

Configuration:
9 segments × 11 digits, 4 LED outputs
V_{DD} = 5 V ±10%, 4.19 MHz oscillation
Segment pin = 5 mA (max)
Timing pin = 15 mA (max)
LED output pin = 10 mA (max)
Vacuum fluorescent display (V_{LOAD}) = −30 V

Consumption:

(1) CPU
5.5 V × 2.0 mA = 11 mW

(2) Output pins
Segment pins: (5/7 × 2 V) × 5 mA × 9 = 64 mW
Timing pins: 2 V × 15 mA = 30 mW
LED output pins: (10/15 × 2 V) × 10 mA × 4 = 53 mW

(3) Pull-down resistors
$(30 + 5.5\,V)^2/80\,k\Omega \times 10 = 158$ mW

Therefore, PT = (1) + (2) + (3) = 316 mW

DC Characteristics

μPD7516H: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 6 V
μPD75CG16H: T_A = −10°C to +70°C, V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than X1, X2
	V_{IH2}	V_{DD} −0.4		V_{DD}	V	X1, X2 (Note 1)
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Other than X1, X2
	V_{IL2}	0		0.4	V	X1, X2 (Note 1)
Output voltage high	V_{OH}	V_{DD} −1.0			V	V_{DD} = 5 V ±10%, I_{OH} = −1 mA
		V_{DD} −0.5			V	μPD7516H only, I_{OH} = −100 μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 5 V ±10%, I_{OL} = 1.6 mA
				0.5	V	μPD7516H only, I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	$V_I = V_{DD}$; other than X1, X2
	I_{LIH2}			20	μA	$V_I = V_{DD}$; X1, X2
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V; other than X1, X2
	I_{LIL2}			−20	μA	V_I = 0 V; X1, X2
Input leakage current	I_{IL}			−200	μA	μPD75CG16H only; V_I = 0 V, I_0–I_7
Output leakage current high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current low	I_{LOL1}			−3	μA	V_O = 0 V; other than display outputs
	I_{LOL2}			−10	μA	$V_O = V_{LOAD} = V_{DD}$ −35 V; display outputs

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DC Characteristics (cont)

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5\,V$ to $6\,V$
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Display output current	I_{OD}	−7			mA	S_0–S_7; (Notes 2 & 3)
		−4			mA	μPD75CG16H; (Notes 2 & 3)
		−15			mA	T_0–T_{15} (Notes 2 & 3)
		−10			mA	μPD75CG16H; (Notes 2 & 3)
		−3			mA	S_0–S_7; (Note 4)
		−2			mA	μPD75CG16H; (Note 4)
		−7			mA	T_0–T_{15} (Note 4)
		−5			mA	μPD75CG16H; (Note 4)
On-chip pull-down resistance	R_L	40	70	120	kΩ	$V_{OD} - V_{LOAD} = 35\,V$
Supply current, μPD7516H	I_{DD1}		3.0	9.0	mA	High speed $V_{DD} = 5\,V \pm 10\%$; (Note 5)
	I_{DD2}		0.6	1.9	mA	Low speed halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 5)
	I_{DD1}		2.0	6.0	mA	High speed $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			400	1200	μA	$V_{DD} = 3\,V \pm 10\%$; (Note 6)
	I_{DD2}		450	1500	μA	Halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			150	400	μA	Halt mode $V_{DD} = 3\,V \pm 10\%$; (Note 6)
	I_{DD3}		0.1	20	μA	Stop mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			0.1	10	μA	Stop mode $V_{DD} = 3\,V \pm 10\%$; (Note 6)
Supply current, μPD75CG16H	I_{DD1}		1.2	3.6	mA	High speed $V_{DD} = 4.75\,V$ to $5.5\,V$; (Note 5)
			1.0	3.0	mA	High speed; (Note 6)
	I_{DD2}		350	1000	μA	Halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
	I_{DD3}			20	μA	Stop mode; (Note 6)

Note:
(1) The circuits in figures 19 and 20 are recommended.
(2) The external circuit in figure 21 is recommended.
(3) $V_{PRE} = V_{DD} - 9\,V \pm 1\,V$, $V_{DD} = 4\,V$ to $6\,V$, $V_{OD} = V_{DD} - 2\,V$
(4) $V_{PRE} = 0\,V$, $V_{OD} = V_{DD} - 2\,V$
(5) 6.55 MHz crystal, C1 = C2 = 10 pF
(6) 4.19 MHz crystal, C1 = C2 = 10 pF

Capacitance

$T_A = 25°C$; $V_{DD} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	(Note 1)
Output capacitance, Display outputs	C_O			35	pF	(Note 1)
Other outputs				15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) $f_c = 1\,MHz$, Unmeasured pins are connected to 0 V.

AC Characteristics

Clock Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5$ V to 6 V

μPD75GC16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5 V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation	f_{XX}	3.5	4.19	4.2	MHz	(Notes 1, 2 & 3)
		4.2	6.55	6.6	MHz	$V_{DD} = 4.5$ V to 6.0 V; (Notes 1, 2 & 3)
System clock input frequency	f_X	0.1		4.2	MHz	(Notes 1 & 4)
		4.2		6.6	MHz	$V_{DD} = 4.5$ V to 6.0 V; (Notes 1 & 4)
X1, X2 input pulse width high, low	t_{XH}	100			ns	(Notes 1 & 4)
	t_{XL}	75				$V_{DD} = 4.5$ V to 6.0 V; (Notes 1 & 4)
EVENT input frequency	f_E			410	kHz	$V_{DD} = 4.0$ V to 6.0 V
				80	kHz	μPD7516H only
EVENT input pulse width high, low	t_{EL}	1.2			μs	$V_{DD} = 4.0$ V to 6.0 V
	t_{EH}	6.25			μs	μPD7516H only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltage table.

(3) Crystal oscillation.

(4) External clock.

Port 1 I/O Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5$ V to 6 V

μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5 V \pm 10\%$

$0.1 MHz \leq f_X, f_{XX} \leq 4.2 MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 output set-up time (to $\overline{PSTB}$ ↑)	t_{PST}	250			ns	(Note 1)
Port 1 output hold time (after $\overline{PSTB}$ ↑)	t_{STP}	100			ns	(Note 1)
$\overline{PSTB}$ pulse width low	t_{STL1}	450			ns	(Note 1)
Output data set-up time (to $\overline{PSTB}$ ↑)	t_{DST}	200			ns	(Note 2)
Output data hold time (after $\overline{PSTB}$ ↑)	t_{STD}	100			ns	(Note 2)

Port 1 I/O Operation (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input data valid time (after $\overline{PSTB}$ ↓)	t_{STDV}			700	ns	(Note 2)
Input data floating time (after $\overline{PSTB}$ ↑)	t_{STDF}	0			ns	(Note 2)
Control set-up time (to $\overline{PSTB}$ ↓)	t_{CST}	100			ns	(Note 2)
Control hold time	t_{STC}					
Output command		100			ns	(Note 2)
Input command		0		80	ns	(Note 2)
$\overline{PSTB}$ pulse width low	t_{STL2}	750			ns	(Note 2)

Note:

(1) Port output mode.

(2) I/O expander mode $V_{DD} = 4$ V to 6 V.

Port 1 I/O Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5$ V to 6.0 V

μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.75$ V to 5.5 V

$4.2 MHz \leq f_X, f_{XX} \leq 6.6 MHz$

Low Speed Mode(1) ($EM_2 = 0$)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 output set-up time (to $\overline{PSTB}$ ↑)	t_{PST}	400			ns	(Note 2)
Port 1 output hold time (after $\overline{PSTB}$ ↑)	t_{STP}	100			ns	(Note 2)
$\overline{PSTB}$ pulse width low	t_{STL1}	600			ns	(Note 2)
Output data set-up time (to $\overline{PSTB}$ ↑)	t_{DST}	400			ns	(Note 3)
Output data hold time (after $\overline{PSTB}$ ↑)	t_{STD}	100			ns	(Note 3)
Input data valid time (after $\overline{PSTB}$ ↓)	t_{STDV}			850	ns	(Note 3)
Input data floating time (after $\overline{PSTB}$ ↑)	t_{STDF}	0			ns	(Note 3)
Control set-up time (to $\overline{PSTB}$ ↓)	t_{CST}	400			ns	(Note 3)

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AC Characteristics (cont)

Port 1 I/O Operation (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Control hold time Output command	t_{STC}	100			ns	(Note 3)
Input command		0		80	ns	(Note 3)
$\overline{PSTB}$ pulse width low	t_{STL2}	1200			ns	(Note 3)

Note:
(1) The μPD82C43/8243H, etc, cannot interface with the μPD7516H in high speed mode ($EM_2 = 1$).
(2) Port output mode.
(3) I/O expander mode $V_{DD} = 4$ V to 6 V.

Serial Interface Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5$ V to 6 V
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	2.1			μs	$V_{DD} = 4$ V to 6 V; Input
		12.5			μs	μPD7516H only; Input
		(1)			μs	$V_{DD} = 4$ V to 6 V; Output
		(2)			μs	μPD7516H only; Output
$\overline{SCK}$ pulse width high, low	t_{KH}	0.7			μs	$V_{DD} = 4$ V to 6 V; Input
	t_{KL}	6.5			μs	μPD7516H only; Input
		(3)			μs	$V_{DD} = 4$ V to 6 V; Output
		(4)			μs	μPD7516H only; Output
SI set-up time (to $\overline{SCK}$ ↑)	t_{SIK}	300			ns	$V_{DD} = 4$ V to 6 V
		1000			ns	μPD7516H only
SI hold time (after $\overline{SCK}$ ↑)	t_{KSI}	450			ns	$V_{DD} = 4$ V to 6 V
		1000			ns	μPD7516H only
SO output delay time (after $\overline{SCK}$ ↓)	t_{KSO}			500	ns	$V_{DD} = 4$ V to 6 V for 7516H
				2000	ns	μPD7516H only

Note:
(1) High speed mode: $16/f_x$ or $16/f_{xx}$
Low speed mode: $64/f_x$ or $64/f_{xx}$
(2) $64/f_{xx}$ or $64/f_{xx}$
(3) High speed mode: $8/f_x$ or $8/f_{xx}$
Low speed mode: $32/f_x$ or $32/f_{xx}$
(4) $32/f_{xx} - 2.0\ \mu s$, or $32/f_{xx} - 2.0\ \mu s$

Other Operations

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5$ V to 6.0 V
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.75$ V to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
INT0 pulse width high, low	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width high, low	t_{I1H}, t_{I1L}	(1)			μs	
RESET pulse width high, low	t_{RSH}, t_{RSL}	10			μs	

Note:
(1) $26/f_x$ or $26/f_{xx}$

μPD75CG16H EPROM Characteristics

$T_A = -10°C$ to $+70°C$; $V_{DD} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Access time	t_{ACC}			700	ns	
$\overline{CE}$ low set-up time to data valid	t_{CE}			700	ns	
Data valid hold time to $\overline{CE}$ rising edge	t_{IH}	0			ns	

Operating Supply Voltages

$T_A = -10°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CPU (Note 1)		4.5		6.0	V	f_x, $f_{xx} = 4.2$ MHz to 6.6 MHz, (Note 3)
		4.0		6.0	V	$f_x = 0.1$ MHz to 4.2 MHz, $f_{xx} = 3.5$ MHz to 4.2 MHz, (Note 3)
		4.5		6.0	V	f_x, $f_{xx} = 4.2$ MHz to 6.6 MHz, (Note 4)
		2.5		6.0	V	$f_x = 0.1$ MHz to 4.2 MHz, $f_{xx} = 3.5$ MHz to 4.2 MHz, (Note 4)

AC Characteristics (cont)

Operating Supply Voltages (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Crystal oscillation circuit (Note 2)		4.5		6.0	V	f_{XX} = 4.2 MHz to 6.6 MHz, C1 = 10 pF, C2 ≤ 10 pF, (Note 5)
		2.7		6.0	V	C1 = 10 pF, C2 ≤ 10 pF, f_{XX} = 3.5 MHz to 4.2 MHz, (Note 5)
		2.85		6.0	V	C1 = 10 pF, C2 ≤ 22 pF, f_{XX} = 3.5 MHz to 4.2 MHz, (Note 5)
		2.5		6.0	V	External clock
Display controller		4.0		6.0	V	
PPG		4.0		6.0	V	
Port 1		2.5		6.0	V	Port output mode
		4.0		6.0	V	I/O expander mode

Note:

(1) Except the crystal oscillation circuit, display controller, PPG, and port 1.

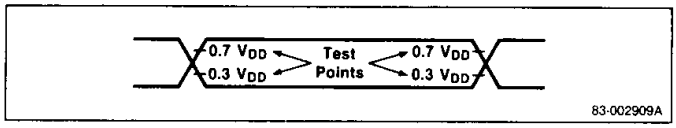
(2) The circuits in figure 19 and 20 are recommended.

(3) High speed mode, $EM_2 = 1$.

(4) Low speed mode, $EM_2 = 0$.

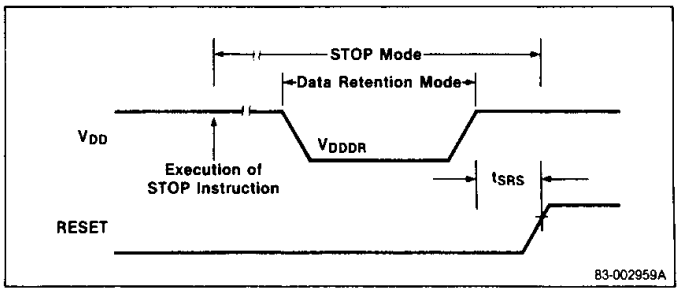
(5) Crystal Oscillator.

AC Waveform Measurement Points (Except X1, X2)

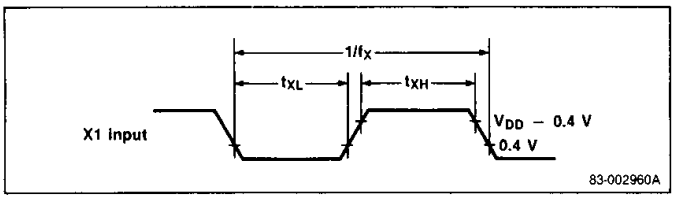


Timing Waveforms

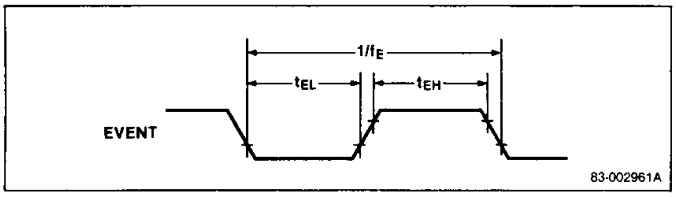
Data Retention Timing



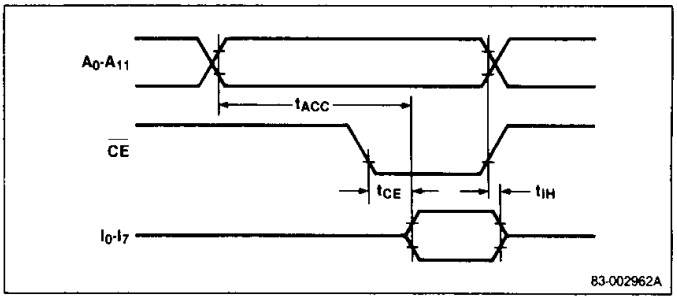
Clock Timing



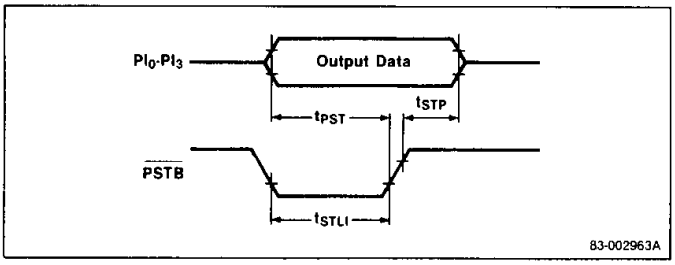
EVENT Timing



EPROM Timing

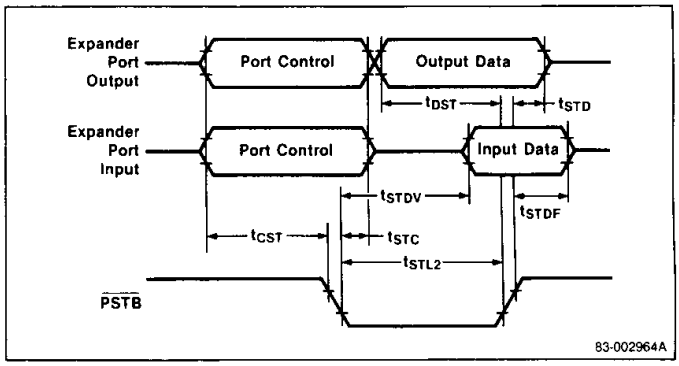


Strobe Output Timing

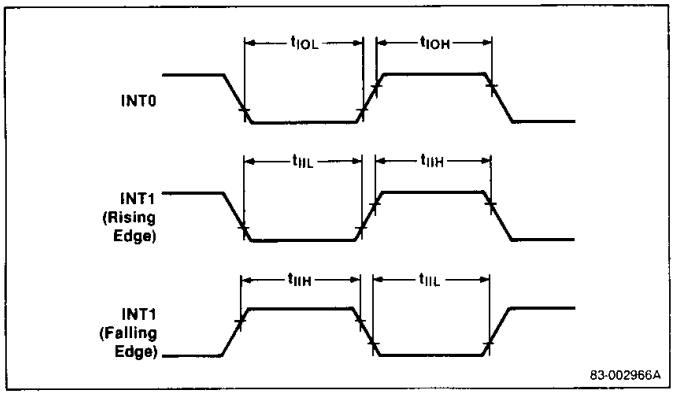


Timing Waveforms (cont)

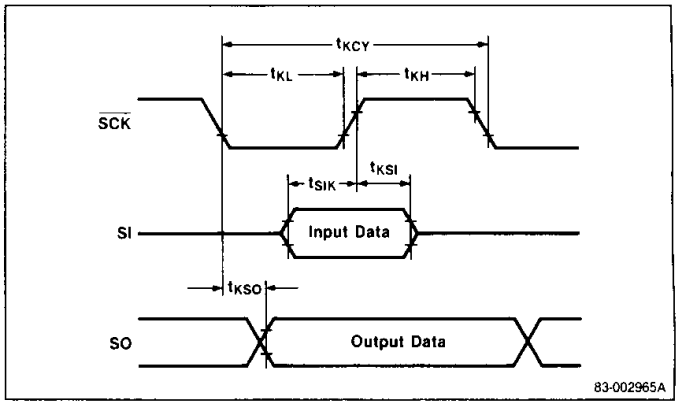
Port I/O Expander I/O Timing



Interrupt Input Timing



Serial Transfer Timing



RESET Input Timing

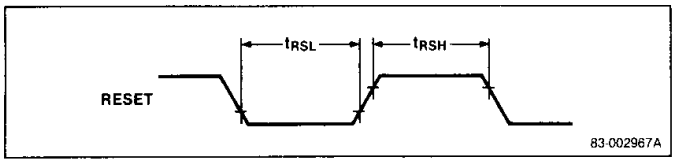


Figure 1. Digital Tuning System Application

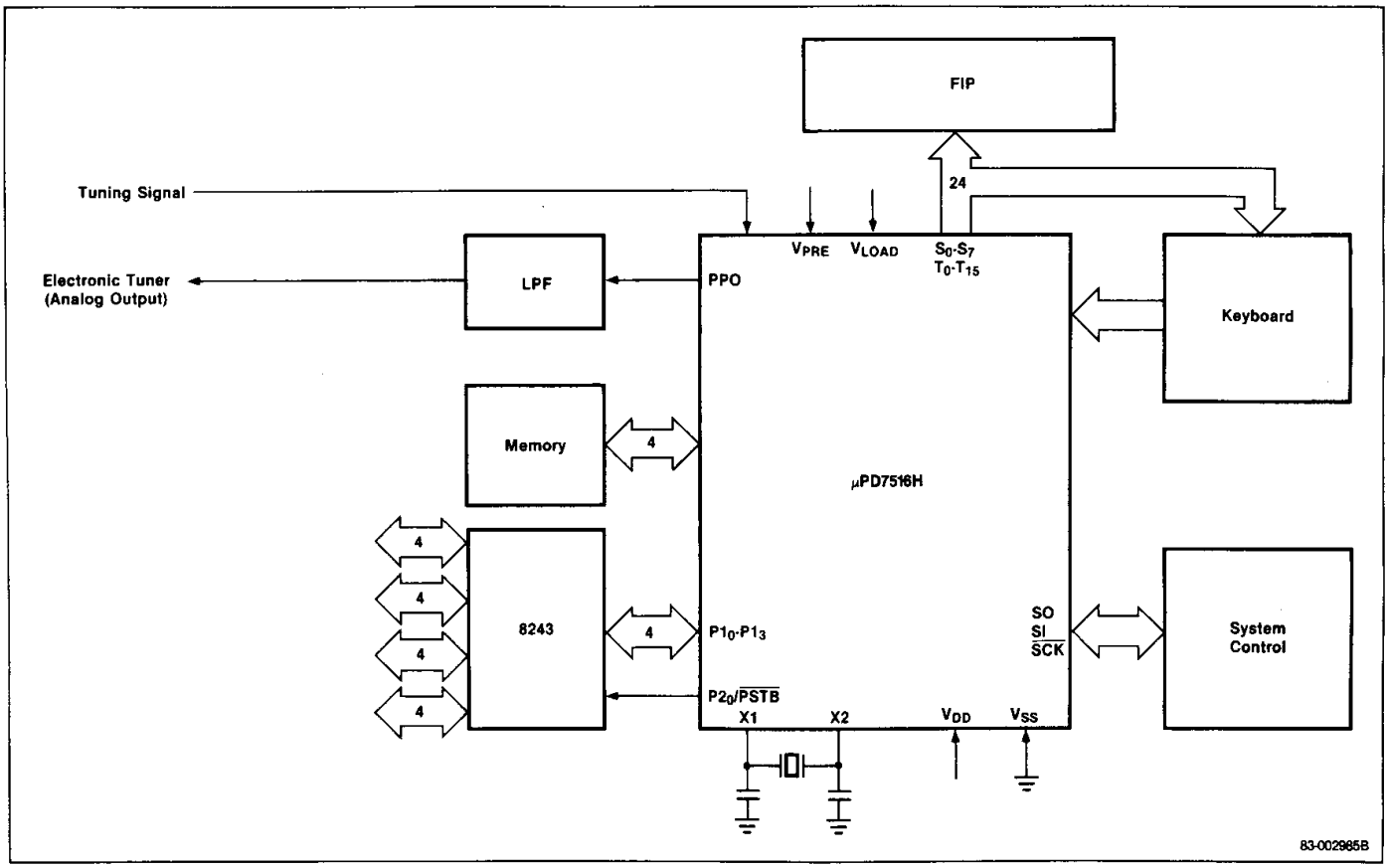


Figure 2. Telephone Application

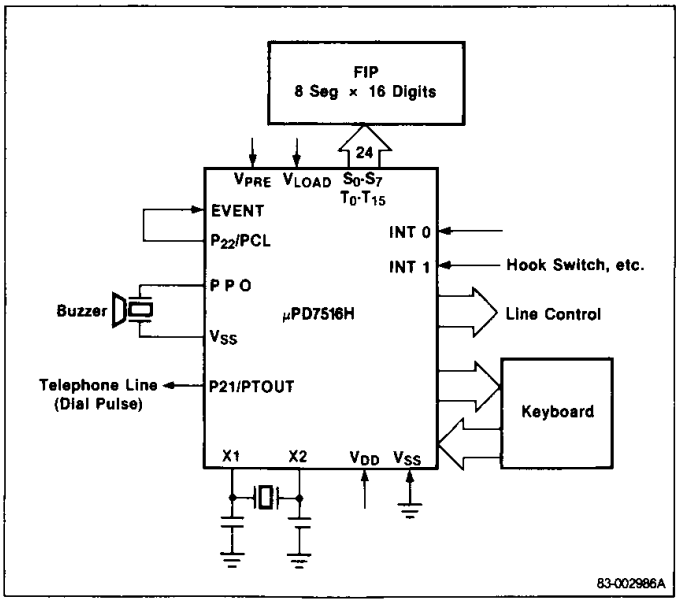


Figure 3. ECR Application

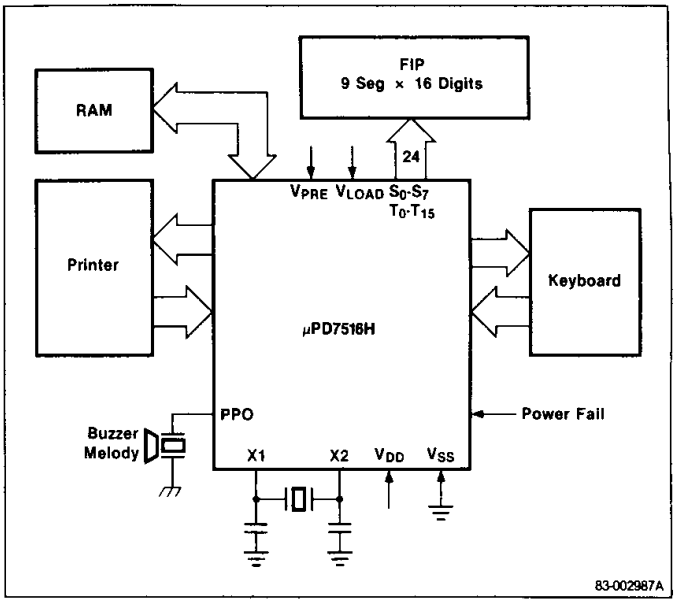
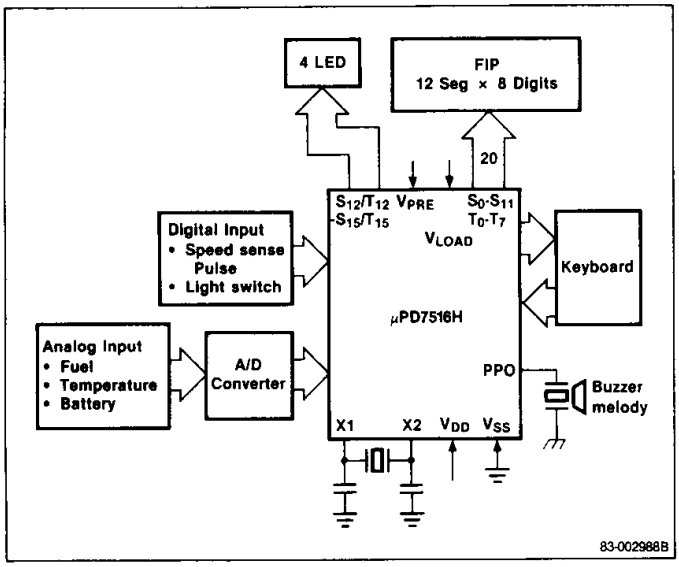


Figure 4. Automotive Equipment Application

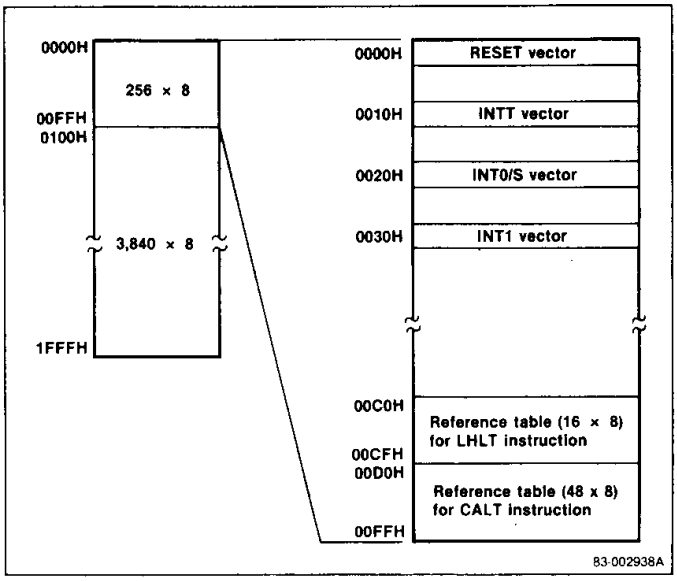


Functional Description

Program Memory (ROM), 6144 Words × 8 Bits

This mask-programmable memory is addressed by the bank flag (BNK) and the program counter (PC), and is used to store programs and table data. See figure 5.

Figure 5. Program Memory Map



General Purpose Registers

Four 4-bit general purpose registers (D, E, H, L) may be paired as follows for 8-bit operations: DE, HL, and DL. These 8-bit register pairs are commonly used as pointers to memory locations. When using the HL register pair as a data pointer, auto-increment and auto-decrement of the L register may be specified.

Data Memory (RAM), 256 Words × 4 Bits

This static RAM used to store display and operation data. It may also function with the accumulator (A) for 8-bit data processing.

There are three types of data memory addressing:

- Direct. Address designation is made on the second byte of the instruction.
- Register indirect. Address designation is made by the contents of a register pair designated by the instruction.
- Stack. Indirect address designation is made by the contents of the stack pointer (SP).

Data memory addresses are from 00H to 0FFH. The first 64 locations are pre-assigned as display data for the FIP display (00H to 03BH) and the programmable pulse generator (PPG) modulo section (03CH to 03FH). When display data is written in 00H-03BH, the FIP controller/driver automatically reads it and generates drive signals for the FIP. See figure 6.

Addresses 00H-03FH cannot be accessed by stack operations. RAM locations 40H-0FFH can be used as a stack area addressed by the SP. This data memory area is used when executing call or return instructions (CALL, CALT, RT, RTS, RTSPW), push/pop instructions (PSHDE, PSHHL, POPDE, POPHL), and when answering an interrupt.

When executing a call instruction or interrupt occurence with interrupts enabled, the contents of the PC and program status word (PSW) are stored in the stack area. A push instruction stores the contents of DE or HL in the stack area. See figure 7.

Figure 6. Data Memory Map

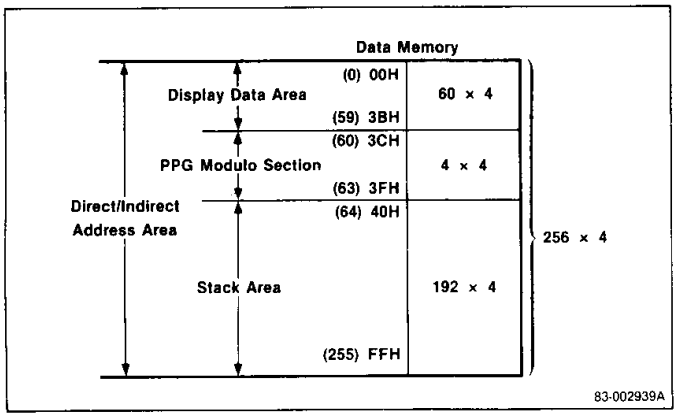
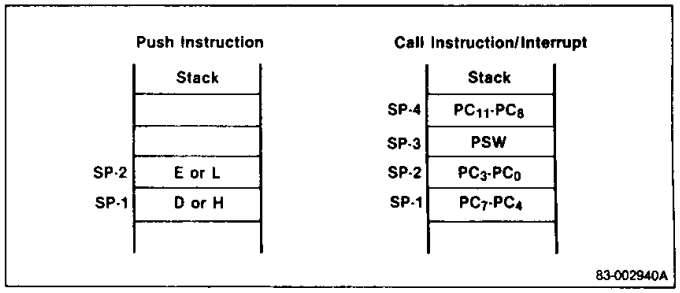


Figure 7. Push, Call, Interrupt



Clock Generator

The system clock generator consists of a crystal oscillator, a frequency divider, and a standby (stop/halt) mode control circuit, as shown in figure 8. When an external crystal is connected to X1 and X2, the crystal oscillator generates the f_{XX}. (The notation 'f_{XX}' is used when referring to crystal oscillation; 'f_X' is used when an external clock is input.) It is also possible to obtain a clock by inputting an external clock into X1 and an inverted clock to X2.

The frequency divider divides the output of the crystal oscillator into four frequencies, as follows:

- 1/2 (pulse generator clock, PPG)
- 1/8 (system clock, CLH)
- 1/32 (system clock, CLL; and FOP controller clock, FIP)
- 1/128 (timer/event counter clock)

The system clock (CL) may be 1/8 or 1/32 frequency-divided, depending on the state of expansion mode register bit 2 (EM_2). $EM_2 = 1$ selects 1/8, and $EM_2 = 0$ selects 1/32. CL is supplied to all circuits except the FIP controller and PPG, which use the $f_{XX} \times 1/32$ and $f_{XX} \times 1/2$, respectively. CL is 1/2 frequency divided to supply the CPU (ϕ) clock. CL is an input to the clock control circuitry used to generate the count pulse (CP) used by the timer/event counter.

The standby mode control circuit consists mainly of the stop and halt flip-flops. The stop flip-flop, when set, stops the crystal oscillator. There is no input to the frequency divider, so no clocks are output to the μPD7516H circuitry. The STOP instruction sets the stop flip-flop; RESET clears it. The halt flip-flop, when set, inhibits the input to the 1/2 frequency divider that generates ϕ, thereby stopping ϕ. A HALT or STOP sets this flip-flop; it is reset by the RELEASE signal (generated when an interrupt flag is set) or at the falling edge of the internal reset (IRESET) signal. (IRESET is released after a waiting time following the release of the external RESET input.)

Figure 8. Clock Generator Circuit

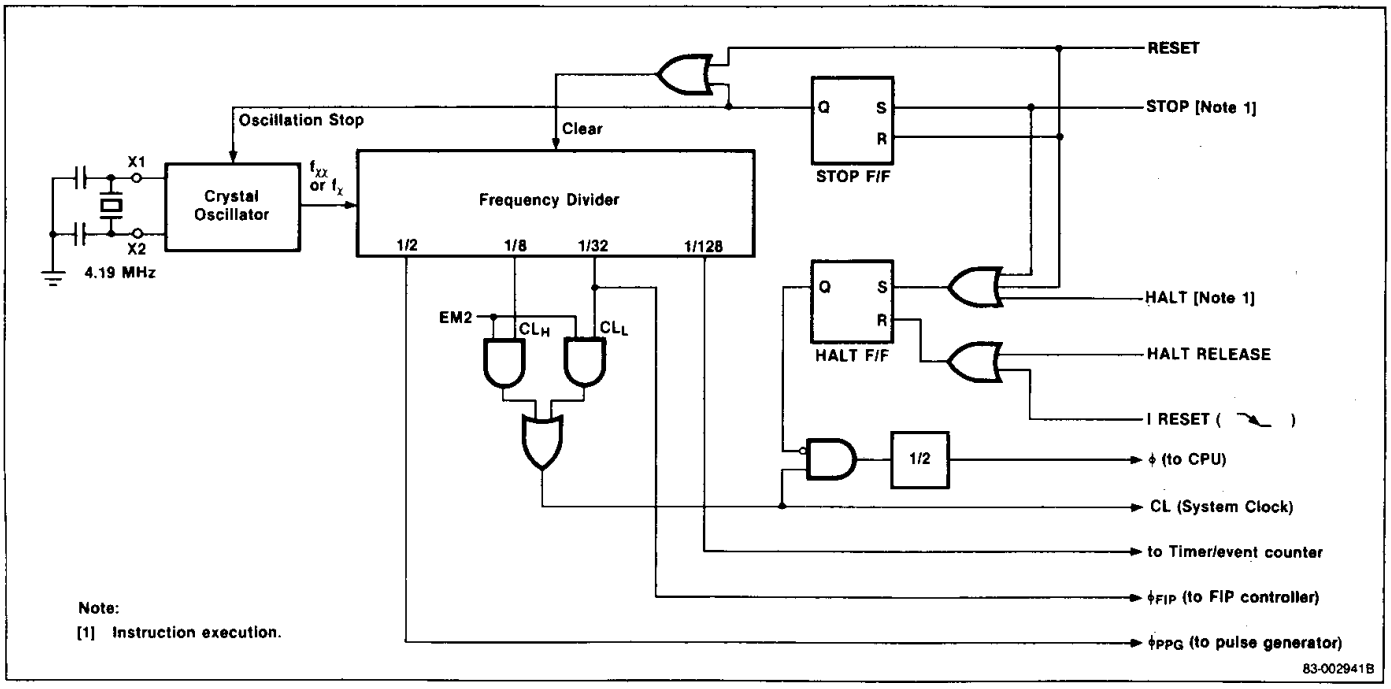
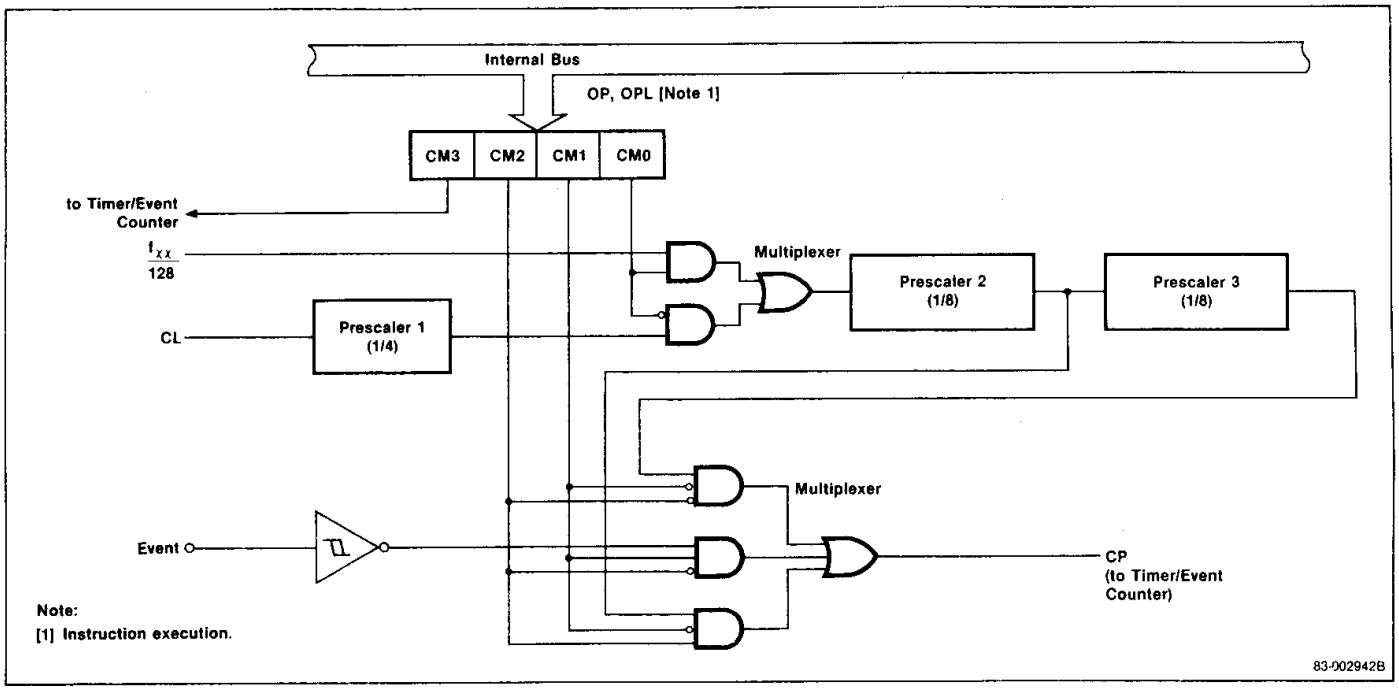


Figure 9. Clock Control Circuit



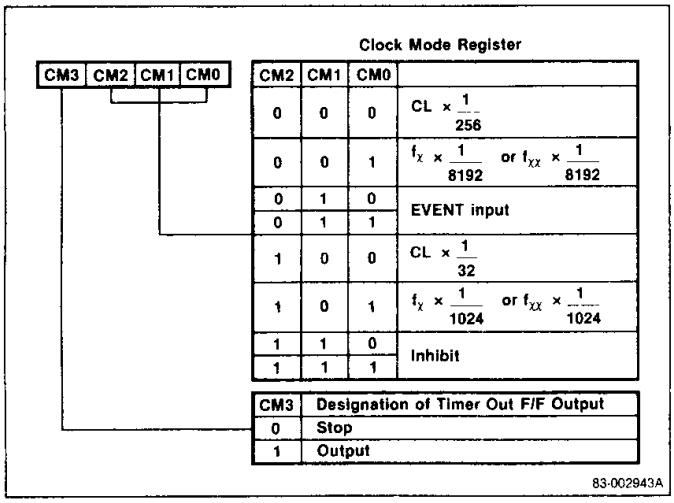
Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CM_0–CM_3), three prescalers, and a multiplexer, as shown in figure 9. The circuit generates the clock pulse (CP) input to the timer/event counter from the following inputs:

- System clock (CL)
- $1/128$ divided clock from the crystal oscillator ($f_{XX}/128$)
- External EVENT pulse

Bit CM_0–CM_2 determine the clock input selection and divide ratio. CM_3 gates the output of a timer out signal from the PTOUT ($P2_1$) pin. When $CM_3 = 1$, output from the timer out flop-flop (TOUT) is output to $P2_1$. Executing an OP or OPL instruction loads the clock mode register. The format of the clock mode register is shown in figure 10.

Figure 10. Clock Mode Register



Timer/Event Counter

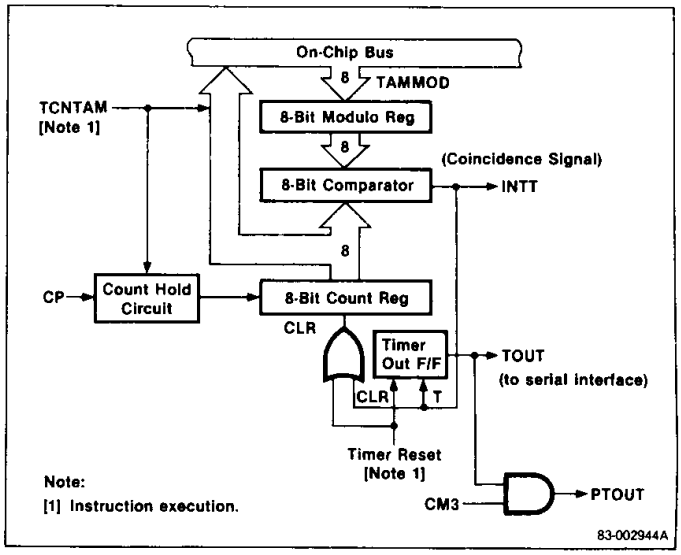
This counter consists of an 8-bit counter register, an 8-bit modulo register, an 8-bit comparator, and a timer-out flip-flop, as shown in figure 11.

The 8-bit count increments at every rising edge of the clock pulse (CP). It is cleared to 0 when executing the TIMER instruction, a RESET input, or a coincidence signal from the comparator.

The modulo register determines the INTT signal interval. The contents of this register are set via the TAMMOD instruction. RESET sets the contents to 0FFH.

The timer-out flip-flop inverts with every INTT signal output from the comparator. Its output, TOUT, can by sent to the PTOUT pin when bit 3 (CM_3) of the clock mode register is set. TOUT may also be used as a serial clock source to the serial interface.

Figure 11. Structure of the Timer/Event Counter



Serial Interface

The serial interface is used for serial data I/O. It consists of an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter, as shown in figure 12. Figure 13 shows the serial shift timing.

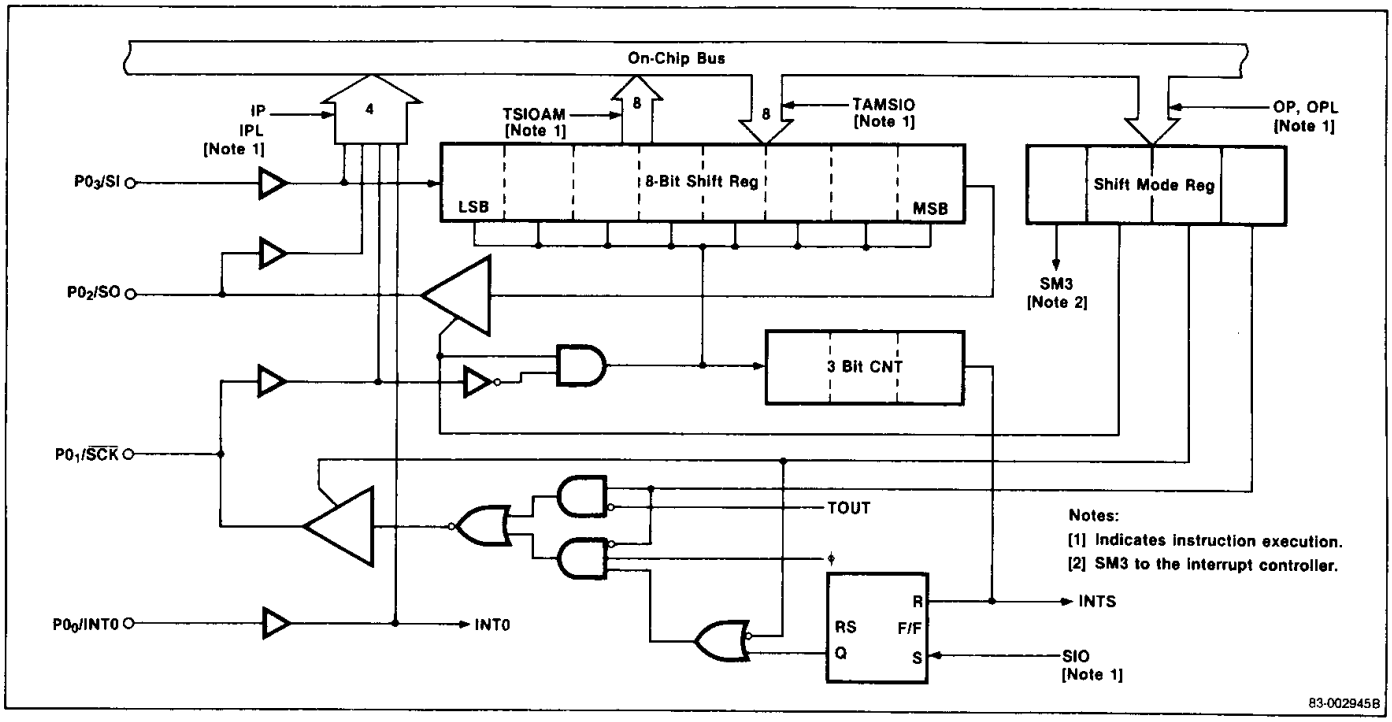
The serial clock ($\overline{SCK}$) controls the serial data communication rate. An 8-bit byte clocks into the serial input (SI) port or out of the serial output (SO) port starting with the MSB. Data transmission occurs synchronously with the falling edge of $\overline{SCK}$. Data reception occurs synchronously with the rising edge of $\overline{SCK}$.

The 3-bit counter counts the number of serial clock pulses. When a byte of serial data is transferred, an internal interrupt signal (INTS) is generated. Selecting INTS (setting SM_3 of the shift mode register to 0) sets the interrupt request flag, INT0/S RQF.

The end of transfer of each byte can also be verified by testing INTS RQF with the SKI instruction instead of interrupt processing.

3

Figure 12. Serial Interface Block Diagram



CPU Clock (ϕ)

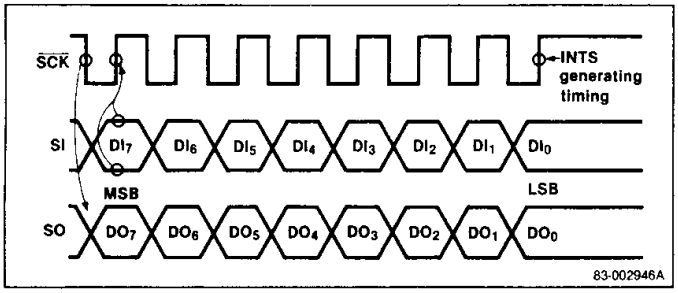
When the SIO instruction executes, eight CPU clock pulses (ϕ) are supplied to the serial interface for the serial clock and output from $\overline{SCK}$. After the eighth clock, $\overline{SCK}$ is fixed high level, automatically stopping serial data I/O after one byte has transferred.

$\overline{SCK}$ does not have to be software controlled. Its transfer rate is determined by the frequency of ϕ. See table 1.

Table 1. $\overline{SCK}$ Frequencies

f_{XX}	Low Speed Mode	High Speed Mode
6.55 MHz	102.4 kHz	409.6 kHz
4.19 MHz	65.5 kHz	262 kHz

Figure 13. Serial Shift Timing



Interrupt Function

There are two external and two internal interrupts, with the specifications listed in table 2. The external interrupt INT0 uses the $P0_0$ port pin as the interrupt signal input, and has the same interrupt process as the internal serial interrupt INTS. Selection of the interrupt is programmable and depends on the application.

Table 2. Interrupt Specifications

Source	Int/ Ext	Priority	Vector Address
INTT (coincidence signal from timer / event counter)	int	1	10H(16)
INT0 (interrupt signal from $P0_0$ terminal)	ext	2	20H(32)
INTS (end of transfer signal from serial interface)	int	2	20H(32)
INT1 (interrupt signal from INT1 terminal)	ext	3	30H(48)

Interrupt Sequence

When an interrupt goes active, the following occur:

- A corresponding interrupt request flag is set.
- The interrupt master enable flip-flop is reset.
- The contents of the PC and PSW are saved in the stack.
- An interrupt start address is generated and jumped to.
- The interrupt request flag set by the interrupt is reset.

Two machine cycles are required for interrupt execution, one for saving the return address and one for jumping to the interrupt start address. If several interrupts occur simultaneously, all respective request flags are set, and the interrupt with the highest priority is processed. The remaining interrupts are pending until serviced by reenabling the master interrupt flip-flop or until their interrupt request flags are reset by executing a SKI instruction.

Figure 14 is a block diagram of the interrupt control circuit.

FIP Controller/Driver

The FIP controller/driver consists of 60 4-bit nibbles of display memory (000-03BH of data RAM), a 4-bit display mode register (DM_3-DM_0), a 4-bit timing mode register (TM_3-TM_0), a 4-bit blanking mode register (BM_3-BM_0), an output selector, and a high voltage output driver. See figure 15.

The FIP controller/driver has 24 outputs for directly driving a high voltage vacuum fluorescent display:

- 8 segment signal outputs (S_0-S_7)
- 8 timing signal (grid) outputs (T_0-T_7)
- 8 timing or segment outputs (T_8/S_8-T_{15}/S_{15})

The contents of the display mode register determines which of the five display modes is available to the user. The modes are as follows:

- Static mode
  - 24 static output
- Dynamic mode
  - 8 segment mode
  - 12 segment mode I
  - 12 segment mode II
  - 16 segment mode

The contents of the timing mode register determine the number of display digits (1-16) and control the number of timing signals (T_0-T_{15}) output. Timing signals drive the grids of vacuum fluorescent display tubes. The voltage on the grid will determine the brightness of a digit (made up of one or more segments) or if the digit will be turned on or off.

The width of the timing signal pulse can be adjusted at eight independent steps by the value loaded into the blanking mode register. This function is useful for dimming control and for preventing display cross-talk of adjacent digits.

The active level of the timing signal can be designated high or low by bit DM_3.

Figure 14. Interrupt Control Circuit Block Diagram

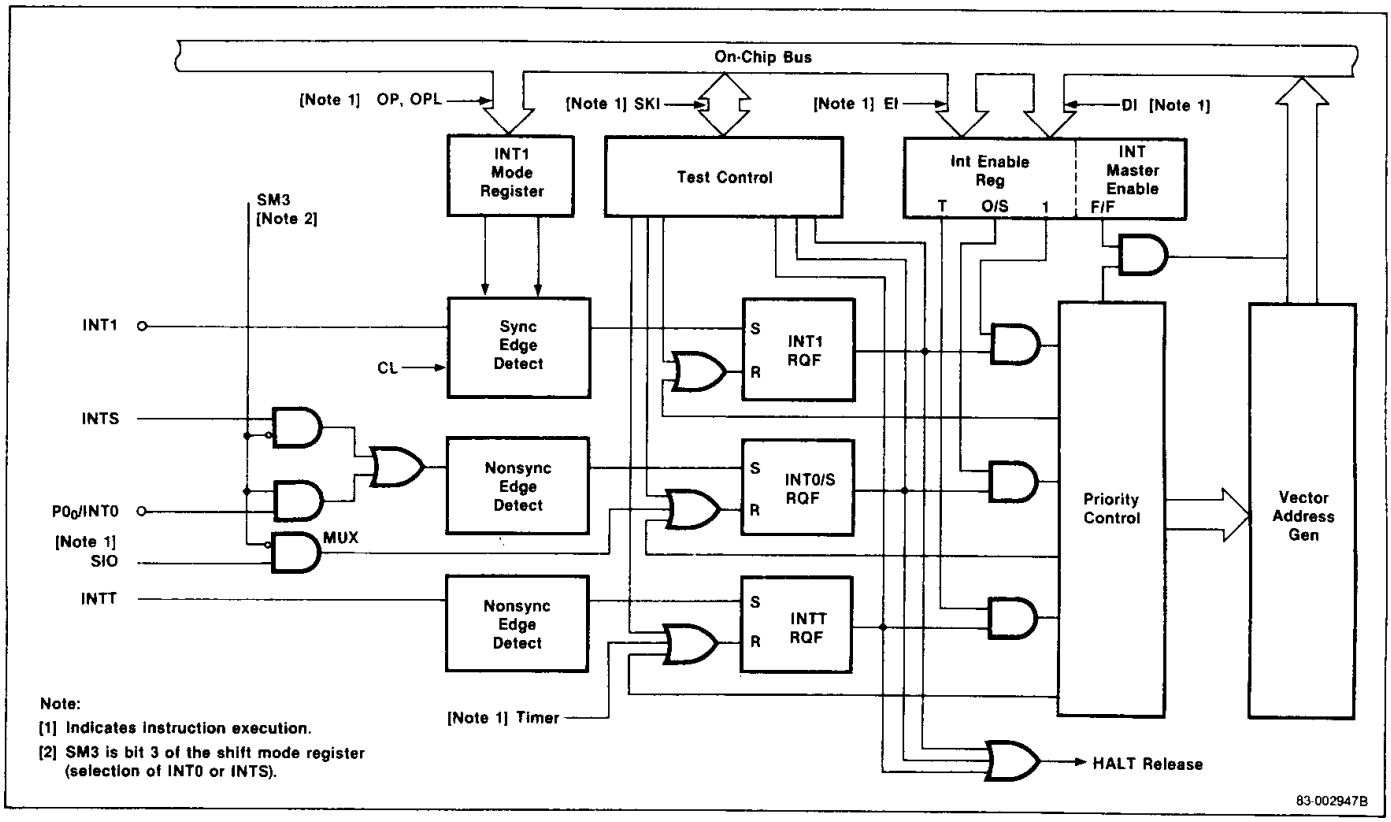
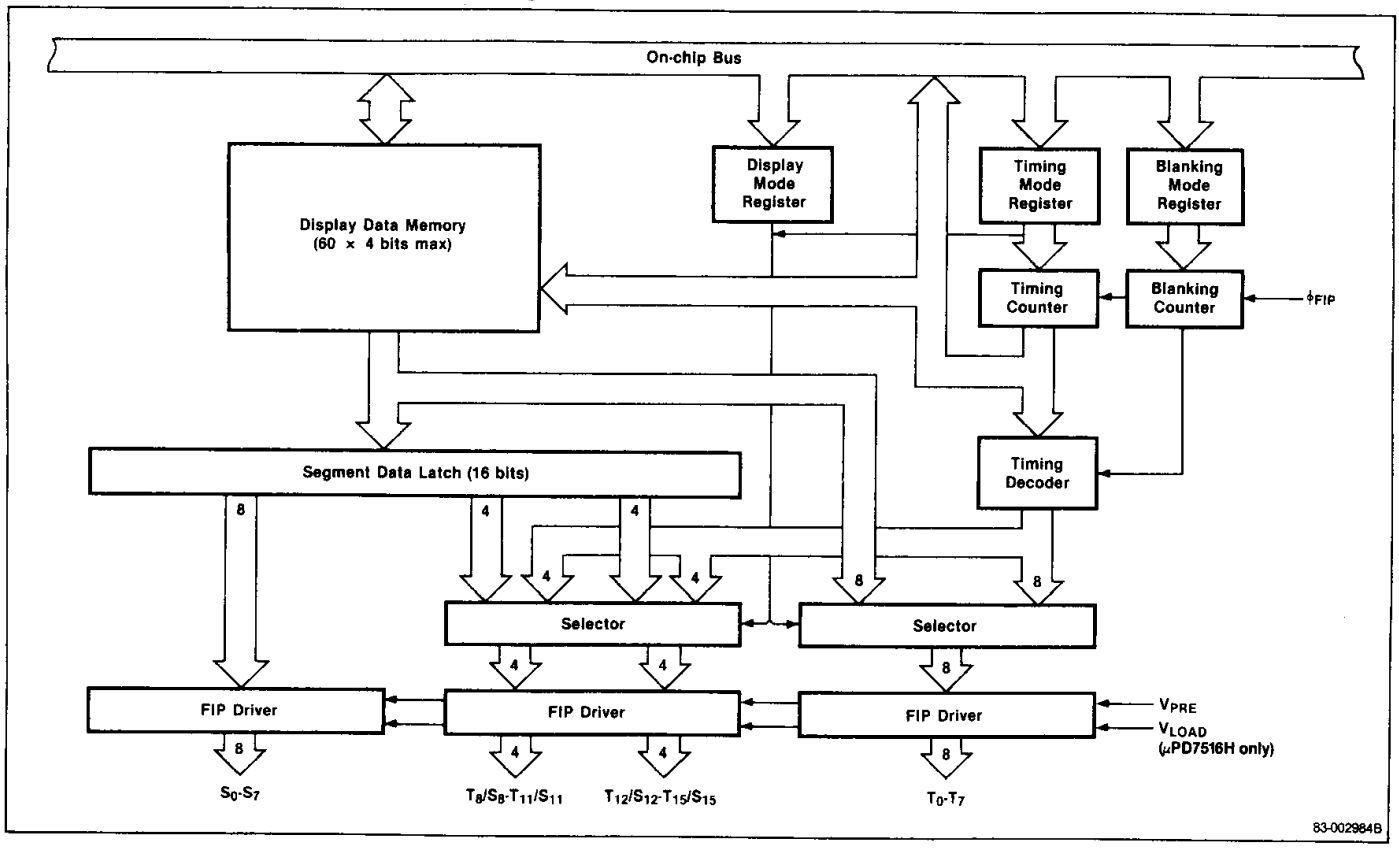


Figure 15. FIP Controller/Driver Block Diagram



Display Mode Register (DM)

This 4-bit write-only register (DM_3–DM_0) determines the display mode (dynamic, static, and off) of the FIP controller/driver. It also determines the active level of the display timing signals. This is shown in figure 16.

The DM register has an output address of 0BH and is accessed by the output instructions OP and OPL when bit EM3 of the expansion mode register is set. The DM register is cleared by a RESET.

Figure 17 shows a display example in 12-segment mode I.

Figure 16. Display Mode Register Format

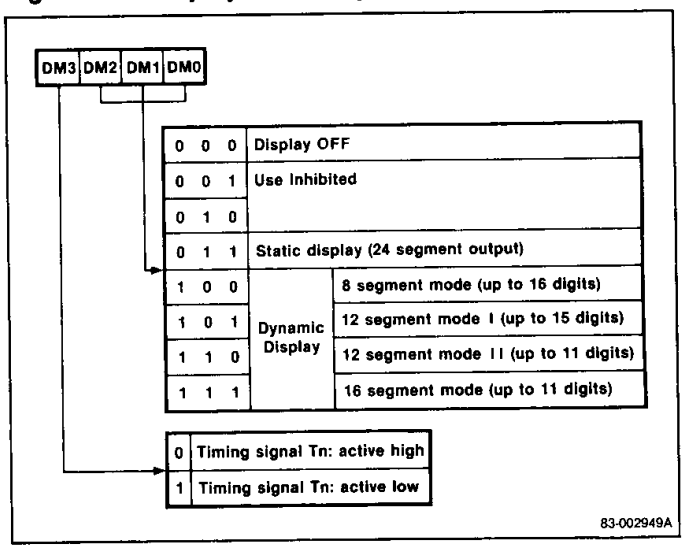
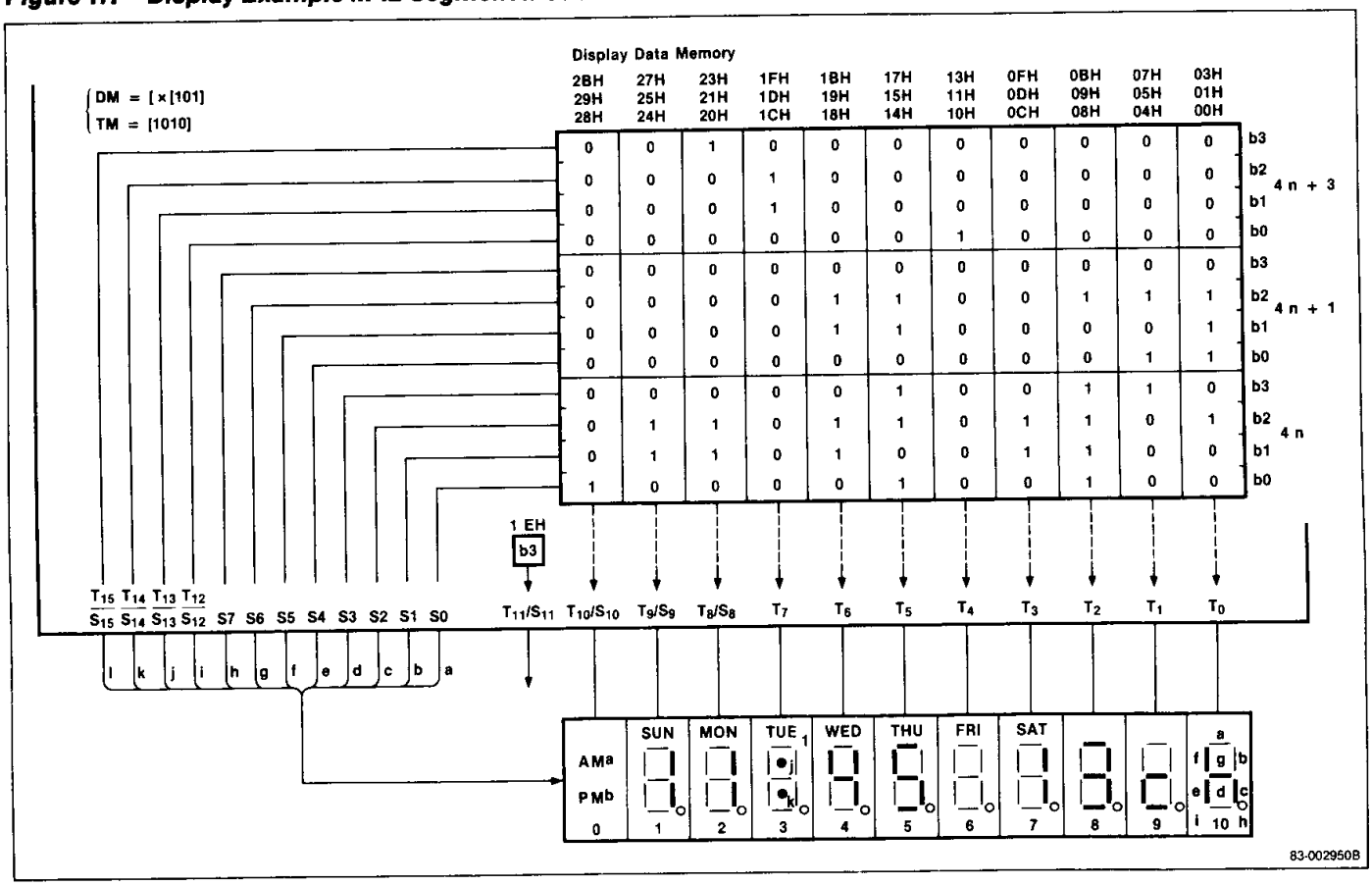


Figure 17. Display Example in 12-Segment Mode I



Standby Function

Two standby modes, stop and halt, hold device power consumption to a minimum. Stop mode is entered via the STOP instruction, and halt mode is entered via the HALT instruction. In stop mode, all clocks are stopped. In halt mode, only the CPU clock (ϕ) is stopped.

Stop mode can only be released by a RESET. Halt mode may be released either by a RESET or by the setting of an interrupt request flag.

Stop Mode

In stop mode, the contents of memory are retained, and all other functions are stopped. RESET releases stop mode.

In stop mode, the X1 input is internally shorted to V_{SS} in order to hold the crystal oscillator leakage to a minimum. A system using stop mode cannot use an external clock.

Halt Mode

When no interrupt flags are set, the HALT instruction causes the device to enter halt mode. In this mode, only ϕ stops; all other clocks continue to operate. The following functions continue to operate:

- Clock oscillation
- Frequency division and output of clocks other than ϕ
- Event input
- Timer/event counter
- Serial interface (except when ϕ is used as SCK)
- FIP controller/driver
- PPG
- Interrupts (INT0, INTS, INTT, INT1)
- RESET

Since a set interrupt flag releases the device from halt mode, this mode cannot be entered if an interrupt request flag is set. It is therefore necessary to reset the request flag(s) either by answering the interrupt(s) (setting the interrupt master enable F/F and process interrupt) or by executing the SKI instruction.

In halt mode, CPU power consumption is eliminated. To hold power consumption to a minimum, all unnecessary circuits should be inactive and the steps below should be taken:

- Set the system clock (CL) to low speed
- Set the FIP controller/driver to the off mode
- Set the PPG for static operation
- Stop $\overline{SCK}$ input

Low Supply Voltage Data Retention (μPD7516H only)

Data retention is possible with V_{DD} as low as 2 V. V_{DD} should be lowered after the device is put in stop mode and while RESET is inactive. Stop mode cannot be released in low voltage data retention mode; V_{DD} should first be raised to normal operation.

Release of Stop Mode

RESET releases stop mode. On RESET's rising edge, the device mode changes to halt mode, starting clock oscillation. At the falling edge of RESET, a waiting time (about 62.5 ms/4.19 MHz, 40 ms/6.55 MHz) elapses, allowing for stabilization of crystal operation; following this the halt mode is released. After normal RESET operation, the CPU begins program execution from address 0000H.

In the release operation, the contents of data memory are retained while the contents of other registers become undefined.

Power-on Reset Circuit

An example of the simplest power-on reset circuit using a resistor and capacitor is shown in figure 18.

Figure 18. Power-on Reset Circuit

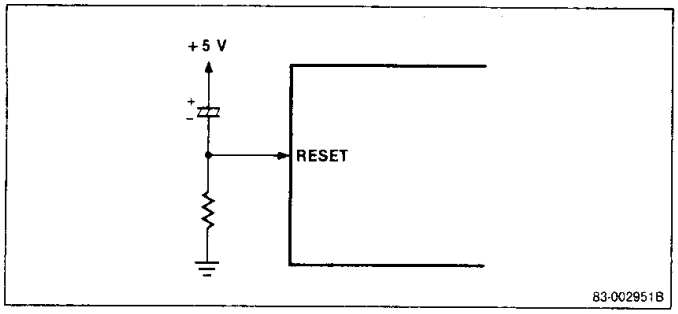


Figure 19. Crystal

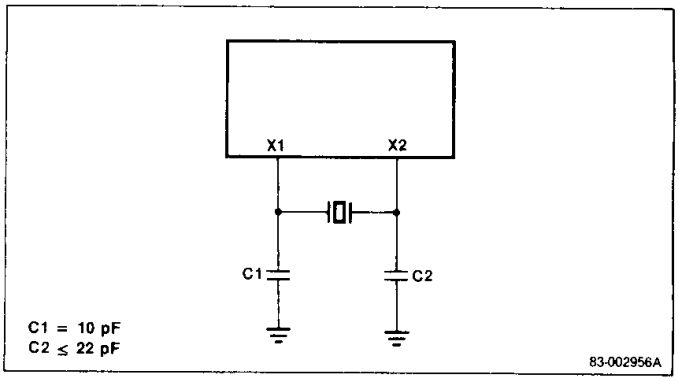


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Figure 20. External Clock

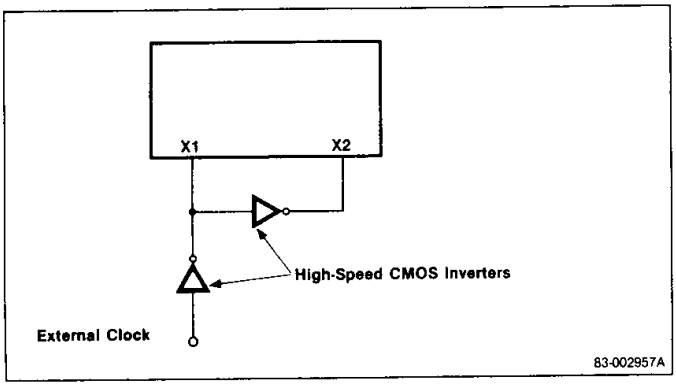
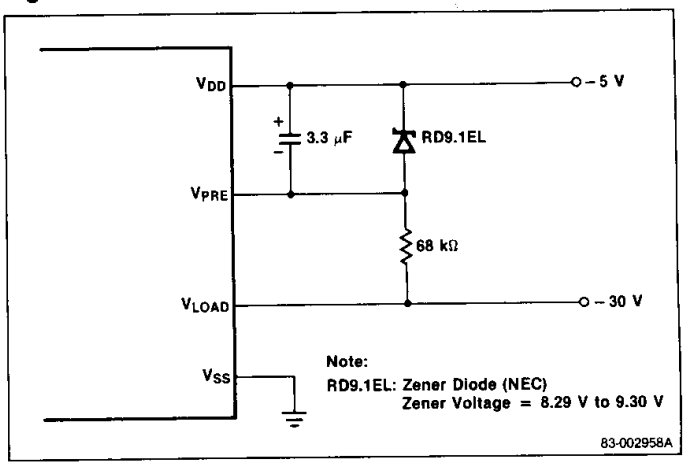
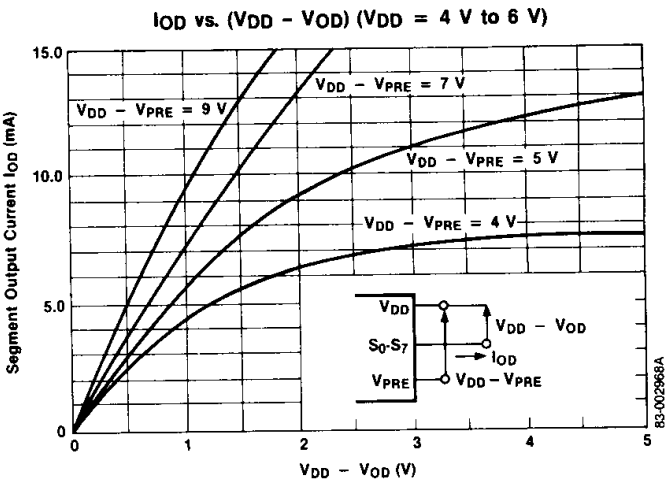


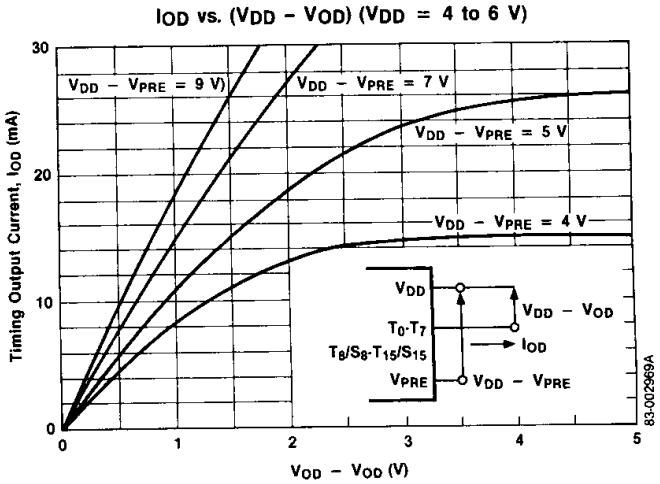
Figure 21. External Circuit

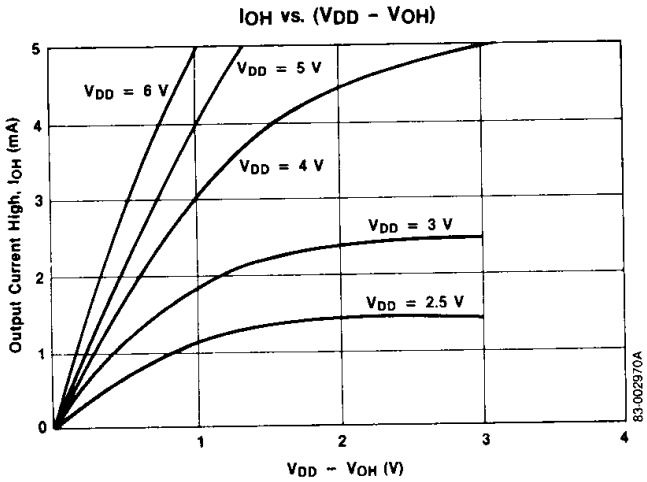


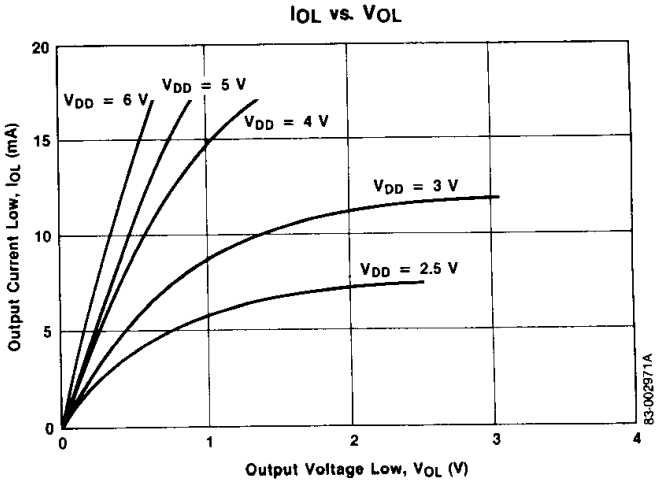
Operating Characteristics

$T_A = 25°C$



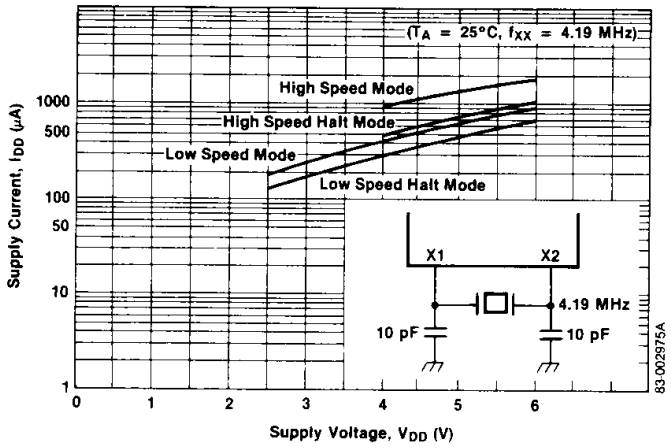




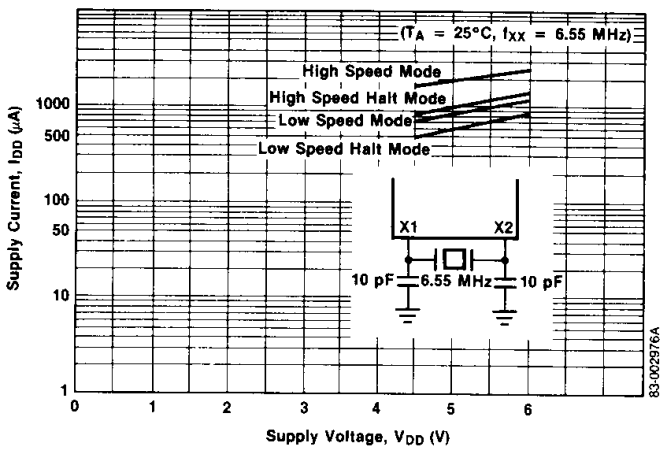


Operating Characteristics (cont)

I_{DD} vs. V_{DD}



I_{DD} vs. V_{DD}



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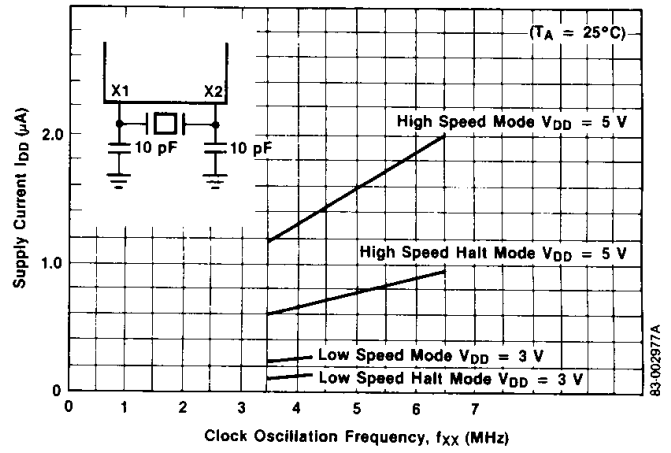
I_{DD} vs. f_{XX}



I_{DD} vs. f_X