NEC

NEC Electronics Inc.

μPD7507H/08H/75CG08HE 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

May 1987

Description

The μPD7507H, μPD7508H, and μPD75CG08HE are pin-compatible, high-speed (4.19 MHz), 4-bit, single-chip CMOS microcomputers with the μPD7500 series architecture. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Thirty-two I/O lines are organized into eight 4-bit ports: input port/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, 6, and 7.

The μPD7507H and μPD7508H execute 92 instructions of the μPD7500 series A instruction set with a 2.86-μs instruction cycle time.

Maximum power consumption is 3 mA at 5 V and less in the HALT and STOP low-power modes.

The 75CG08HE is a piggyback EPROM prototyping chip that is pin-compatible with 7507H and 7508H. A 2716 plugged into the top of the 75CG08HE emulates the ROM of a 7507H. A 2732 emulates the ROM of 7508H. When emulating the 7507H, the user must take care to use only the first 128 RAM locations. Although 7507H and 7508H can operate over a range of 2.7 to 6.0 V, 75CG08HE is limited to 5 V ±10%. Table 1 summarizes the differences among 7507H, 7508H, and 75CG08HE.

Features

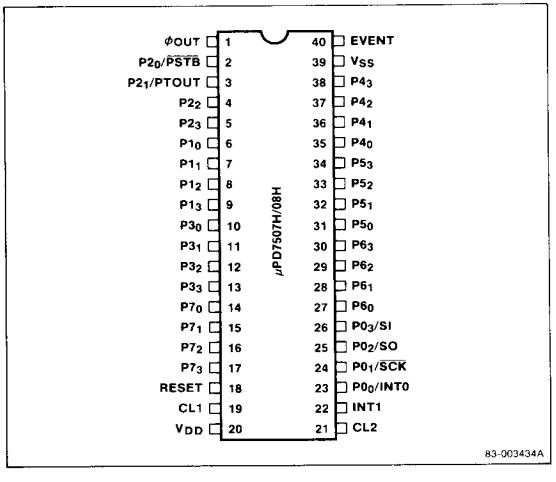
- ☐ Single-chip microcomputer
- ☐ Program ROM
  - — μPD7507H: 2048 x 8-bit
  - — μPD7508H: 4096 x 8-bit
  - — μPD75CG08HE: piggyback EPROM
- ☐ Data RAM
  - — μPD7507H: 128 x 4-bit
  - — μPD7508H: 224 x 4-bit
  - — μPD75CG08HE: 224 x 4-bit
- ☐ 8-bit timer/event counter
- ☐ Four 4-bit general purpose registers
- ☐ Four vectored, prioritized interrupts
- ☐ Executes 92 instructions of 7500 series A instruction set
- ☐ 2.86-μs instruction cycle/4.19-MHz external clock
- ☐ Two standby modes
- ☐ 32 I/O lines
- ☐ LED direct drive (ports 2-5; 16 lines)
- ☐ Low power HALT and STOP modes

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7507HC	40-pin plastic DIP	4.19 MHz
μPD7507HCU	40-pin plastic shrink DIP	4.19 MHz
μPD7507HG-22	44-pin plastic miniflat	4.19 MHz
μPD7508HC	40-pin plastic DIP	4.19 MHz
μPD7508HCU	40-pin plastic shrink DIP	4.19 MHz
μPD7508HG-22	44-pin plastic miniflat	4.19 MHz
μPD75CG08HE	40-pin ceramic piggyback DIP	4.19 MHz

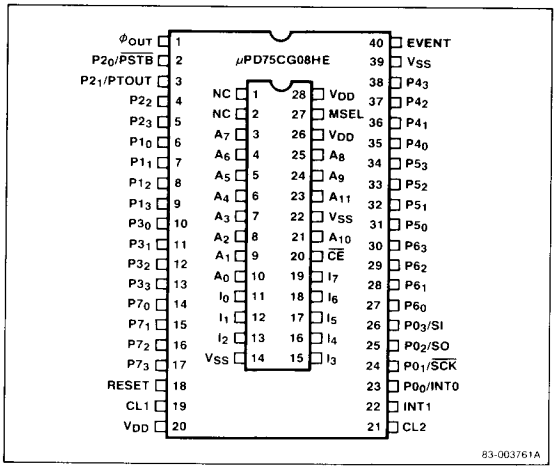
Pin Configurations

40-Pin Plastic DIP and Plastic Shrink DIP

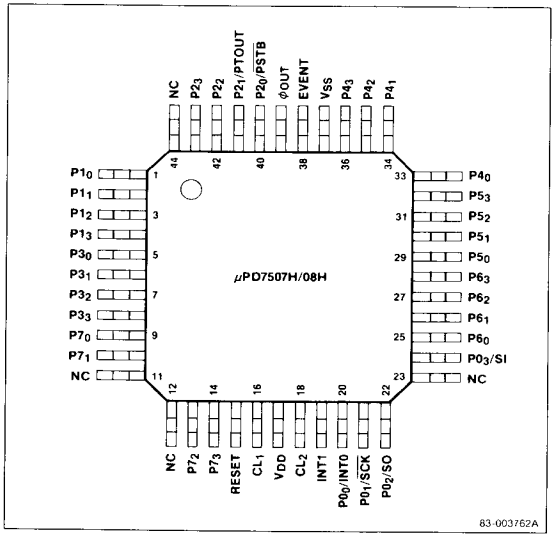


Pin Configurations (cont)

40-Pin Ceramic Piggyback DIP



44-Pin Plastic Miniflat



Pin Identification

40-Pin DIP, Shrink DIP, and Piggyback DIP

No.	Symbol	Function
1	Φ_{OUT}	$f_{CC}/12$ square wave
2-5	$P2_0/\overline{PSTB}$ $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0$/INT0, $P0_1/\overline{SCK}$, $P0_2$/SO $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_0$-$P4_3$	I/O port 4
39	V_{SS}	Ground
40	EVENT	External event input port

44-Pin Miniflat

No.	Symbol	Function
1-4	$P1_0$-$P1_3$	I/O port 1
5-8	$P3_0$-$P3_3$	Port 3 output
9, 10, 13, 14	$P7_0$-$P7_3$	I/O port 7
11-12	NC	Not connected
15	RESET	RESET input
16, 18	CL1, CL2	System clock inputs
17	V_{DD}	Positive power supply
19	INT1	External interrupt 1
20	$P0_0$/INT0	Port 0 input/Interrupt 0
21	$P0_1/\overline{SCK}$	Port 0 input/Serial clock I/O
22	$P0_2$/SO	Port 0 input/Serial output
23	NC	Not connected
24	$P0_3$/SI	Port 0 input/Serial output
25-28	$P6_0$-$P6_3$	I/O port 6
29-32	$P5_0$-$P5_3$	I/O port 5
33-36	$P4_0$-$P4_3$	I/O port 4

Pin Identification (cont)

44-Pin Miniflat (cont)

No.	Symbol	Function
37	V_{SS}	Ground
38	EVENT	External event input
39	ϕ_{OUT}	$f_{CC}/12$ square wave
40	$P2_0/\overline{PSTB}$	Port 2 output/Output strobe pulse
41	$P2_1$/PTOUT	Port 2 output/Timer out F/F signal
42, 43	$P2_2$, $P2_3$	Port 2 output
44	NC	Not connected

28-Pin EPROM Socket on Piggyback DIP

No.	Symbol	Function
1, 2	NC	Not connected
3-10	A_7-A_0	Address bits 7-0
11-13	I_0-I_2	Data bits 0-2
14, 22	V_{SS}	Ground
15-19	I_3-I_7	Data bits 3-7
20	$\overline{CE}$	Chip enable
21, 23	A10, A11	Address bits 10, 11
24, 25	A9, A8	Address bits 9, 8
26, 28	V_{DD}	Positive power supply
27	MSEL	Memory select

Pin Functions

$P0_0$/INT0, $P0_1/\overline{SCK}$, [Port 0/External Interrupt, Serial Interface] $P0_2$/SO, $P0_3$/SI

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1/\overline{SCK}$, $P0_2$/SO, or $P0_2$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0/\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0/\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

ϕ_{OUT} [Clock Out]

Outputs a square wave with frequency $f_{CC}/12$.

EVENT [External Event Input]

Pulses on this line are counted by the timer/event counter and an interrupt is generated when a predetermined count is reached.

CL1, CL2 [System Clock Input]

The system clock can be generated by connecting a crystal or a ceramic resonator across CL1 and CL2 and capacitors from each side of the crystal to ground. Alternatively a clock signal can be input to CL1 and its invert to CL2. See figure 1.

RESET [Reset]

A high level input to this pin initializes the μPD7507H/08H after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Table 1. Features Comparison

	μPD75CG08H	μPD7507H/7508H
Program memory	2K x 8 EPROM (2716) 4K x 8 EPROM (2732)	2K x 8 masked ROM (7507H) 4K x 8 masked ROM (7508H)
Data memory	224 x 4	128 x 4 (7507H) 224 x 4 (7508H)
Data retention mode	Use more current than 7507H, 7508H	Yes
Power supply	5 V ±10%	2.7 to 6.0 V
Package types	40-pin ceramic piggyback DIP	40-pin plastic DIP 40-pin plastic shrink DIP 44-pin plastic miniflat

Block Diagram

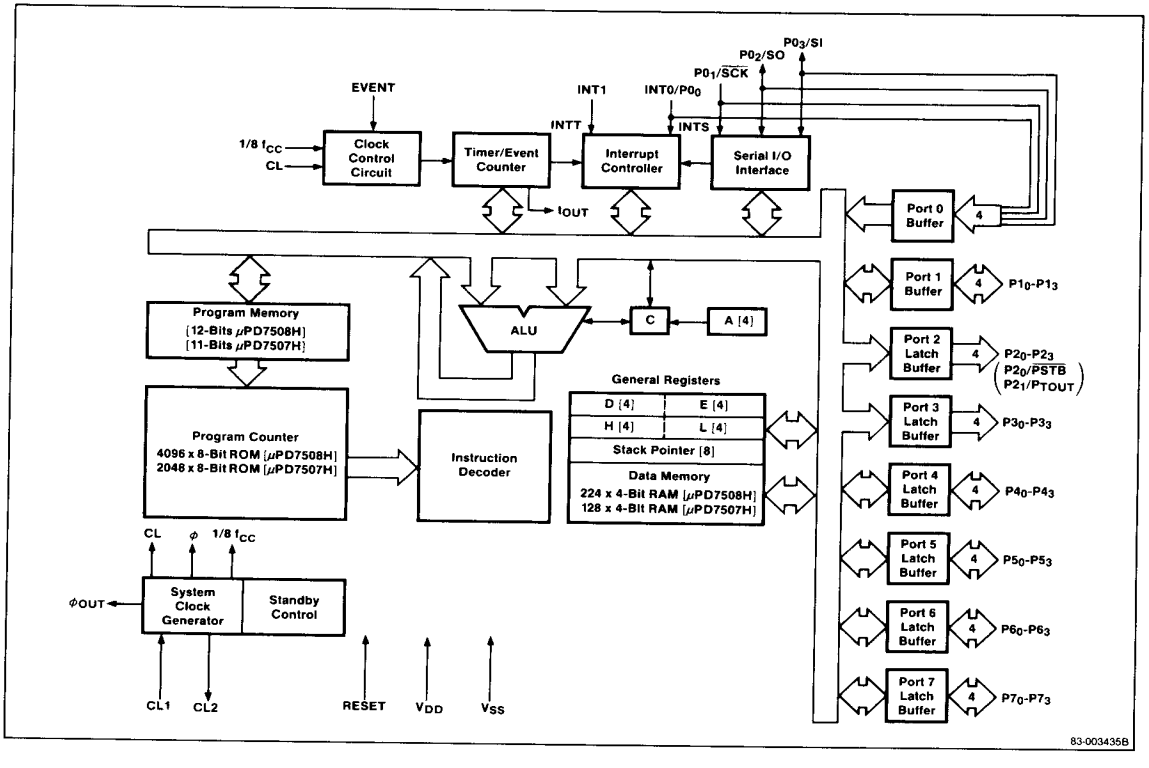
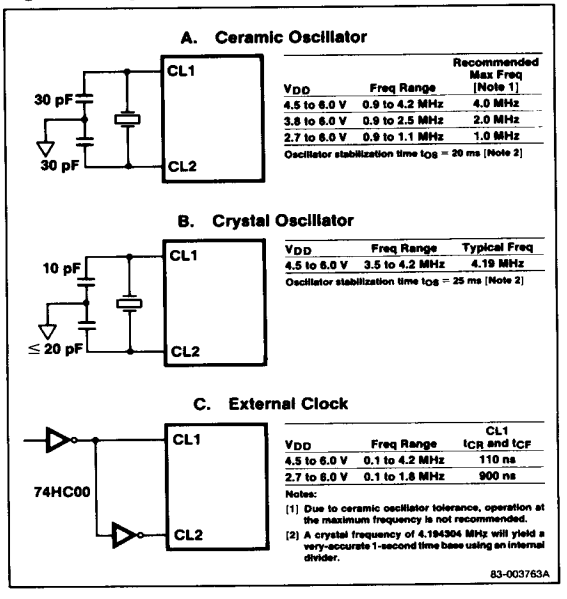


Figure 1. System Clock Options



Memory Map

Figure 2 shows the ROM program map of the 7507H/7508H.

Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM_0-CM_3), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and external EVENT input. It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter. Figure 3 shows the clock control circuit.

Table 2 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency. Bit CM_3 controls the timer out F/F; it is disabled when the bit is 0 and output when the bit is 1.

Table 2. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	$f_{CC}/1536$ (or CL/256)
0	0	1	$f_{CC}/512 = (f_{CC}/8)$ (1/64)
0	1	0	EVENT input
0	1	1	Not used
1	0	0	$f_{CC}/192$ (or CL/32)
1	0	1	$f_{CC}/64 = (f_{CC}/8)$ (1/8)
1	1	0	Not used
1	1	1	Not used

Figure 2. ROM Map

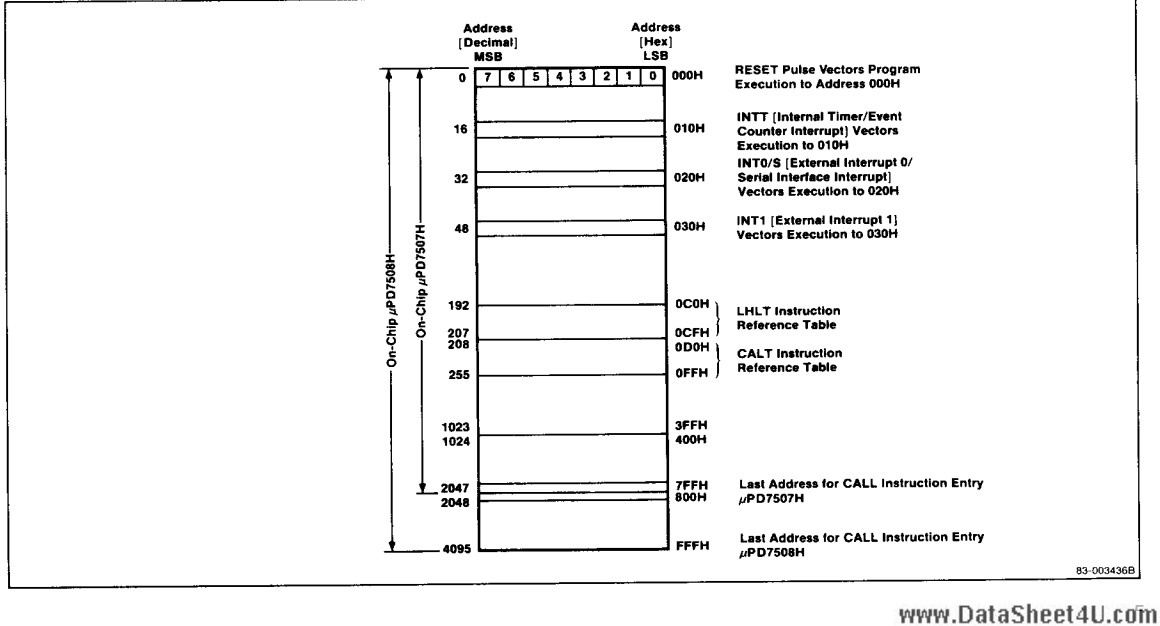
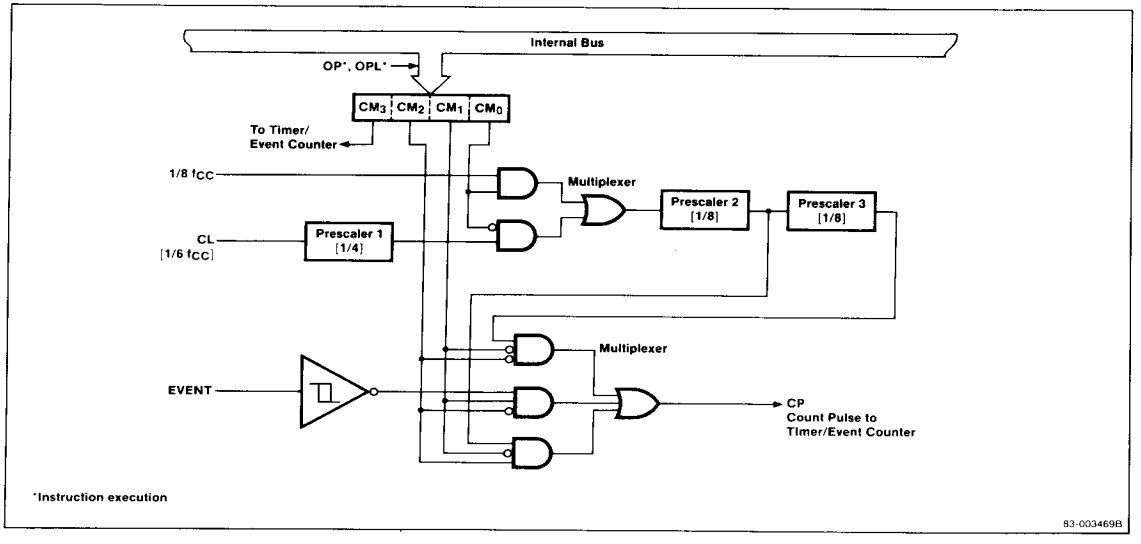


Figure 3. Clock Control Circuit



Timer/Event Counter

The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop as shown in figure 4.

The 8-bit count register is a binary 8-bit up counter, which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and the modulo register and outputs an INTT one clock pulse after they are equal.

Serial Interface

The 8-bit serial interface allows the μPD7507H/08H to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Interrupts

The μPD7507H/08H has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 3 is a summary of the four interrupts.

Table 3. μPD7507H/08H Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 4. Timer/Event Counter

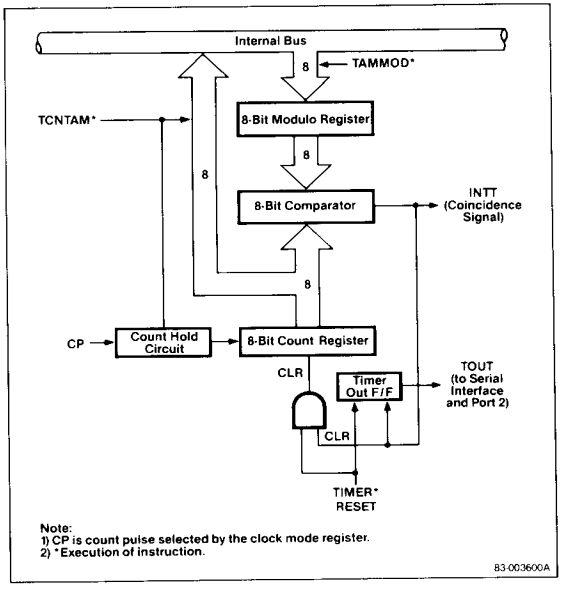
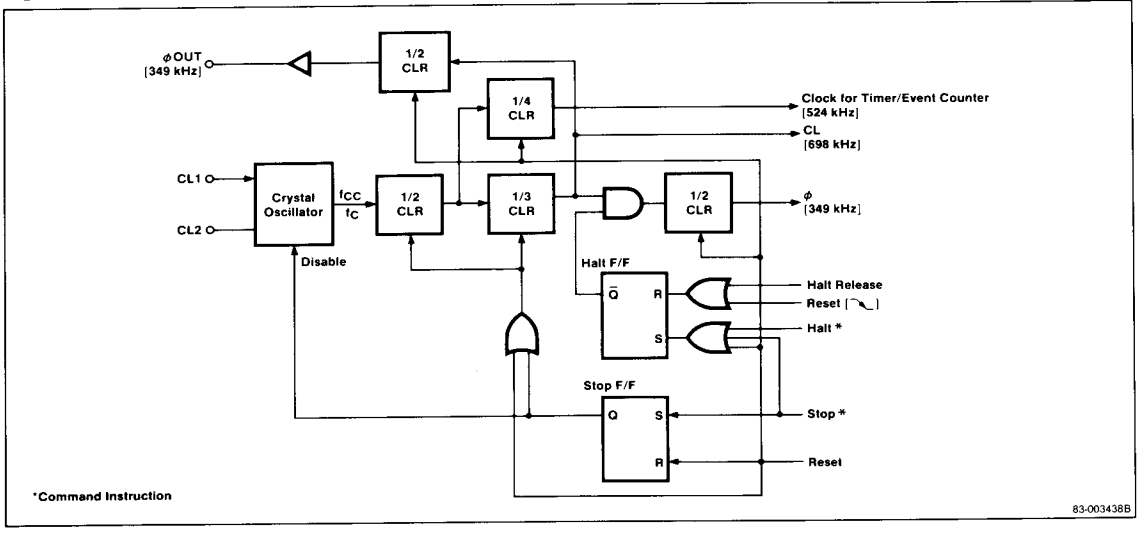


Figure 5. System Clock Circuitry



System Clock and Timing Circuitry

There are four time bases available for the μPD7507H/08H. Table 4 shows these bases and the frequencies generated.

The CPU clock is used by the CPU and serial interface. The system clock is used by the timer/event counter and the INT1 signal.

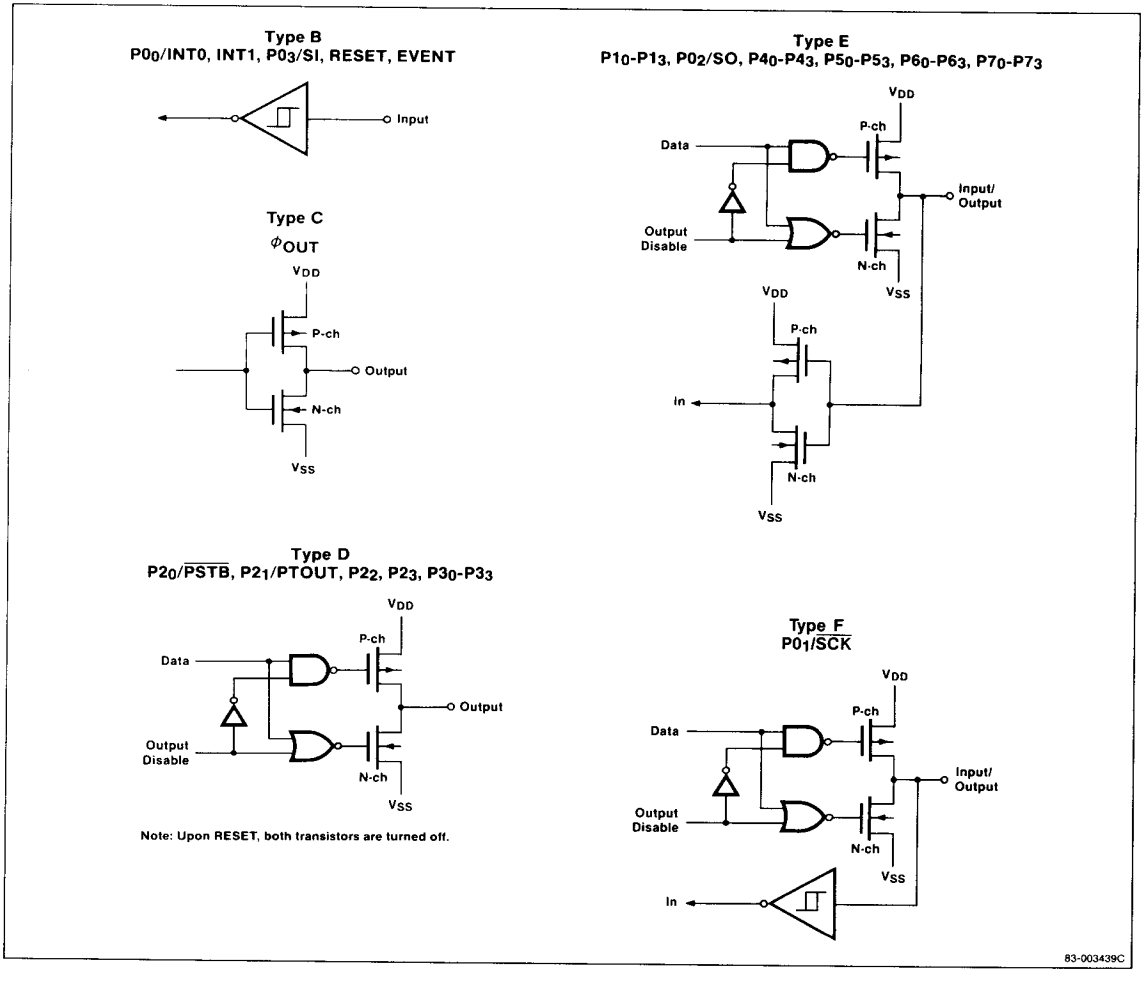
Table 4. μPD7507H/08H Time Bases

Base	Symbol	Frequency	Derivation
System clock	CL	698 kHz	$f_{CC}/6$ (4.19 MHz/6)
CPU clock	ϕ	349 kHz	$f_{CC}/12$ (4.19 MHz/12)
External clock	ϕ_{OUT}	349 kHz	$f_{CC}/12$ (4.19 MHz/12)
Timer/event counter clock	—	524 kHz	$f_{CC}/8$ (4.19 MHz/8)

I/O Port Interfaces

Figure 6 shows the internal circuit configurations at the I/O ports.

Figure 6. Interface at Input/Output Ports



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current, high, I_{OH}	
One pin	−5 mA
All pins, total	−20 mA
Output current, low, I_{OL}	
One pin	17 mA
Ports 6, 7	20 mA
Total ports	200 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = 2.7$ to 6.0 V (5 V ±10% for 75CG08HE)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, CL2
	V_{IH2}	$V_{DD} - 0.5$		V_{DD}	V	CL1, CL2
	V_{IHDR}	0.9 V_{DDDR}		$V_{DDDR} + 0.2$	V	RESET, data retention mode, μPD7507H/08H only
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, CL2
	V_{IL2}	0		0.5	V	CL1, CL2
Output voltage, high	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA; $V_{DD} = 4.5$ to 6.0 V; except A_{11}/V_{PP}, for μPD75CG08HE
		$V_{DD} - 0.5$			V	$I_{OL} = -100$ μA
		$V_{DD} - 0.75$			V	A_{11}/V_{PP}; $I_{OH} = -5$ mA (μPD75CG08HE only)
Output voltage, low	V_{OL}		0.5	1.5	V	$I_{OL} = 12$ mA; $V_{DD} = 4.5$ to 6.0 V; Ports 2-5
				0.4	V	$I_{OL} = 1.6$ mA; $V_{DD} = 4.5$ to 6.0 V; Ports 6-7
				0.5	V	$I_{OL} = 400$ μA
High level input current (MSEL)	I_{IH}	$V_{IN} = V_{DD}$		300	μA	μPD75CG08HE only
Low level input current (I_0-I_7)	I_{IL}	$V_{IN} = 0$ V		−200	μA	μPD75CG08HE only
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, CL2; $V_I = V_{DD}$
	I_{LIH2}			20	μA	CL1, CL2; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, CL2; $V_I = 0$ V
	I_{LIL2}			−20	μA	CL1, CL2; $V_I = 0$ V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode, μPD7507H/08H only
Supply current	I_{DD1}		900 (1) 1000 (2)	3000 (1) 3000 (2)	μA μA	Normal operation, $V_{DD} = 4.5$ to 6.0 V; $f_{CC} = 4.19$ MHz
			150 (2)	700 (2)	μA	Normal operation, $V_{DD} = 2.7$ to 3.3 V; $f_{CC} = 1$ MHz, μPD7507H/08H only
	I_{DD2}		350 (1) 500 (2)	800 (1) 1100 (2)	μA μA	HALT mode, X1 = 0 V; $V_{DD} = 4.5$ to 6.0 V; $f_{CC} = 4.19$ MHz
			70 (2)	180 (2)	μA	HALT mode, X1 = 0 V; $V_{DD} = 2.7$ to 3.3 V; $f_{CC} = 1$ MHz, μPD7507H/08H only
	I_{DD3}		0.1	10	μA	STOP mode, μPD7507H/08H only
			0.5	50	μA	STOP mode, μPD75CG08HE only

Note:

(1) Crystal oscillation; C1 = C2 = 10 pF.

(2) Ceramic oscillation; C1 = C2 = 30 pF.

AC Characteristics

T_A = −10 to +70°C; V_{DD} = 2.7 to 6.0 V (5 V ±10% for 75CG08HE)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
System clock period	t_{CY}	2.86		120	μs	V_{DD} = 4.5 to 5.5 V
		6.7		120	μs	
Clock high pulse width	t_{CH}					see figure 1
Clock low pulse width	t_{CL}					see figure 1
Clock rise time	t_{CR}			0.2	μs	
Clock fall time	t_{CF}			0.2	μs	
EVENT input frequency	f_E	0		700	kHz	V_{DD} = 4.5 to 6.0 V
		0		250	kHz	
EVENT input high	t_{EH}	0.7			μs	V_{DD} = 4.5 to 6.0 V
EVENT input low	t_{EL}	3.3			μs	
SCK cycle time	t_{KCY}	2.5			μs	SCK as input; V_{DD} = 4.5 to 6.0 V
		10			μs	SCK as input
		2.86			μs	SCK as output; V_{DD} = 4.5 to 6.0 V
		11			μs	SCK as output
SCK pulse width	t_{KH}, t_{KL}	1.1			μs	SCK as input; V_{DD} = 4.5 to 6.0 V
		4.5			μs	SCK as input
		1.3			μs	SCK as output; V_{DD} = 4.5 to 6.0 V
		5.0			μs	SCK as output
SI setup time to SCK ↑	t_{SIK}	300			ns	
SI hold time after SCK ↑	t_{KSI}	450			ns	
SO delay time after SCK ↓	t_{KSO}			850	ns	V_{DD} = 4.5 to 6.0 V
				1200	ns	
Port 1 output setup time to PSTB ↑	t_{PST}	(Note 1)			μs	V_{DD} = 4.5 to 6.0 V
		(Note 2)			μs	
Port 1 output hold time after PSTB ↑	t_{STP}	80			ns	
PSTB pulse width	t_{SWL}	(Note 1)			μs	V_{DD} = 4.5 to 6.0 V
		(Note 2)			μs	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1WH}, t_{I1WL}	1 (Note 3)			t_{CY}	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	μPD7507H/08H only
Clock stabilization time	t_{OS}	25			ms	After V_{DD} reaches 4.5 V

Note:

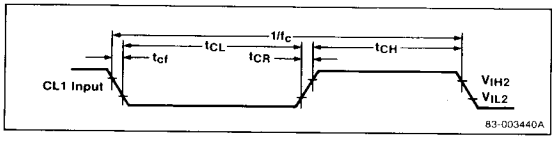
(1) $(3 \times 10^3) \div (f_{CC}$ or f_C in kHz) − 0.35 μs.

(2) $(3 \times 10^3) \div (f_{CC}$ or f_C in kHz) − 1.00 μs.

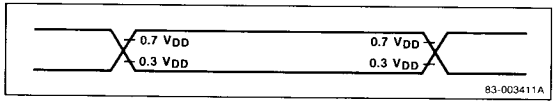
(3) $t_{CY} = 12 \div f_{CC}$ or f_C.

Timing Waveforms

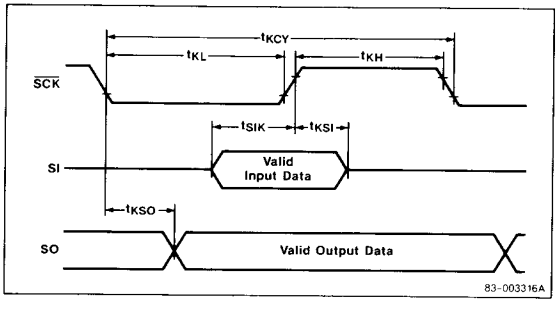
Clocks



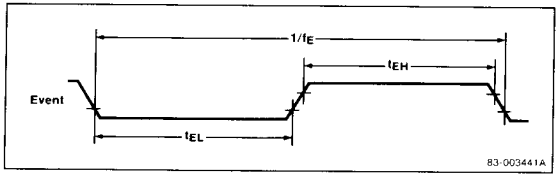
Timing Measurement Points



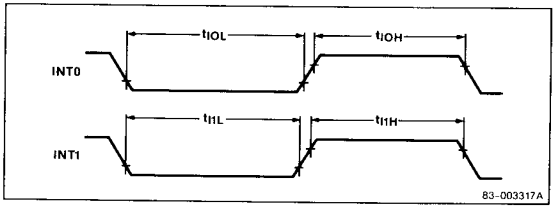
Serial Interface



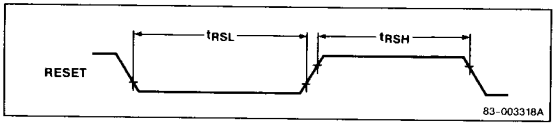
EVENT Input



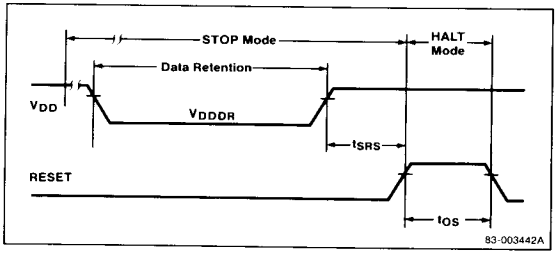
External Interrupts



Reset



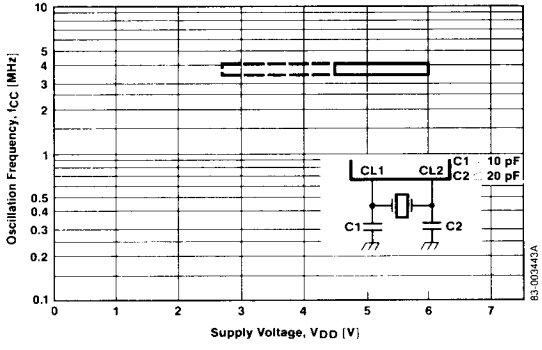
STOP Mode



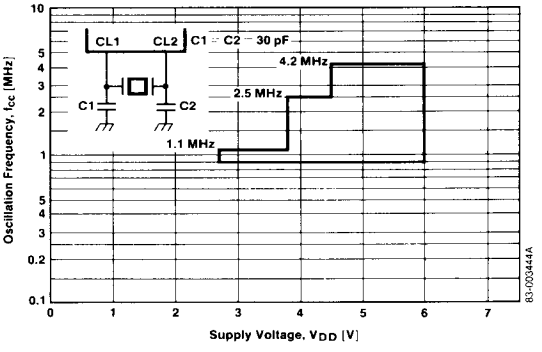
Operating Characteristics (cont)

$T_A = 25°C$

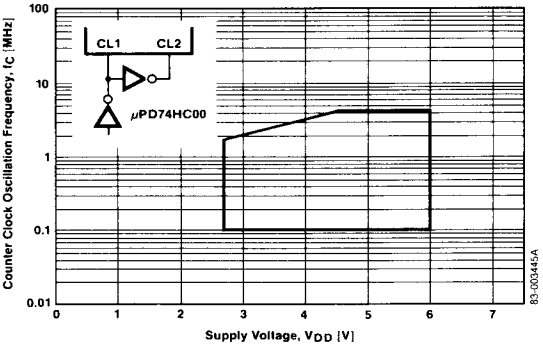
Oscillator Frequency vs Supply Voltage



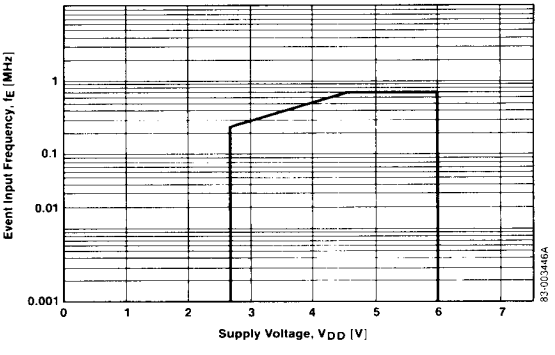
Oscillator Frequency vs Supply Voltage



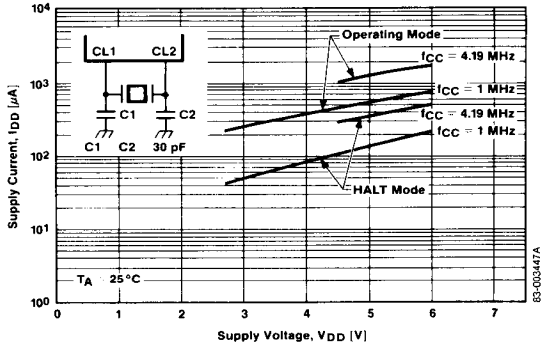
Clock Frequency vs Supply Voltage



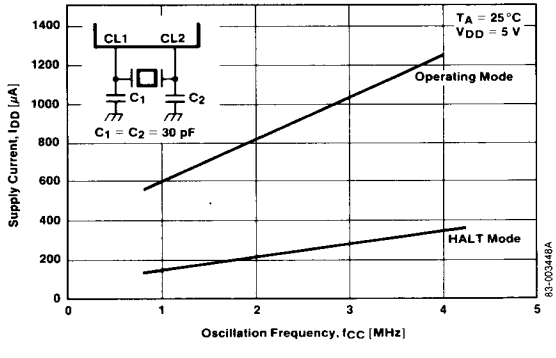
Event Frequency vs Supply Voltage



Supply Current vs Supply Voltage



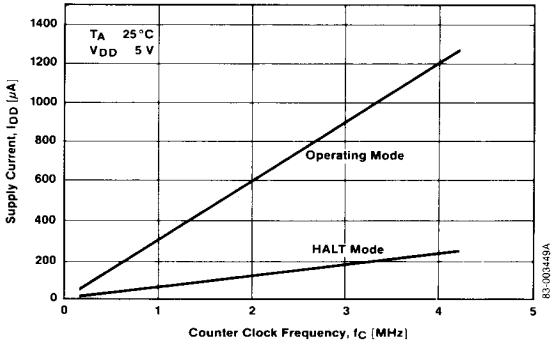
Oscillator Frequency vs Supply Voltage



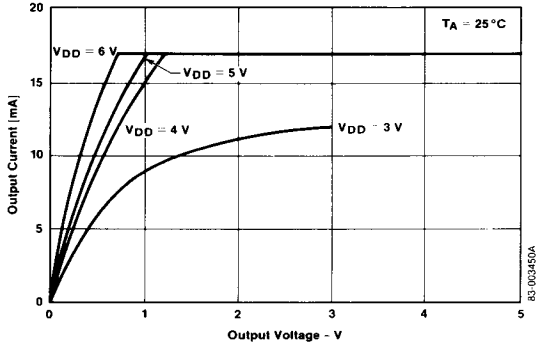
Operating Characteristics (cont)

$T_A = 25°C$

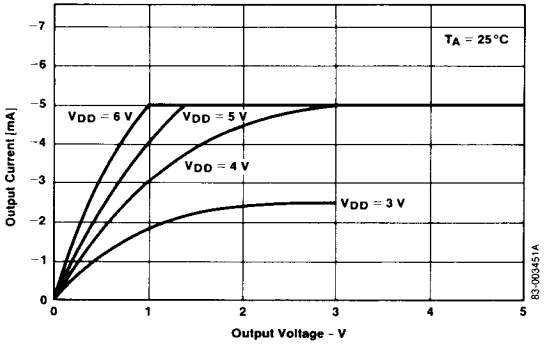
Clock Frequency vs Supply Voltage



V_{OL} vs. I_{OL} [Ports 2-7]



V_{OH} vs. I_{OH}



Packaging Information

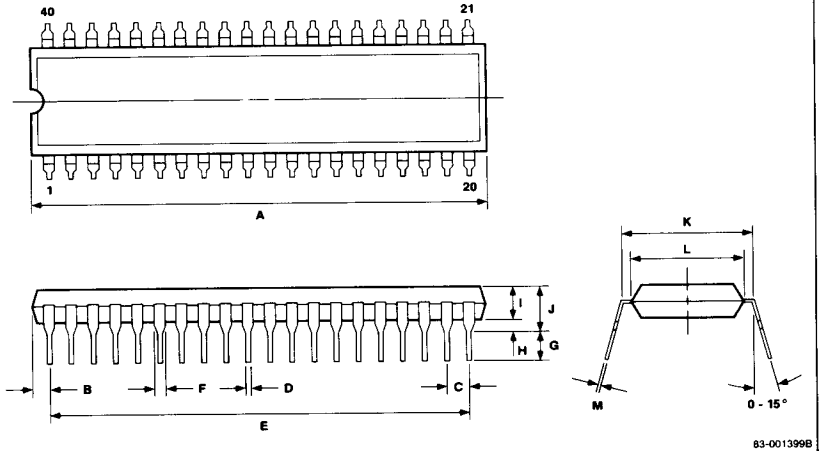
40-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	48.26	1.900
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001399B

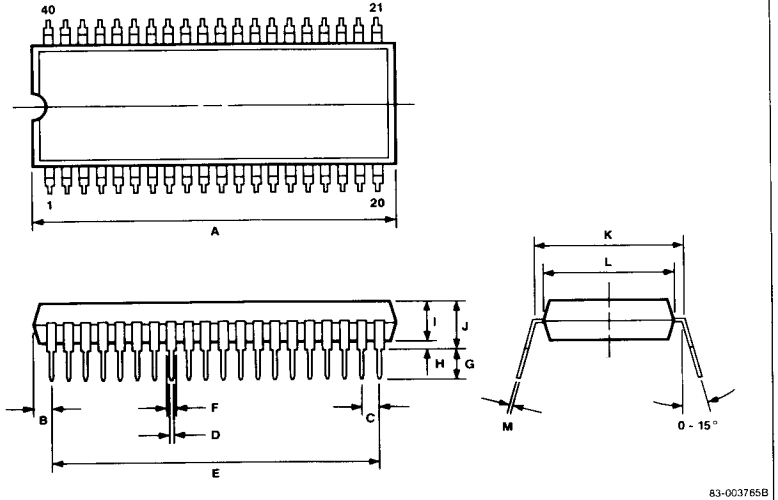
40-Pin Plastic Shrink DIP (600 mil)

Item	Millimeters	Inches
A	39.13 max	1.541 max
B	2.67 max	.106 max
C	1.778 [TP]	.070 [TP]
D	.50 ± .10	.020 ± .004
E	33.78	1.330
F	.9 min	.035 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003765B

Packaging Information (cont)

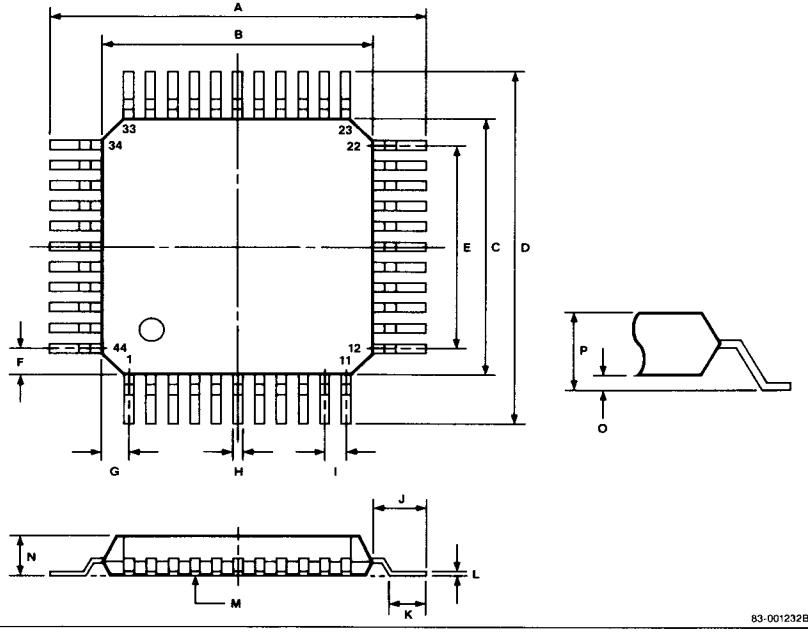
44-Pin Plastic Miniflat

Item	Millimeters	Inches
A	13.6 ±.4	.535 $^{+.017}_{-.016}$
B	10 ±.2	.394 $^{+.008}_{-.009}$
C	10 ±.2	.394 $^{+.008}_{-.009}$
D	13.6 ±.4	.535 $^{+.017}_{-.018}$
E	8.0	.315
F	1.0	.039
G	1.0	.039
H	.35 $^{+.20}_{-.10}$	.014 $^{+.006}_{-.005}$
I	.8 [TP] Note 1	.031 [TP]
J	1.8 ±.2	.071 $^{+.008}_{-.009}$
K	1.0 ±.2	.039 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	1.45 ±.1	.057 $^{+.005}_{-.004}$
O	0.0 ±.1	0.000 ±.004
P	1.85 max	.065 max

Note:

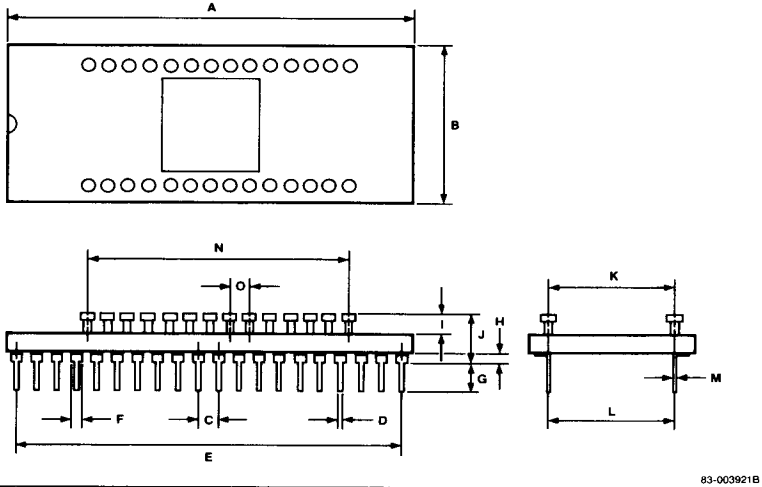
[1] Each lead centerline is located within .15 mm [.006 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



40-Pin Ceramic Piggyback DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.1 max
B	20.32	.8
C	2.54 ± .25	.1 ± .01
D	0.46 ± .05	.018 ± .002
E	48.26	1.9
F	1.02	.04
G	3.2 min	.126 min
H	1.02 min	.04 min
I	3.0 max	.118 max
J	4.32 max	.17 max
K	15.24	.6
L	15.24	.6
M	.25 ± .05	.01 ± .002
N	33.02	1.3
O	2.54 ± .25	.1 ± .01



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