PC Card Controller compliant with PCMCIA 2.1/JEIDA 4.2

RF5C296/RF5C396L/RB5C396/RF5C396

APPLICATION MANUAL

RICOH

ELECTRONIC DEVICES DIVISION

NO.EA-028-9804

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June 1995

RF5C296/RF5C396L/RB5C396/RF5C396

APPLICATION MANUAL

CONTENTS

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COMPLIANT WITH PCMCA2.1/JEIDA4.2 PC CARD CONTROLLER

RF5C296/RF5C396L/RB5C396/RF5C396

OUTLINE

The RF5C296, the RF5C396L, the RB5C396, and the RF5C396 are enhanced version of the RF5C266 and RF5C366, LSIs functioning as controllers for interfacing IC memory cards, modems, and I/O cards, such as HDDs, to system buses in compliance with the PCMCIA2.1 or JEIDA4.2 Standard. These controller LSIs can be used to configure an ISA bus system which supports PC cards.

The RF5C296 supports one PC card slot while the RF5C396L, the RB5C396 and the RF5C396 support two PC card slots. Incorporating a buffer and a transceiver, each of these devices can be directly coupled to the ISA system bus and the PC card slots. The devices are also capable of providing an independent power supply of 3.3V or 5V for each slot interface, system bus, and core logic. Further, they effect substantial space savings through implementation in slimline packages (i.e. the 144pin LQFP for the RF5C296, the 208pin LQFP for the RF5C396L, the 256pin PBGA for the RB5C396 and the 208pin QFP for the RF5C396).

Unless otherwise noted, the RF5C396L, the RB5C396 and the RF5C396 are collectively referred to as the RF5C396 in this manual.

FEATURES

- Enhanced version of RF5C266/RF5C366
  - · DMA mode support
  - · Enhanced power management
  - · INPACK# pin support
  - · Available in thin (t=1.5mm) LQFP and PBGA
- Compliant with PCMCIA2.1/JEIDA4.2
- i82365SL B_Step compatible register set
- Direct connection to PCMCIA2.1/JEID4.2 PC Card slot
- Easy host interface using ISA I/O addresses 3E0h, 3E1h
- Direct connection to ISA Bus
- Programmable IRQs to level mode or edge trigger mode
- Enhanced Power Management based on socket and window inactivity
- PCMCIA-AT-A Disk interface support
- 8bit cycles follow SBHE# independent of programmed window size
- 5 programmable memory windows per slot
- 2 programmable I/O windows per slot
- 3.3V & 5V Mixed Voltage Operation
- DMA mode Support

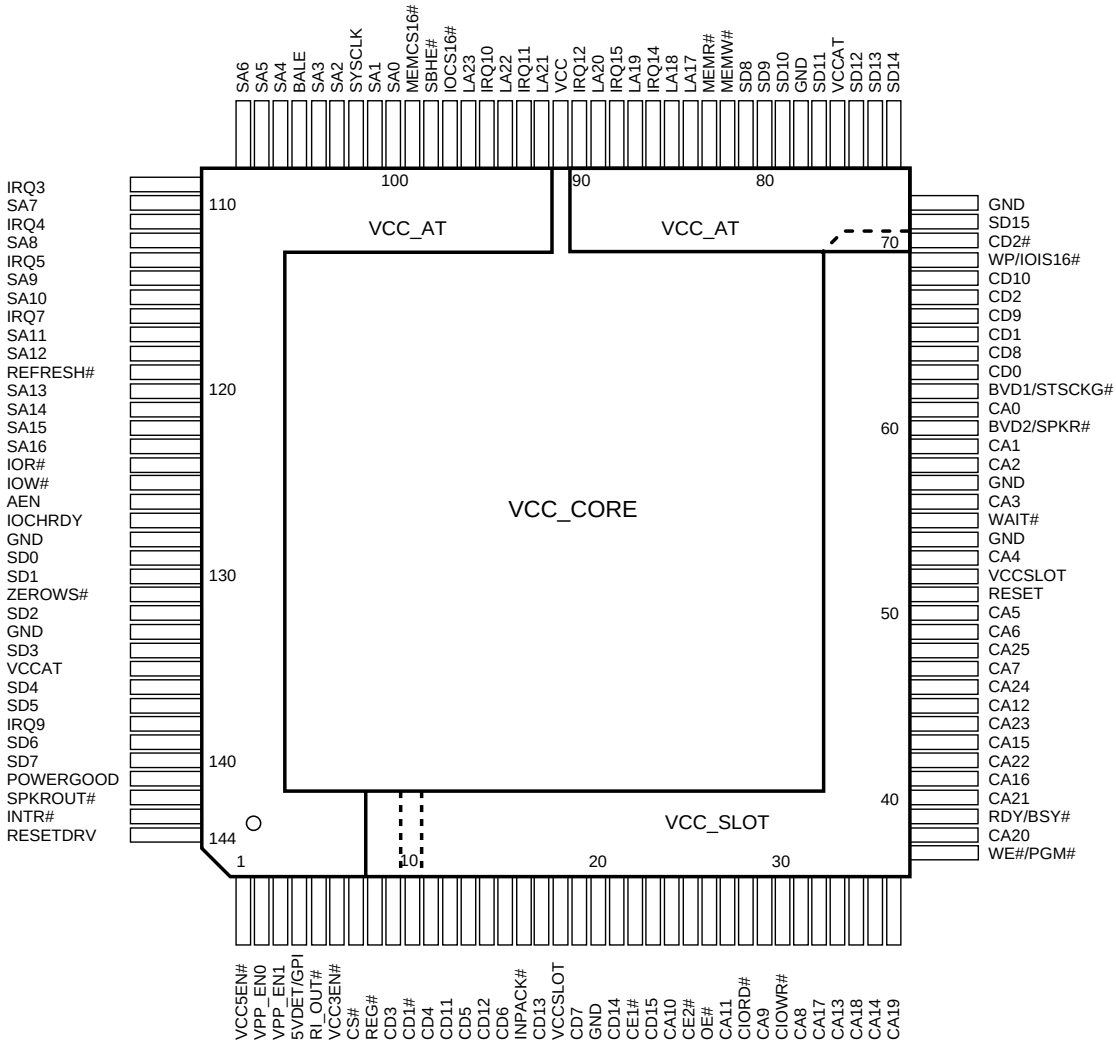
- PACKAGES
  - · RF5C296 144pin LQFP (t=1.7mm)
  - · RF5C396L 208pin LQFP (t=1.7mm)
  - · RB5C396 256pin PBGA (23 × 23)
  - · RF5C396 208pin QFP

APPLICATIONS

- PC (Notebook Type, Pen-based Type and Palm Top Type)
- Docking Station
- PDA
- Handy Terminal

PIN CONFIGURATION

• RF5C296 Pin Assignments (Top View)



*) CD1# and CD2# are powered by VCC_AT

PIN ASSIGNMENTS

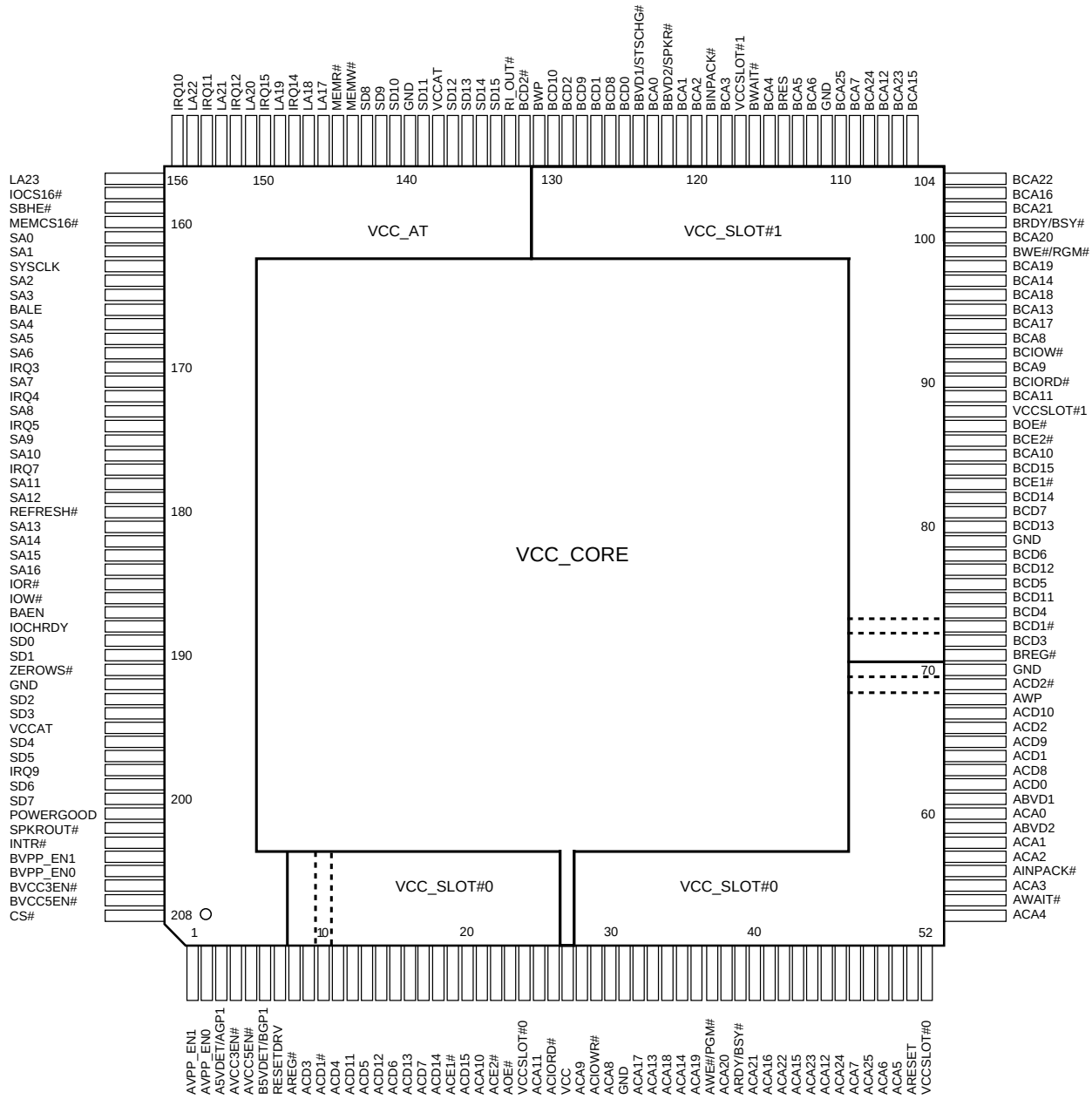
• RF5C296

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VCC5EN#	37	WE#/PGM#	73	SD14	109	IRQ3
2	VPP_EN0	38	CA20	74	SD13	110	SA7
3	VPP_EN1	39	RDY/BSY#	75	SD12	111	IRQ4
4	5VDET/GPI	40	CA21	76	VCCAT	112	SA8
5	RIOUT#	41	CA16	77	SD11	113	IRQ5
6	VCC3EN#	42	CA22	78	GND	114	SA9
7	CS#	43	CA15	79	**SD10**	115	SA10
8	REG#	44	CA23	80	SD9	116	IRQ7
9	CD3	45	CA12	81	SD8	117	SA11
10	CD1#	46	CA24	82	MEMW#	118	SA12
11	CD4	47	CA7	83	MEMR#	119	REFRESH#
12	CD11	48	CA25	84	LA17	120	SA13
13	CD5	49	CA6	85	LA18	121	SA14
14	CD12	50	CA5	86	IRQ14	122	SA15
15	CD6	51	RESET	87	LA19	123	SA16
16	INPACK#	52	VCCSLOT	88	IRQ15	124	IOR#
17	CD13	53	CA4	89	LA20	125	IOW#
18	VCCSLOT	54	GND	90	IRQ12	126	AEN
19	CD7	55	WAIT#	91	VCC	127	IOCHRDY
20	GND	56	CA3	92	LA21	128	GND
21	CD14	57	GND	93	IRQ11	129	SD0
22	CE1#	58	CA2	94	LA22	130	SD1
23	CD15	59	CA1	95	IRQ10	131	ZEROWS#
24	CA10	60	BVD2/SPKR#	96	LA23	132	SD2
25	CE2#	61	CA0	97	IOCS16#	133	GND
26	OE#	62	BVD1/STSCHG#	98	SBHE#	134	SD3
27	CA11	63	CD0	99	MEMCS16#	135	VCCAT
28	CIORD#	64	CD8	100	SA0	136	SD4
29	CA9	65	CD1	101	SA1	137	SD5
30	CIOWR#	66	CD9	102	SYSCLK	138	IRQ9
31	CA8	67	CD2	103	SA2	139	SD6
32	CA17	68	CD10	104	SA3	140	SD7
33	CA13	69	WP/IOIS16#	105	BALE	141	POWERGOOD
34	CA18	70	CD2#	106	SA4	142	SPKROUT#
35	CA14	71	SD15	107	SA5	143	INTR#
36	CA19	72	GND	108	SA6	144	RESETDRV

*) I : Active “low” signals are indicated by “#”.

PIN CONFIGURATION

• RF5C396L/RF5C396



∗) ACD1# ,ACD2# ,BCD1#,BCD2# are powered by VCC_AT

PIN ASSIGNMENTS

• RF5C396L/RF5C396

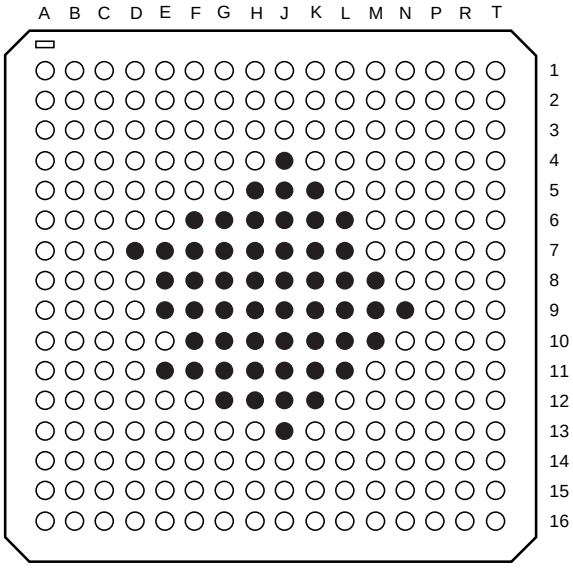
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	AVPP_EN1	37	AWE#/PGM#	73	BCD1#	109	BCA7
2	AVPP_EN0	38	ACA20	74	BCD4	110	BCA25
3	A5VDET/AGPI	39	ARDY/BSY#	75	BCD11	111	GND
4	AVCC3EN#	40	ACA21	76	BCD5	112	BCA6
5	AVCC5EN#	41	ACA16	77	BCD12	113	BCA5
6	B5VDET/BGPI	42	ACA22	78	BCD6	114	BRESET
7	RESETDRV	43	ACA15	79	GND	115	BCA4
8	AREG#	44	ACA23	80	BCD13	116	BWAIT#
9	ACD3	45	ACA12	81	BCD7	117	VCCSLOT#1
10	ACD1#	46	ACA24	82	BCD14	118	BCA3
11	ACD4	47	ACA7	83	BCE1#	119	BINPACK#
12	ACD11	48	ACA25	84	BCD15	120	BCA2
13	ACD5	49	ACA6	85	BCA10	121	BCA1
14	ACD12	50	ACA5	86	BCE2#	122	BBVD2/SPKR#
15	ACD6	51	ARESET	87	BOE#	123	BCA0
16	ACD13	52	VCCSLOT#0	88	VCCSLOT#1	124	BBVD1/STSCHG#
17	ACD7	53	ACA4	89	BCA11	125	BCD0
18	ACD14	54	AWAIT#	90	BCIORD#	126	BCD8
19	ACE1#	55	ACA3	91	BCA9	127	BCD1
20	ACD15	56	AINPACK#	92	BCIOWR#	128	BCD9
21	ACA10	57	ACA2	93	BCA8	129	BCD2
22	ACE2#	58	ACA1	94	BCA17	130	BCD10
23	AOE#	59	ABVD2/SPKR#	95	BCA13	131	BWP/IOIS16#
24	VCCSLOT#0	60	ACA0	96	BCA18	132	BCD2#
25	ACA11	61	ABVD1/STSCHG#	97	BCA14	133	RIOUT#
26	ACIORD#	62	ACD0	98	BCA19	134	SD15
27	VCC	63	ACD8	99	BWE#/PGM#	135	SD14
28	ACA9	64	ACD1	100	BCA20	136	SD13
29	ACIOWR#	65	ACD9	101	BRDY/BSY#	137	SD12
30	ACA8	66	ACD2	102	BCA21	138	VCCAT
31	GND	67	ACD10	103	BCA16	139	SD11
32	ACA17	68	AWP/IOIS16#	104	BCA22	140	GND
33	ACA13	69	ACD2#	105	BCA15	141	SD10
34	ACA18	70	GND	106	BCA23	142	SD9
35	ACA14	71	BREG#	107	BCA12	143	SD8
36	ACA19	72	BCD3	108	BCA24	144	MEMW#

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
145	MEMR#	161	SA0	177	IRQ7	193	SD2
146	LA17	162	SA1	178	SA11	194	SD3
147	LA18	163	SYSCLK	179	SA12	195	VCCAT
148	IRQ14	164	SA2	180	REFRESH#	196	SD4
149	SA19	165	SA3	181	SA13	197	SD5
150	IRQ15	166	BALE	182	SA14	198	IRQ9
151	LA20	167	SA4	183	SA15	199	SD6
152	IRQ12	168	SA5	184	SA16	200	SD7
153	LA21	169	SA6	185	IOR#	201	POWERGOOD
154	IRQ11	170	IRQ3	186	IOW#	202	SPKROUT#
155	LA22	171	SA7	187	AEN	203	INTR#
156	IRQ10	172	IRQ4	188	IOCHRDY	204	BVPP_EN1
157	LA23	173	SA8	189	SD0	205	BVPP_EN0
158	IOCS16#	174	IRQ5	190	SD1	206	BVCC3EN#
159	SBHE#	175	SA9	191	ZEROWS#	207	BVCC5EN#
160	MEMCS16#	176	SA10	192	GND	208	CS#

*) I : Active “low” signals are indicated by “#”.

PIN CONFIGURATION

• RB5C396



PIN ASSIGNMENTS

• RB5C396

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
A1	LA22	B1	IOCS16#	C1	SYSCLK	D1	BALE
A2	LA21	B2	IRQ11	C2	SA2	D2	SA5
A3	LA19	B3	IRQ12	C3	SBHE#	D3	MEMCS16#
A4	LA17	B4	IRQ14	C4	IRQ15	D4	SA1
A5	SD8	B5	MEMR#	C5	LA18	D5	IRQ10
A6	SD11	B6	SD9	C6	SD10	D6	MEMW#
A7	SD14	B7	SD12	C7	SD13	D7	GND
A8	BCD2#	B8	SD15	C8	RIOUT#	D8	VCCAT
A9	BCD9	B9	BCD2	C9	BWP/IOIS16#	D9	BCD10
A10	BCD0	B10	BCD8	C10	BCD1	D10	BCA0
A11	BCA1	B11	BBVD2/SPKR#	C11	BBVD1/STSCHG#	D11	BCA2
A12	BCA3	B12	BINPACK#	C12	BWAIT#	D12	BCA5
A13	BRESET	B13	BCA4	C13	BCA24	D13	BCA7
A14	BCA25	B14	BCA6	C14	BCA12	D14	BCA19
A15	BCA23	B15	BCA21	C15	BCA20	D15	BCA18
A16	BCA16	B16	BRDY/BSY#	C16	BCA14	D16	BCA17

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
E1	IRQ3	G1	IRQ7	J1	SA16	L1	SD1
E2	SA7	G2	SA11	J2	IOW#	L2	SD2
E3	SA6	G3	SA12	J3	IOR#	L3	ZEROWS#
E4	SA3	G4	SA9	J4	GND	L4	SD4
E5	LA23	G5	SA4	J5	GND	L5	INTR#
E6	LA20	G6	GND	J6	GND	L6	GND
E7	GND	G7	GND	J7	GND	L7	GND
E8	GND	G8	GND	J8	GND	L8	GND
E9	GND	G9	GND	J9	GND	L9	GND
E10	VCCSLOT#1	G10	GND	J10	GND	L10	GND
E11	GND	G11	GND	J11	GND	L11	GND
E12	BCA15	G12	GND	J12	GND	L12	ACA2
E13	BCA22	G13	BCIOWR#	J13	GND	L13	AWP/IOIS16#
E14	BCA13	G14	BCD15	J14	BCD6	L14	BCD3
E15	BCA8	G15	BCD10	J15	BCD12	L15	BREG#
E16	BCIORD#	G16	BCE1#	J16	BCD5	L16	ACD2#
F1	SA8	H1	REFRESH#	K1	AEN	M1	SD3
F2	IRQ5	H2	SA13	K2	SD0	M2	SD5
F3	SA10	H3	SA15	K3	IOCHRDY	M3	SD6
F4	IRQ4	H4	SA14	K4	VCCAT	M4	CS#
F5	SA0	H5	GND	K5	GND	M5	AVPP_EN1
F6	GND	H6	GND	K6	GND	M6	AVCC5EN#
F7	GND	H7	GND	K7	GND	M7	ACD4
F8	GND	H8	GND	K8	GND	M8	GND
F9	GND	H9	GND	K9	GND	M9	GND
F10	GND	H10	GND	K10	GND	M10	GND
F11	GND	H11	GND	K11	GND	M11	ACA7
F12	BWE#	H12	GND	K12	GND	M12	ACA4
F13	BCA9	H13	VCCSLOT#1	K13	ACD8	M13	ABVD1/STSCHG#
F14	BOE#	H14	BCD7	K14	BCD11	M14	ACD9
F15	BCA11	H15	BCD14	K15	BCD4	M15	ACD10
F16	BCE2#	H16	BCD13	K16	BCD1#	M16	ACD2

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
N1	IRQ9	P1	POWERGOOD	R1	BVPP_EN0	T1	BVCC5EN#
N2	SD7	P2	BVPP_EN1	R2	BVCC3EN#	T2	AVPP_EN0
N3	SPKROUT#	P3	A5VDET/AGPI	R3	AREG#	T3	RESETDRV
N4	B5VDET/BGPI	P4	AVCC3EN#	R4	ACD11	T4	ACD1#
N5	ACD3	P5	ACD5	R5	ACD6	T5	ACD12
N6	ACD13	P6	ACE1#	R6	ACD14	T6	ACD7
N7	VCCSLOT#0	P7	ACE2#	R7	ACA10	T7	ACD15
N8	VCC	P8	ACIORD#	R8	ACA11	T8	AOE#
N9	GND	P9	ACIOWR#	R9	ACA8	T9	ACA9
N10	ACA21	P10	ACA13	R10	ACA18	T10	ACA17
N11	ARDY/BSY#	P11	ACA19	R11	AWE#	T11	ACA14
N12	VCCSLOT#0	P12	ACA15	R12	ACA16	T12	ACA20
N13	ACA1	P13	ACA24	R13	ACA23	T13	ACA22
N14	AINPACK#	P14	ACA3	R14	ACA25	T14	ACA12
N15	ACD1	P15	ACA0	R15	ACA5	T15	ACA6
N16	ACD0	P16	ABVD2/SPKR#	R16	AWAIT#	T16	ARESET

PIN DESCRIPTION

1. ISA Bus Interface

Symbol	Function	Pin No.		I/O*	Drive
		RF5C296	RF5C396*1		
LA23 to LA17	ISA Bus System Address 23 to 17	96,94,92,89,87,85, 84	157,155,153,151, 149,147,146	I	—
SA16 to SA0	ISA Bus System Address 16 to 0	123,122,121,120, 118,117,115,114, 112,110,108,107, 106,104,103,101, 100	184,183,182,181, 179,178,176,175, 173,171,169,168, 167,165,164,162, 161	I	—
AEN	Address Enable. High signal is input in DMA mode.	126	187	I	—
BALE	Address Latch Enable. This signal latches LA23 pin to LA17 pin.	105	166	I	—
SBHE#	System Bus High Byte Enable	98	159	I	—
REFRESH#	This active low signal indicates that an ISA-bus refresh cycle is either requested or in progress.	119	180	I	—
SD15 to SD0	System Data Bus	71,73,74,75,77,79, 80,81,140,139, 137,136,134,132, 130,129	134,135,136,137, 139,141,142,143, 200,199,197,196, 194,193,190,189	I/O	12mA
IOR#	I/O Port Read	124	185	I	—
IOW#	I/O Port Write	125	186	I	—
MEMR#	Memory Read	83	145	I	—
MEMW#	Memory Write	82	144	I	—
IOCS16#	16bit I/O Transfer Mode Chip Select	97	158	O (OD)	16mA
MEMCS16#	16bit Memory Transfer Mode Chip Select	99	160	O (OD)	16mA
ZEROWS#	Zero Wait State	131	191	O (TS)	12mA
IOCHRDY	I/O Channel Ready. This active High signal indicates that the accessed device on the ISA-bus is ready to terminate the bus cycle.	127	188	O (TS)	16mA
IRQn	Interrupt Request Signal. IRQ3, IRQ4, IRQ5, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15. Level mode interrupt or Edge mode interrupt is programmable. IRQ12 can be used as a LED driver. IRQ9, IRQ10, IRQ11, or IRQ15 may be used as system side DACK#, system side DREQ, and system side TC respectively in DMA mode.	109,111,113,116, 138,95,93,90,86, 88	170,172,174,177, 198,156,154,152, 148,150	O (TS)	8mA

*) I : Input, O : Output, I/O : Input/Output, O (OD) : Open Drain Output, O (TS) : Tri-State Output.
*1) Pin No. of the RB5C396 differ from those of others. Refer to “PIN CONFIGURATION”.

Symbol	Function	Pin No.		I/O*	Drive
		RF5C296	RF5C396*1		
SYSCLK	System Clock Input	102	163	I	—
CS#	Chip Select input. This signal is use for configuration CS# control power down mode, in case of driving by the I/O address.	7	208	I	—

*) I : Input, O : Output, I/O : Input/Output, O (OD) : Open Drain Output, O (TS) : Tri-State Output.
*1) Pin No. of the RB5C396 differ from those of others. Refer to “PIN CONFIGURATION”.

2. Card Slot Interface

Symbol	Function	Pin No.		I/O*1	Drive
		RF5C296	RF5C396*2		
CA25 to CA0	Card Address Output	48,46,44,42,40,38,36,34,32,41,43,35,33,45,27,24,29,31,47,49,50,53,56,58,59,61	Slot#0 : 48,46,44,42,40,38,36,34,32,41,43,35,33,45,25,21,28,30,47,49,50,53,55,57,58,60 Slot#1 : 110,108,106,104,102,100,98,96,94,103,105,97,95,107,89,85,91,93,109,112,113,115,118,120,121,123	O (TS)	8mA
CD15 to CD8	Card Data Bus High Byte. Input buffer is disabled when card slot power supply is off or card is not inserted.	23,21,17,14,12,68,66,64	Slot#0 : 20,18,16,14,12,67,65,63 Slot#1 : 84,82,80,77,75,130,128,126	I/O (PD)	8mA
CD7 to CD0	Card Data Bus Low Byte. Input buffer is disabled when card slot power supply is off or card is not inserted.	19,15,13,11,9,67,65,63	Slot#0 : 17,15,13,11,9,66,64,62 Slot#1 : 81,78,76,74,72,129,127,125	I/O (PD)	8mA
CE2#	Card Enable High Byte	25	Slot#0 : 22 Slot#1 : 86	O (TS)	8mA
CE1#	Card Enable Low Byte	22	Slot#0 : 19 Slot#1 : 83	O (TS)	8mA
CIORD#	Card I/O Read	28	Slot#0 : 26 Slot#1 : 90	O (TS)	8mA
CIOWR#	Card I/O Write	30	Slot#0 : 29 Slot#1 : 92	O (TS)	8mA
OE#	Card Output Enable	26	Slot#0 : 23 Slot#1 : 87	O (TS)	8mA
WE#/PGM#	Card Write Enable/Program	37	Slot#0 : 37 Slot#1 : 99	O (TS)	8mA
BVD1 (STSCHG# /RI#)	The battery voltage detect input 1 on the memory PC card, and Card Status Change#/Ring indicate# input on the I/O card.	62	Slot#0 : 61 Slot#1 : 124	I	—
BVD2 (SPKR#)	The battery voltage detect input 2 on the memory PC card, and SPEAKER# (Digital Audio) input on the I/O card. This pin may also be used as card side DREQ in DMA mode.	60	Slot#0 : 59 Slot#1 : 122	I	—

*1) I : Input, O : Output, I/O : Input/Output, I/O (PD) : Input/Output with Pull-down Register, O (TS) : Tri-State Output.
*2) All card slot interface signal names are pretended with A-(slot#0) and B-(slot#1).
For example, ACA25 to ACA0 are the card address buses to the slot#0.
Pin No. of the RB5C396 differ from those of others. Refer to "PIN CONFIGURATION".

Symbol	Function	Pin No.		I/O*1	Drive
		RF5C296	RF5C396*2		
CD1#, CD2#	Card Detect Input 1 & 2*3	10,70	Slot#0 : 10,69 Slot#1 : 73,132	I	—
RDY/BSY# (IREQ#)	READY/BUSY# input on the memory PC card, and IREQ# input on the I/O card.	39	Slot#0 : 39 Slot#1 : 101	I	—
REG#	When this signal is "L" memory access is limited to Attribute memory. During normal access for I/O, this signal must be kept "L". During DMA cycle, this signal must be kept "H". This pin may also be used as card side DACK in DMA mode.	8	Slot#0 : 8 Slot#1 : 71	O(TS)	4mA
WAIT#	Bus Cycle Wait Input from PC Card	55	Slot#0 : 54 Slot#1 : 116	I	—
WP (IOIS16#)	Write Protect switch input on the memory PC card and, IOIS16# is asserted by PC card when the I/O cycle is 16bit on the I/O. This pin may also be used as card side DREQ in DMA mode.	69	Slot#0 : 68 Slot#1 : 131	I	—
RESET	Card Reset Output	51	Slot#0 : 51 Slot#1 : 114	O(TS)	4mA
INPACK#	Input Acknowledge. "L" is output to INPACK# on the PCMCIA bus only when I/O ports accessed during I/O signal read are enabled on PC cards that support this signal. When INPACK# signal is enabled for RF5C296/RF5C396, I/O signal read data will be output to the system only when the INPACK# signal is enabled. This pin may also be used as card side DREQ in DMA mode.	16	Slot#0 : 56 Slot#1 : 119	I	—

*1) I : Input, O : Output, I/O : Input/Output, O (TS) : Tri-State Output.
*2) All card slot interface signal names are pretended with A-(slot#0) and B-(slot#1).
For example, ACA25 to ACA0 are the card address buses to the slot #0.
Pin No. of the RB5C396 differ from those of others. Refer to "PIN CONFIGURATION".
*3) CD1# and CD2# are powered by VCC_AT instead of VCC_SLOT because hot plug-in/out is supported during card slot power is off.

3. Other Control Pins

Symbol	Function	Pin No.		I/O*1	Drive
		RF5C296	RF5C396*2		
POWERGOOD	POWERGOOD input. Connect to GND if not used.	141	201	I	—
RESETDRV	Reset Drive Input. This active High signal indicates Main System Cold Reset.	144	7	I (PD)	—
SPKROUT#	Speaker Output. Passes through SPKR# from an I/O card.	142	202	O (TS)*3	4mA
RI_OUT#	Ring Indicate Output. Passes through RI_OUT# from an I/O card.	5	133	O (TS)*3	4mA
INTR#	Interrupt Request Output	143	203	O (TS)*3	4mA
5VDET/GPI	5V detect input/General Purpose Input, on GPI enable. IRQ generation is programmable when transition occurs. Basically user can use this input arbitrarily. This pin shall be connected to the VSI# in the card slot for use as 5V Detect Input.	4	Slot#0 : 3 Slot#1 : 6	I (PU)	—
VCC5EN#	Power Control (5V)	1	Slot#0 : 5 Slot#1 : 207	O	4mA
VCC3EN#	Power Control (3.3V)	6	Slot#0 : 4 Slot#1 : 206	O	4mA
VPP_EN0	Program Power Supply Control 0 (VPP_VCC)	2	Slot#0 : 2 Slot#1 : 205	O	4mA
VPP_EN1	Program Power Supply Control 1 (VPP_PGM)	3	Slot#0 : 1 Slot#1 : 204	O	4mA

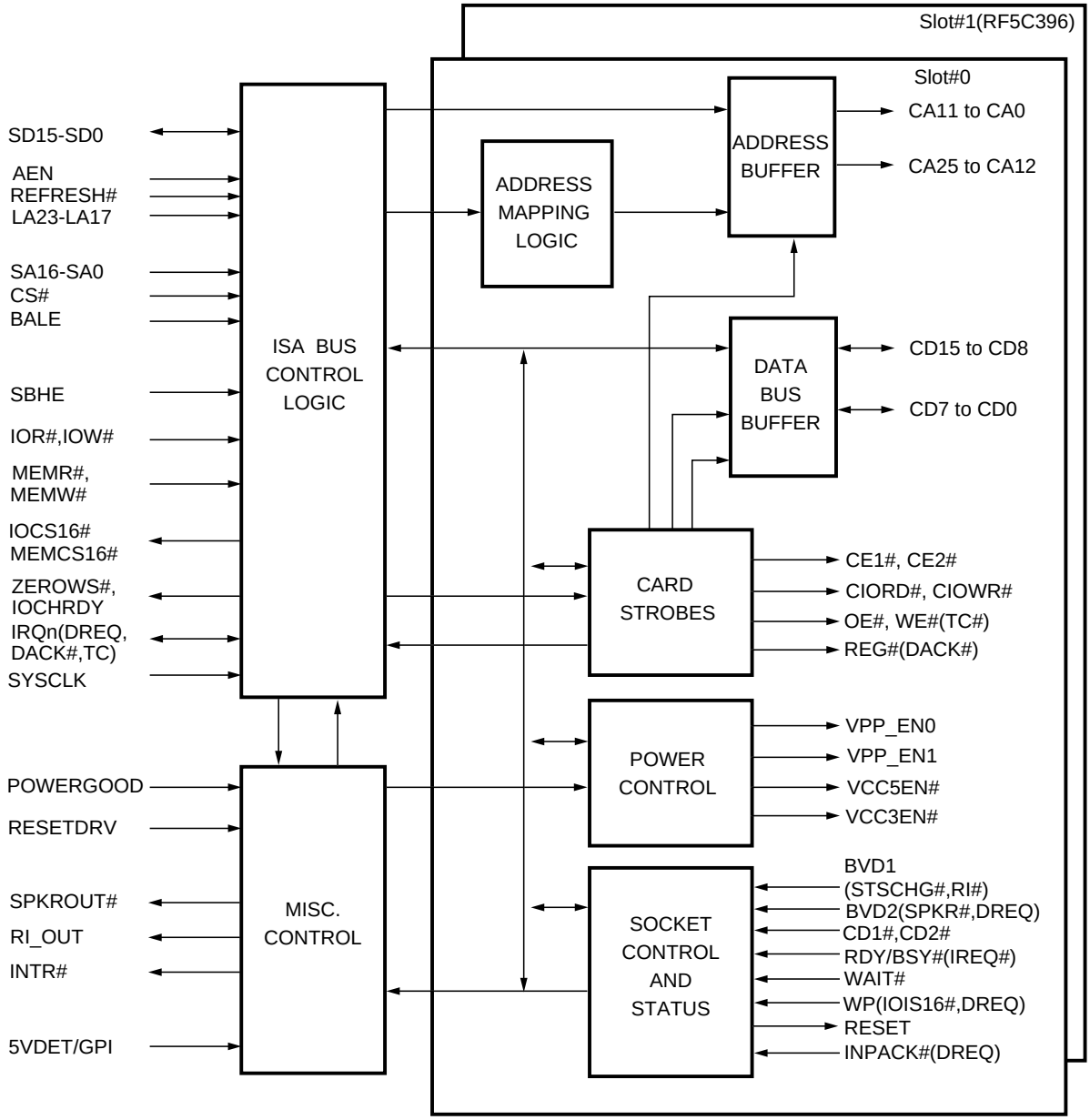
∗1) I : Input, O : Output, I/O : Input/Output, I (PU) : Input with Pull-up Register, I (PD) : Input with Pull-down Register, O (TS) : Tri-State Output.
∗2) All card slot interface signal names are pretended with A-(slot#0) and B-(slot#1).
For example, ACA25 to ACA0 are the card address buses to the slot #0.
Pin No. of the RB5C396 differ from those of others. Refer to “PIN CONFIGURATION”.
∗3) Applicable to only RF5C296.

4. Power and Ground Supply Pins

Symbol	Function	Pin No.	
		RF5C296	RF5C396*1
VCC	VCC for Core Logic	91	27
VCCAT	VCC for ISA Interface Signals	76, 135	138, 195
VCCSLOT	VCC for Card Interface Signals	18, 52	Slot#0 : 24,52 Slot#1 : 88,117
GND	Ground Pin	20,54,57,72,78, 128,133	31,70,79,111,140, 192

*1) All card slot interface signal names are pretended with A-(slot#0) and B-(slot#1).
For example, ACA25 to ACA0 are the card address buses to the slot#0.
Pin No. of the RB5C396 differ from those of others. Refer to “PIN CONFIGURATION”.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

RF5C296 (RF5C396) is a controller for supporting one (two) card slot compliant to PCMCIA2.1/JEIDA4.2 68pin standard. Direct connection to the card slot is allowed due to the complete buffering of signals to the card. RF5C296/RF5C396 can also interface directly to the ISA bus.

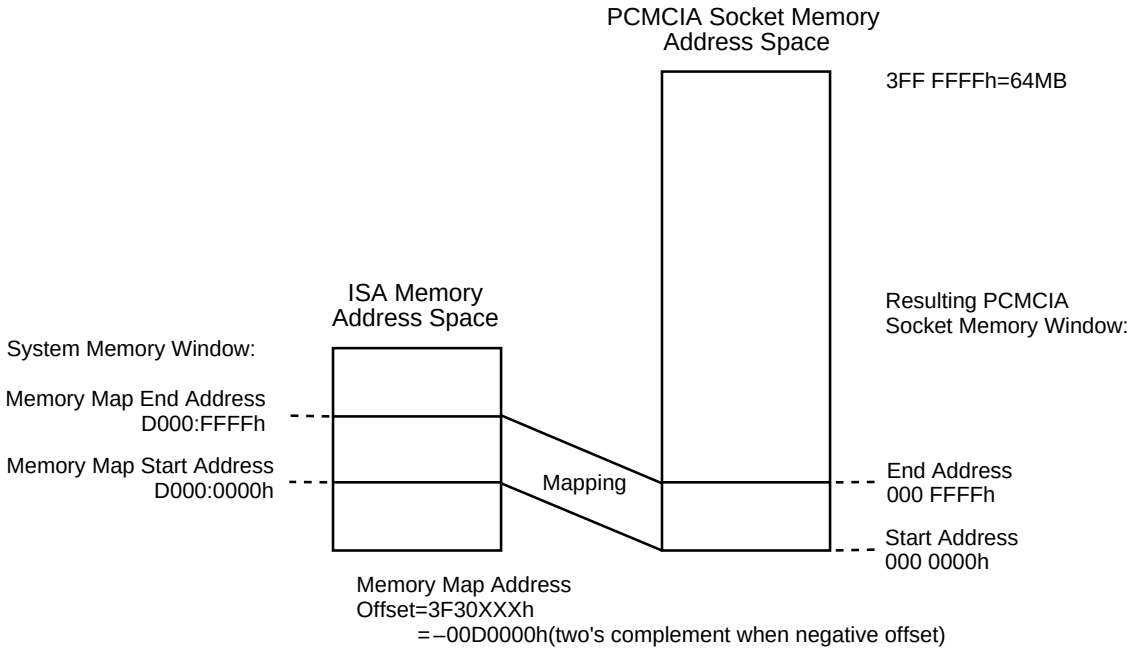
1. Address Mapping

Each socket has five independently enabled and controlled system memory address mapping windows and two independently enabled and controlled system I/O address mapping windows.

Some portions of 64MB common memory and 64MB attribute memory spaces on the PC Cards can be mapped into the smaller 16MB ISA address space.

Mapping of each system memory window can start and stop on any 4kB boundary of ISA system memory above 64kB except for I/O address space of 0000h to 0FFFFh by setting the system memory mapping start register, system memory mapping stop register, and card memory offset register. The summation result (in 2's complement) of the value in the card memory offset register and ISA system address value will result in the memory card address.

Each window has independent control of data bus size, the number of wait cycles, and the selection of common memory area or attribute memory area.



Each I/O window can be mapped with 1byte resolution between 0000h to 0FFFFh in the ISA system address space by setting the I/O start address register and the I/O stop address register. I/O mapping is not allowed during the DMA cycle.

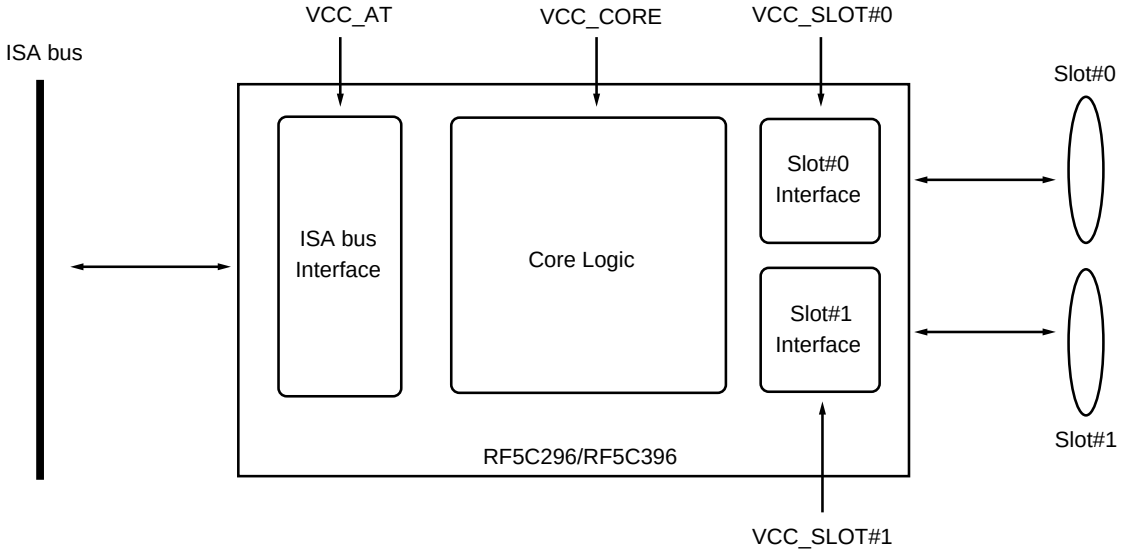
2. Power Management

When card slot is empty or the power supply is off, each card slot has independently power management because each slot has its own buffers and transceivers. In order to achieve the low power consumption especially for the notebook PCs, each address mapping circuit will be powered down when it is not activated. In addition to the function, setting the power down bit in the global control register to "1" enables the RF5C296/RF5C396 to go into the power down mode. There is a single power down control bit which can be written with either a Slot#0 or Slot#1 Global Control Register Index. Setting this bit to "1" goes into the power down mode. Even in the power down mode, RF5C296/RF5C396 can generate a card status change interrupt and PC Card interrupt for I/O cards. The RF5C296/RF5C396 can also generate the RI_OUT# signal when configured for ring indicate resume from I/O cards. In this Power down mode, the following ISA bus signals will be ignored.

SD[15 : 0], LA[23 : 17], SA[16 : 0], IORD#, IOWR#, AEN, BALE, SYSCLK, MEMW#, MEMR#, SBHE#

3. Mixed Voltage Operation

There are three/four different power nets ; VCC for ISA bus interface, VCC for core logic, VCC for card slot interface ; to be handled in RF5C296/RF5C396. Each of these power nets can be independently running at 3.3V or 5V. All of the voltage combinations listed on the next page are supported. RF5C296/RF5C396 can operate even with the single power supply of 5V or 3.3V



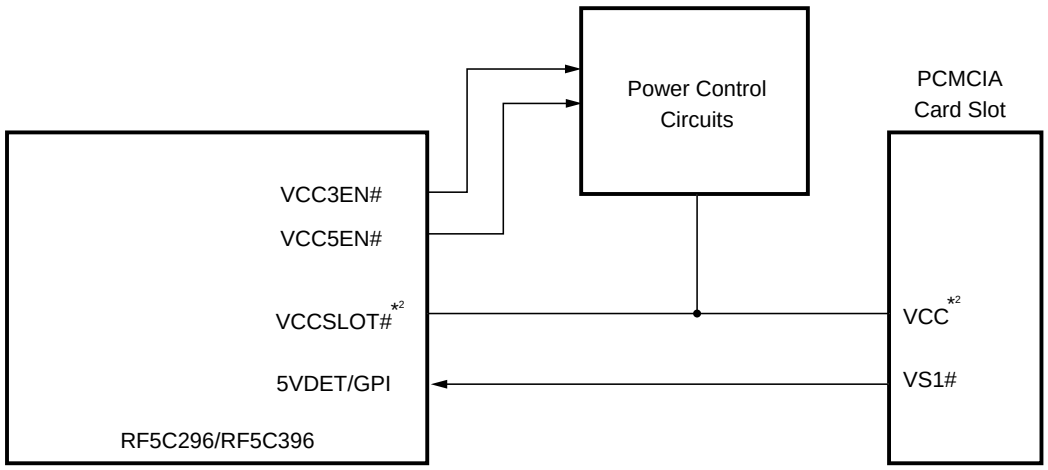
Core (VCC_CORE)	Card Slot#0 (VCC_SLOT#0)	Card Slot#1 (VCC_SLOT#1)	ISA bus Interface (VCC_AT)
5V	5V	5V	5V
3.3V	5V	5V	5V
3.3V	3.3V	5V	5V
3.3V	5V	3.3V	5V
3.3V	3.3V	3.3V	5V
3.3V	5V	5V	3.3V
3.3V	5V	3.3V	3.3V
3.3V	3.3V	5V	3.3V
3.3V	3.3V	3.3V	3.3V

Mixed Voltage Operation

When 5VDET/GPI pin is connected to PCMCIA card slot pin #43 (VS1#) as shown in the figure, the following should be considered.

(1) Interface Status Register bit7*1 indicate inverted 5VDET/GPI.

(2) Card Detect and Control Register bit2*1 (GPI enable) must be kept "0".



*1) Refer to page 27 "INTERNAL RESISTERS"

*2) As shown in the above table, the RF5C296 and the RF5C396 allow sharing of a power supply between their VCC_SLOTs and the PCcard slots, provided that the VCC_CORE should be set to 3.3V.

4. Address Mapping

To prevent any conflict between interrupt request signals derived from the RF5C296 or the RF5C396 and from any other device, the PC card status change, such as fluctuations in the voltage of the battery for the PC card and insertion or removal of the PC card into or from the PC card slot, as well as interrupt request signals (IREQ#) derived from the I/O cards can be assigned to one of the ten interrupt lines for ten interrupt request signals (IRQ15, IRQ14, IRQ12, IRQ11, IRQ10, IRQ9, IRQ7, IRQ5, IRQ4, and IRQ3).

These interrupt requests are programmable to the level mode or the edge trigger mode.

In addition to steering IRQn output, INTR# output is also used as an interrupt output. The INTR# pin signal is normally input to the EXTSMI# pin of the Intel 386SL to output a low-level pulse having three times the width of the SYSCLK pulse at the time of interrupt request generation and a high-level pulse at any other time.

In addition to these interrupts sources, it is programmable that IRQs will be generated when the transition occurs on GPI (General Purpose Input).

If card status change while other card status change interrupt request, second interrupt request pulse is not generated. In this case, the appropriate bit must be set to "1" in the Card Status Change Register (Index : 04h) in the Explicit Write Back Acknowledge Mode to enable interrupt request recognition by the host system interrupt processing routine. Upon interrupt request recognition, the bit is reset to "0".

Incidentally, all the bits in the Card Status Change Register (Index : 04h) are reset to "0" when it is read in any other mode than the Explicit Write Back Acknowledge Mode.

IRQ9, IRQ10, IRQ12, IRQ11 (or IRQ15) are multi-function pins. In PCMCIA-ATA mode, IRQ12 can drive LED. In DMA mode, IRQ9, IRQ10, IRQ11 (or IRQ15) work as DACK#, DREQ, TC.

5. Bus Sizing

In addition to 16bit bus cycle, RF5C296/RF5C396 supports 8bit bus cycle. The 8bit bus cycle to a PC Card can be generated even when the window is configured for 16bit. This means that the combination of SBHE# input and SA0 input override the data size configuration. On 8bit host systems, the SBHE# input must be pulled high (inactive) for proper operation. The following is a truth table of the card enable logic.

16bit Window	SBHE#	A0	CE2#	CE1#
YES	L	L	L	L
YES	L	H	L	H
YES	H	L	H	L
YES	H	H	H	L
NO	L	L	H	L
NO	L	H	H	L
NO	H	L	H	L
NO	H	H	H	L

6. Internal Register Access

All of the control registers of the RF5C296/RF5C396 are 8bit width registers and can be accessed using an indirect indexing scheme. Only two I/O addresses such as (3E1h) and (3E0h) are used to access all control registers.

RF5C296/RF5C396 has the external decode mode. In this mode, I/O address is decoded outside and input to CS#. When RESETDRV falls, if the level of INTR# pin is "H" ("L"), internal decode mode (external decode mode) can be selected.

Consequently, these operations can be enabled by externally pulling up or down the INTR# pin to such a degree as not to affect normal operation.

In the Internal Decode Mode, too, the CS# pin should be caused to transition to low level at the time of internal register access (the CS# pin should be caused to transition to high level only in the Power Down Mode).

The Index Register has the bit settings shown below :

Index Register (3E0h)							
bit7	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
"0": Device#0 "1": Device#1	"0": Slot#0 "1": Slot#1	Register Index					

There are 56 control registers provided for each PC card slot. The Index Register has bit7 for indicating a device number depending on the status of the SPKROUT# pin for the RF5C396 or the RI_OUT# pin for the RF5C296 at the falling edge of the RESETDRV pin signal. For the RF5C296, in particular, the Index Register has bit6 (Slot bit) for indicating a device number depending on the status of the SPKROUT# pin at the falling edge of the RESETDRV pin signal.

Both the SPKROUT# and RI_OUT# pins operate in the same manner as the INTR# pin described above.

The status of the SPKROUT# pin (for the RF5C396) or the RI_OUT# pin (for the RF5C296) corresponds to the index range as shown in the tables in "7. Plural (Three) Slot Systems" on the next page. Note that these pins also require their status control for connecting a single unit of the RF5C296 or the RF5C396.

7. Plural Slots System

7.1 Up to 4 slots

As described before, the settings of bit7 and bit6 (Slot bit) in the Index Register depend on the status of the SPKROUT# pin for the RF5C396 or the RI_OUT# pin for the RF5C296 and on the status of the the SPKROUT# pin for the RF5C296, respectively, at the falling edge of the RESETDRV pin signal. Therefore, 4 slots system can be constructed using plural RF5C296/RF5C396's without modifying I/O address (3E0h, 3E1h)

1-slot system : one RF5C296

2-slot system : one RF5C396 or two RF5C296

3-slot system : one RF5C396 and one RF5C296, or three RF5C296

4-slot system : two RF5C396, or one RF5C396 and two RF5C296, or four RF5C296

The following tables show the relation between the index range and the status of SPKROUT# and RI-OUT# when RESETDRV falls.

• RF5C296

RI_OUT#	SPKROUT#	Device bit	Slot bit	Index Range
VDD	VDD	0	0	00 to 3Fh
VDD	GND	0	1	40 to 7Fh
GND	VDD	1	0	80 to BFh
GND	GND	1	1	C0 to EFh

• RF5C396

SPKROUT#	Device bit	Slot bit	Index Range
VDD	0	0	00 to 3Fh
VDD	0	1	40 to 7Fh
GND	1	0	80 to BFh
GND	1	1	C0 to EFh

Notice

Access to any other index range than is specified at power-on is invalidated while any attempt to read the Index Register results in a data bus output of high impedance.

7.2 Five or More Slots

More than five PC card slots can also be supported through external decoding of the A15 to A1 pin signals for input to the CS# pin and thereby setting of any given I/O addresses of the internal registers for the RF5C296 and the RF5C396.

8. PCMCIA-ATA Mode

RF5C296/RF5C396 supports a PCMCIA-ATA interface mode. The following table shows the card interface signals when PCMCIA-ATA mode is configured.

PIN No.	PCMCIA I/O Interface Signal	ATA Interface Signal	PIN No.	PCMCIA I/O Interface Signal	ATA Interface Signal
1	GND	GND	35	GND	GND
2	CD3	CD3	36	CD1#	CD1#
3	CD4	CD4	37	CD11	CD11
4	CD5	CD5	38	CD12	CD12
5	CD6	CD6	39	CD13	CD13
6	CD7	CD7	40	CD14	CD14
7	CE1#	CE1#	41	CD15	CD15
8	CA10	CA10	42	CE2#	CE2#
9	OE#	OE#	43	NC	NC
10	CA11	CA11	44	CIORD#	CIORD#
11	CA9	CA9	45	CIOWR#	CIOWR#
12	CA8	CA8	46	CA17	CA17
13	CA13	CA13	47	CA18	CA18
14	CA14	CA14	48	CA19	CA19
15	WE#	WE#	49	CA20	CA20
16	IREQ#	IREQ#(IREQ)	50	CA21	*
17	VCC	VCC	51	VCC	VCC
18	VPP1	VPP1	52	VPP2	VPP2
19	CA16	CA16	53	CA22	*
20	CA15	CA15	54	CA23	*
21	CA12	CA12	55	CA24	*
22	CA7	CA7	56	CA25	*
23	CA6	CA6	57	RFU	NC
24	CA5	CA5	58	RESET	RESET
25	CA4	CA4	59	WAIT#	WAIT#
26	CA3	CA3	60	NC	NC
27	CA2	CA2	61	REG#	REG#
28	CA1	CA1	62	SPKR#	LED#
29	CA0	CA0	63	STSCHG#	STSCHG#
30	CD0	CD0	64	CD8	CD8
31	CD1	CD1	65	CD9	CD9
32	CD2	CD2	66	CD10	CD10
33	IOIS16#	IOIS16#	67	CD2#	CD2#
34	GND	GND	68	GND	GND

*) The signals are settable in the internal registers of RF5C296/RF5C396.

Setting the bit0 of the Mode Control Register 1 (Index=1Fh) to "1" configures the corresponding card slot to the PCMCIA-ATA mode. In PCMCIA-ATA mode, if the bit1 of the Mode Control Register is set to "1", the SPKR# input works as an LED input and IRQ12 works as an open drain LED output. At this time SPKROUT# will become inactive.

Bits2 to 6 can be set to specify the values of the CA21 to CA25 pin signals (marked with "*" in the pin definition table in the PCMCIA-ATA Mode on the previous page). In the PCMCIA-ATA Mode, the output CA21 to CA25 pin signals assume the values thus specified by bits2 to 6.

Bit7 can be set to prevent any conflict between the system floppy disk signal and the card interface signals. When set to "1", bit7 is disabled during reading from an I/O address of 3F7h and 377h on the system data bus.

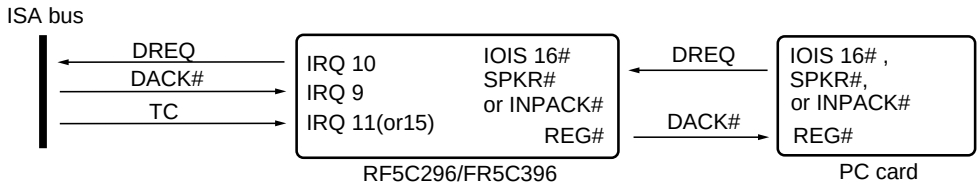
Mode Control Register 1 (Index=1Fh)							
bit7	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
377h, 3F7h Disable (in I/O Read)	A25	A24	A23	A22	A21	LED Enable	PCMCIA-ATA Mode

9. DMA Mode

RF5C296/RF5C396 provide the DMA Mode for supporting interfacing with external floppy disk units or other DMA devices via the PC card slots. Setting bit1 of Mode Control Register 3 to "1" enables DMA mode. The DMA data will be transferred to/from DMA capable PC Card with the ISA bus as a DMA master.

On the DMA mode, some of RF5C296/RF5C396 signal pins will be redefined. IRQ9 will work as DACK# input, IRQ10 will work as DREQ output, IRQ11 (or IRQ15) will work as TC input.

DREQ from the PC Card can be assigned to one of three PCMCIA inputs (IOIS16#, SPKR# or INPACK#) by setting bit7 and bit6 of Mode Control Register 2.



DMA made configuration

DMA transfer between the ISA system memory and the I/O card is available in the following two types :

1) DMA transfer between the ISA system memory and the I/O card
2) DMA transfer between memory in the I/O card and the I/O port via the system data bus.

Notice

Only one slot at a time should be enabled for DMA transfer. And DMA transfer to/from DMA capable PC Card may be 8 or 16bit as shown in the bus sizing table of page 21.

The TC# (terminal count) pin signal input to the PC card becomes active low for output from the OE# pin at a cycle for reading from the PC card (a cycle for writing to the memory) and from the E# pin at a cycle for writing to the PC card (a cycle for reading from the memory). Further, the output REG# pin signal is always held at high level during DMA transfer. Thus, it is easy to distinguish between DMA transfer and ordinary bus cycles. Namely, the REG# pin signal functions as DMA transfer acknowledgment for the PC card.

Notice on the DMA mode

1) IRQ9, IRQ10 and IRQ11 (or IRQ15) are redefined as DMA signals for ISA Bus. Therefore these signals can not be used as interrupt lines.
2) Bit5 of General Control Register must be set to "1" to select I/O card.
3) If WP/IOIS16# is used as DREQ, bit4 of Interface Status Register indicates DREQ from PC Card.
4) If BVD2/SPKR# is used as DREQ, SPKROUT# and LED output can not be used.
5) If INPACK# is used as DREQ, bit2 of Mode Control Register 2 must be kept "0".
6) TC input can be assigned to one of two IRQ signals (IRQ11 or IRQ15) by setting bit4 of Mode Control Register .

INTERNAL REGISTERS

RF5C396 has the registers both for Slot#0 (2) and Slot#1 (3). RF5C296 has the registers only for Slot#0 (1, 2, 3).

The internal registers have default bit settings (immediately after the falling edge of the RESETDRV pin signal when the POWERGOOD pin signal is set to "0") as enumerated below:

1. Chip Control

1.1 Identification and Revision Register*

Index : 00h Default value : 1000 0011b Read only

bit7 to bit6 : These bits indicate the type of PC Cards supported by the RF5C296/RF5C396.

bit7	bit6	Interface
0	0	I/O Only
0	1	Memory Only
1	0	Memory & I/O
1	1	Reserved

bit5 : Reserved

bit4 : Reserved

bit3 : Revision# : 0

bit2 : Revision# : 0

bit1 : Revision# : 1

bit0 : Revision# : 1

*) In this register, bits7 and 6 identify the type of the PC card controllers while bits3 to 0 indicate revision numbers. If this register is read, can be read back "83h".

1.2 Interface Status Register

Index : 01h Default value : Depends on PC card slot status Read only

bit7 : Indicates the state of the reverse of the GPI pin.

bit6 : PC Card Power Active. Indicates the current power status of the socket. "0" shows that power to the socket is off, and "1" shows that the power is provided to the socket.

bit5 : Ready/Busy Status Bit. This bit indicates the busy status when set to "0" and the ready status when set to"1" when the PC card is the memory card. Further, this bit specifies reading back of the IREQ# pin signal when the PC card is the I/O card.

bit4 : Memory Write Protect. Indicates the state of the WP pin. Memory write accesses to the slot will not be blocked unless the Write Protect bit in the Card Memory Offset Address Register High Byte is set to "1".

bit3 : Card Detect 2. This bit specifies reading back of the input CD2# pin signal in the inverted state. This bit will be set to "1" in the presence of the card in the slot when the IC core is connected to the external pull-up resistor because the CD2# pin is connected to the GND pin inside the card.

bit2 : Card Detect 1. This bit specifies reading back of the input CD1# pin signal in the inverted state. This bit will be set to "1" in the presence of the card in the slot when the IC core is connected to the external pull-up resistor because the CD1# pin is connected to the GND pin inside the card.

bit1 to 0 : Battery Voltage Detect 2&1. Bits 1 and 0 can be used to specify reading back of the status of the input BVD2 and BVD1 pin signals, respectively, when the PC card is the memory card. Bits 1 and 0 can also be used to specify the battery status as shown in the table below:

bit0	bit1	Status
0	0	Battery Dead
0	1	Battery Dead
1	0	Warning
1	1	Battery Good

For I/O card, bit0 indicates the current status of the (STSCHG#/RI#) signal from the I/O card when the ring indicate enable bit in the Interrupt and General Control Register is set to "0".

1.3 Power and RESETDRV Control Register

Index : 02h Default value : 0000 0000b Read & Write

bit7 : Output Enable. When set to "0", this bit specifies high impedance for slot output signals from the following pins : CA [25 : 0], CD [15 : 0], CE1#, CE2#, CIORD#, CIOWR#, OE#, REG#, RESET, and WE#. Note that the pull-down resistor and input slot signal of the DC [15 : 0] pin remain valid.

bit6 : Disable Resume RESETDRV. If bit is set to "1" and PWRGOOD="1", the restable registers of RF5C296/RF5C396 will not be reset. If the RESETDRV is a result of a system reset (PWRGOOD= "0"), the reset able registers of RF5C296/RF5C396 will be reset regardless of the setting bit.

bit5 : Auto Power Switch Enable. When this bit is set to "1", the power control values specified by bits4 to 0 (Power Control Bits) in this register and bit0 in the Mixed Voltage Control Register (Index : 2Fh) are automatically output upon setting of both the CD1# and CD2# pin signals to "0". Conversely, upon setting of either the CD1# or CD2# pin signal to "1", all the the power control values become inactive. When this bit is set to "0", the power control values specified by bits4 to 0 (Power Control Bits) in this register and bit0 in the Mixed Voltage Control Register (Index : 2Fh) are output regardless of whether the CD1# and CD2# pin signals are set to "0" or "1".

bit4 to bit0 : Power Control Bits. These bits cooperate with bit0 in the Mode Control Register (Index : 2Fh) to set the VCC3EN, VCC5EN, VPP_EN1, and VPP_EN0 pin signals to “0” or “1” as shown in the table below :

bit4	bit3*1	bit2*1	bit1	bit0	bit0 of Mode Control Register	VCC3EN#	VCC5EN#	VPP_EN1*2	VPP_EN0*3
1	×	×	0	0	0	1	**0**	0	0
1	×	×	0	0	1	0	**1**	0	0
1	×	×	0	1	0	1	**0**	0	1
1	×	×	0	1	1	0	**1**	0	1
1	×	×	1	0	0	1	**0**	1	0
1	×	×	1	0	1	0	**1**	1	0
1	×	×	1	1	0	1	**0**	1	1
1	×	×	1	1	1	0	**1**	1	1
0	×	×	×	×	×	1	1	1	0

⋆1) bit3 and bit2 : don't care. VCCnEN# means VCC5EN# or VCC3EN#, this signal defined by voltage selection.
⋆2) The settings of bits 3 and 2 are don't care. The settings of the VPP_EN1 and VPP_EN0 pin signals to “0” and “0”, “0” and “1”, “1” and “0”, and “1” and “1” specify their connection to no pin, connection to the VCC pin, connection to the VPP pin, and reservation, respectively.

1.4 Card Status Change Register

Index : 04h Default value : 0000 0000h Read & Write

bit7 to bit5 : Reserved

bit4 : GPI Change Bit. This bit will be set upon generation of any interrupt due to the GPI pin status change. This bit is held at “0” unless the GPI Enable Bit is set to “1” in the Card Detect and General Control Register.

bit3 : Card Detect Change. Bit is set to “1” when a change has been detected on either the CD#1 or CD2# pin.

bit2 : Ready Change. Bit is set to “1” when a low to high has been detected on the Ready/Busy# pin. Bit reads “0” for I/O cards.

bit1 : Bit is set to “1” when Battery Warning Condition has been detected. For the Battery Warning Condition, see the description of bits1 and 0 in the Interface Status Register (Index : 01h). Bit reads “0” for I/O cards.

bit0 : Bit is set to “1” when Battery Dead Condition has been detected for memory card. For the Battery Warning Condition, see the description of bits1 and 0 in the Interface Status Register (Index : 01h).
For I/O cards, bit is set to “1” if Ring Indicate Enable bit in the Interrupt and General Control Register is set to “0” and STSCHG#/RI# signal from I/O card has been pulled low. This bit reads “0” for I/O cards if the Ring Indicate Enable bit in the Interrupt and General Control Register is set to “1”.

The Card Status Change Register contains the status for sources of the card status change interrupt.

These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the Card Status Change Interrupt Configuration Register. There are two ways to reset this register,

(1) Read Card Status Change Register

(2) Write back "1" into the corresponding bit in the Card Status Change Register after setting Explicit Write Back Card Status Change Acknowledge bit to "1" in the Global Control Register.

1.5 Card Detect and General Control Register

Index : 16h Default value : 0000 0000b Read & Write

bit7 to bit6 : Reserved

bit5 : Software Card Detect Interrupt. If the Card Detect Enable bit is set to "1" in the Card Status Change Interrupt Configuration Register, then writing "1" to the Software Card Detect bit in the Card Detect and General Control Register will cause a card detect and status change interrupt. The functionality and acknowledgement of this software interrupt will work the same way as the hardware generated interrupt. This bit is always read as "0".

bit4 : Card Detect Resume Enable. When this bit is set to "1", and once a card detect change has been detected on the CD1# and CD2# inputs, RI-OUT# output will go "High" to "Low" and bit3 of Card Status Change Register will be set to "1". The RI_OUT# pin signal is held at "0" until bit3 is reset to "0" in the and Status Change Register. The RI_OUT# pin signal is not generated up on and detection unless the card detection enable bit is first set to "1" in the Card Status Interrupt Configuration Register (Index : 05h). If the card status change is routed to either the INTR# and any of IRQn signals, the setting of this bit to "1" will prevent INTR# and IRQn signal becoming active as a result of card status change.

bit3 : GPI Transition Control. Default value is "0".
If this bit is set to "0", a card status change interrupt will be generated when GPI# input goes "H" to "L".
If this bit is set to "1", a card status change interrupt will be generated when GPI# input goes "L" to "H".

bit2 : GPI Enable. If this bit is set to "1", a card status change interrupt will be generated when GPI# input changes.

bit1 : Configuration Reset Enable. If this bit is set to "1", a reset pulse will be generated when both CD1# and CD2# goes "L" to "H". This reset pulse reset the following registers.

Interrupt and General Control (Index : 03h) (except INTR# enable bit)
Address Window Enable (Index : 06h) (except MEMCS16# Decode A23 to A12 bit)
I/O Control (Index : 07h)
I/O Address n Start Low Byte (Index : 08h, 0Ch)
I/O Address n Start High Byte (Index : 09h, 0Dh)
I/O Address n Stop Low Byte (Index : 0Ah, 0Eh)
I/O Address n Stop High Byte (Index : 0Bh, 0Fh)
System Memory Address n Mapping Start Low Byte (Index : 10h, 18h, 20h, 28h, 30h)
System Memory Address n Mapping Start High Byte (Index : 11h, 19h, 21h, 29h, 31h)
System Memory Address n Mapping Stop Low Byte (Index : 12h, 1Ah, 22h, 2Ah, 32h)
System Memory Address n Mapping Stop High Byte (Index : 13h, 1Bh, 23h, 2Bh, 33h)
Card Memory Offset Address n Low Byte (Index : 14h,1Ch, 24h, 2Ch, 34h)
Card Memory Offset Address n High Byte (Index : 15h,1Dh, 25h, 2Dh, 35h)

bit0 : 16bit memory delay inhibit. Default value is “0”. If this bit is set to “0”, the falling edge of the control strobes OE# and WE# will be generated from the first falling edge of SYSCLK after the falling edge of MEMW# or MEMR# in the 16bit memory cycle. If this bit is set to “1”, the control strobes OE# and WE# will not be synchronously delayed by SYSCLK.

1.6 Global Control Register

Index : 1Eh Default value : ×××× 0000b Read &Write

This register is not duplicated per slot. This register can be accessed from either Slot#0 or Slot1# in RF5C396. Consequently, access to indexes of 1Eh and 5Eh means access to the same register.

bit7 to bit4 : Reserved

bit3 : IRQ14 Pulse Mode Enable. Setting this bit to "1" and bit 1 (Level Mode Interrupt Enable) to "0" will enable the RF5C296/RF5C396 to support pulse-mode IRQ14 interrupt output.

bit2 : Explicit Write Back Card Status Change Acknowledge Bit. Setting this bit to "1" will require an explicit write of "1" to the Card Status Change Register Bit which indicates an interrupting condition. Default value is "0". When this bit is set to "0", the card status change interrupt is acknowledged by reading the Card Status Change Register, and the register bits are cleared upon a read.

bit1 : In the Level Mode, the IRQn pin signals are held at high impedance until generation of any interrupt caused by the Card Status Change Register (Index : 04h) or routed by the IRQn pin signals from the I/O card. When this bit is set to "1", the IRQn pin signals are caused to transition from high impedance to "0" upon interrupt generation and reverted to high impedance upon completion of interrupt processing (in the Level Mode). When this bit is set to "0", the IRQn pin signals are caused to transition from "1" to "0" upon interrupt enabling and from "0" to "1" upon interrupt generation, and becomes inactive upon completion of interrupt processing (in the Edge Mode).

bit0 : Power Down Bit

If this bit is set to "1", then setting CS# to "1" will go into the power down mode. During CS# controlled power down, all internal registers are inaccessible, outputs are disabled, and the chip is at minimum power consumption level. IRQn and RI_OUT# will still be active to monitor the card detect and RI# status for resume indication.

CS#	Power Down Control Bit	Power Down Mode
0	0	No
1	0	No
0	1	No
1	1	Yes

1.7 Address Window Enable Register

Index : 06h Default value : 0000 0000b Read & Write

bit7 : I/O Window 1 Enable. If this bit is set to “0”, an I/O access within the I/O address Window 1 will inhibit the card enable signal.

bit6 : I/O Window 0 Enable. If this bit is set to “0”, an I/O access within the I/O address Window 0 will inhibit the card enable signal.

bit5 : MEMCS16# Decode A23 to A12. If this bit is set to “0”, MEMCS16# is generated from a decode of A23 to A17. If this bit is set to “1”, MEMCS16# is generated from a decode of A23 to A12. The MEMCS16# pin signal is output within any specified address range whether the PC card is the memory card or the I/O card.

bit4 : Memory Window 4 Enable Bit. If this Bit is set to “0”, a memory access within the Memory Window 4 will inhibit the card enable signal.

bit3 : Memory Window 3 Enable Bit. If this Bit is set to “0”, a memory access within the Memory Window 3 will inhibit the card enable signal.

bit2 : Memory Window 2 Enable Bit. If this Bit is set to “0”, a memory access within the Memory Window 2 will inhibit the card enable signal.

bit1 : Memory Window 1 Enable Bit. If this Bit is set to “0”, a memory access within the Memory Window 1 will inhibit the card enable signal.

bit0 : Memory Window 0 Enable Bit. If this Bit is set to “0”, a memory access within the Memory Window 0 will inhibit the card enable signal.

1.8 Interrupt and General Control Register

Index : 03h Default value : 0000 0000b Read & Write

bit7 : Ring Indicate Enable.
Setting this bit to "0" for I/O card, the STSCHG#/RI# signal from the I/O card is used as the status change signal STSCHG#. The current status of the signal is then available to the read from the Interface Status Register and this signal can be configured as a source for the card status change interrupt. Setting this bit to "1", STSCHG#/RI# signal from the I/O card is used as a ring indicator signal and is passed through to the RI_OUT# pin. For memory PC Card, bit has no function.

bit6 : PC Card Reset#. Setting this bit to "0" activates the Reset signal to the PC Card. The Reset signal will be active until this bit is set to "1".

bit5 : PC Card type. Setting this bit to "1" selects an I/O card. Setting this bit to "0" selects a memory card.

bit4 : INTR# Enable. Setting bit to "1" enables the card status change interrupt on the INTR# signal. If this bit is set to "0", the card status change interrupt is steered to one of the IRQn lines according bits7 through 4 in the card status change interrupt configuration register.

bit3 to bit0 : IRQn level selection (I/O card only).

bit3	bit2	bit1	bit0	IRQn Selection
0	0	0	0	IRQ not Selected
0	0	1	1	IRQ3 Enabled
0	1	0	0	IRQ4 Enabled
0	1	0	1	IRQ5 Enabled
0	1	1	1	IRQ7 Enabled
1	0	0	1	IRQ9 Enabled
1	0	1	0	IRQ10 Enabled
1	0	1	1	IRQ11 Enabled
1	1	0	0	IRQ12 Enabled
1	1	1	0	IRQ14 Enabled
1	1	1	1	IRQ15 Enabled

1.9 Card Status Interrupt Configuration Register

Index : 05h Default value : 0000 0000b Read & Write

bit7 to bit4 : These bits select the redirection of the card status change interrupt if the interrupt is not selected to INTR# pin.

INTR# Enable bit	bit3	bit2	bit1	bit0	IRQn Selection
0	0	0	0	0	IRQ not Selected
0	0	0	1	1	IRQ3 Enabled
0	0	1	0	0	IRQ4 Enabled
0	0	1	0	1	IRQ5 Enabled
0	0	1	1	1	IRQ7 Enabled
0	1	0	0	1	IRQ9 Enabled
0	1	0	1	0	IRQ10 Enabled
0	1	0	1	1	IRQ11 Enabled
0	1	1	0	0	IRQ12 Enabled
0	1	1	1	0	IRQ14 Enabled
0	1	1	1	1	IRQ15 Enabled
1	×	×	×	×	redirected to INTR#

bit3 : Card Detect Enable. Setting bit to “1” enables a card status change interrupt when a change has been detected on CD1# or CD2# signals.

bit2 : Ready Enable. Setting this bit to “1” enables a card status change interrupt when a “L” to “H” transition has been detected on READY/BUSY# signals. This bit is ignored when interface is configured for I/O card.

bit1 : Battery Warning Enable. Setting this bit to “1” enables a card status change interrupt when battery warning condition has been detected. This bit is ignored when interface is configured for I/O card.

bit0 : Battery Dead Enable. For memory cards, Setting this bit to “1” enables a card status change interrupt when a battery dead condition has been detected. For I/O cards, a card status change interrupt will be generated if the STSCHG#/RI# has been pulled “L” assuming Ring Indicate Enable Bit (bit7) in Interrupt and General Control Register is set to “0”.

2. I/O Mapping

2.1 I/O Control Register

Index : 07h Default value : 0000 0000b Read & Write

bit7 : I/O Window 1 Waite State. If this bit is set to “1” or this wait state is set by the wait# signal which is common to 8 and 16bit, 16bit system accesses occur with 1 additional wait state(4 SYSCLK).

bit6 : I/O Window 1 Zero Waite State. If this bit is set to “1”, 8bit system I/O accesses occur with zero additional wait states and ZEROWS# signal will be active.

bit5 : I/O Window 1 IOCS16# Source. If this bit is set to “0”, IOCS16# signal will be generated based on the value of the data size bit. If this bit is set to “1”, IOCS16# signal will be generated based on the IOIS16# signal.

bit4 : I/O Window 1 data size. “0” indicates 8bit mode, and “1” indicates 16bit mode.

bit3 : I/O Window 0 Wait State. If this bit is set to “1” or this wait state is set by the wait # signal which is common to 8 and 16bit, 16bit system accesses occur with 1 additional wait state(4 SYSCLK).

bit2 : I/O Window 0 Zero Waite State. If this bit is set to “1”, 8bit system I/O accesses occur with zero additional wait states and ZEROWS# signal will be active.

bit1 : I/O Window 0 IOCS16# Source. If this bit is set to “0”, IOCS16# signal will be generated based on the value of the data size bit. If this bit is set to “1”, IOCS16# signal will be generated based on the IOIS16# signal.

bit0 : I/O Window 0 data size. “0” indicates 8bit mode, and “1” indicates 16bit mode.

2.2 I/O Address n Start Register Low Byte

Index I/O Window 0 : 08h Default value : 0000 0000b Read & Write

Index I/O Window 1 : 0Ch

I/O Window 0 Start Address A7 to A0

bit7 : address 7

bit6 : address 6

bit5 : address 5

bit4 : address 4

bit3 : address 3

bit2 : address 2

bit1 : address 1

bit0 : address 0

2.3 I/O Address n Start Register High Byte

Index I/O Window 0 : 09h Default value : 0000 0000b Read & Write
Index I/O Window 1 : 0Dh

I/O Window 0 Start Address A15 to A8
bit7 : address 15
bit6 : address 14
bit5 : address 13
bit4 : address 12
bit3 : address 11
bit2 : address 10
bit1 : address 9
bit0 : address 8

2.4 I/O Address n Stop Register Low Byte

Index I/O Window 0 : 0Ah Default value : 0000 0000b Read & Write
Index I/O Window 1 : 0Eh

I/O Window 0 Stop Address A7 to A0
bit7 : address 7
bit6 : address 6
bit5 : address 5
bit4 : address 4
bit3 : address 3
bit2 : address 2
bit1 : address 1
bit0 : address 0

2.5 I/O Address n Stop Register High Byte

Index I/O Window 0 : 0Bh Default value : 0000 0000b Read & Write
Index I/O Window 1 : 0Fh

I/O Window 0 Stop Address A15 to A8
bit7 : address 15
bit6 : address 14
bit5 : address 13
bit4 : address 12
bit3 : address 11
bit2 : address 10
bit1 : address 9
bit0 : address 8

3. Memory Mapping

3.1 System Memory Address n Mapping Start Low Byte Register Index

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
10h	18h	20h	28h	30h

Default value : 0000 0000b Read & Write

bit7 : address 19
bit6 : address 18
bit5 : address 17
bit4 : address 16
bit3 : address 15
bit2 : address 14
bit1 : address 13
bit0 : address 12

3.2 System Memory Address n Mapping Start High Byte Register Index

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
11h	19h	21h	29h	31h

Default value : 0000 0000b Read & Write

bit7 : Data Size Bit. “0” indicates 8bit mode and “1” indicates 16bit mode.
bit6 : Zero Wait State. If this bit is set to “1”, an 8bit system memory access occur with zero additional wait states and ZEROWS# signal will be active. The WAIT# signal will override this bit.
bit5 : Scratch bit (Unused but intended for reading and writing.)
bit4 : Scratch bit (Unused but intended for reading and writing.)
bit3 : address 23
bit2 : address 22
bit1 : address 21
bit0 : address 20

3.3 System Memory Address n Mapping Stop Low Byte Register

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
12h	1Ah	22h	2Ah	32h

Default value : 0000 0000b Read & Write

bit7 : address 19
bit6 : address 18
bit5 : address 17
bit4 : address 16
bit3 : address 15
bit2 : address 14
bit1 : address 13
bit0 : address 12

3.4 System Memory Address n Mapping Stop High Byte Register

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
13h	1Bh	23h	2Bh	33h

Default value : 0000 0000b Read & Write

bit7 : Wait State Bit 1
bit6 : Wait State Bit 0

wait state bit 1	wait state bit 0	# of additional cycle	# of SYSCLK per access
0	0	standard 16bit cycle	3
0	1	1	4
1	0	2	5
1	1	3	6

bit5 : Reserved
bit4 : Reserved
bit3 : address 23
bit2 : address 22
bit1 : address 21
bit0 : address 20

3.5 Card Memory Offset Address n Low Byte Register

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
14h	1Ch	24h	2Ch	34h

Default value : 0000 0000b Read & Write

bit7 : offset address 19
bit6 : offset address 18
bit5 : offset address 17
bit4 : offset address 16
bit3 : offset address 15
bit2 : offset address 14
bit1 : offset address 13
bit0 : offset address 12

3.6 Card Memory Offset Address n High Byte Register

Index :

Memory Window 0	Memory Window 1	Memory Window 2	Memory Window 3	Memory Window 4
15h	1Dh	25h	2Dh	35h

Default value : 0000 0000b Read & Write

bit7 : Write Protect Bit. If this bit is set to "1", write operations to the PC Card through the corresponding system memory window are inhibited.
bit6 : Reg Active.If this bit is set to "1", accesses to the system memory window will result in attribute memory on PC Card being accessed.
bit5 : offset address 25
bit4 : offset address 24
bit3 : offset address 23
bit2 : offset address 22
bit1 : offset address 21
bit0 : offset address 20

4. Expansion Function

4.1 Mode Control Register 1

Index : 1Fh Default value : 0000 0000b Read & Write

bit7 : When set to "1", this bit specifies disabling bit7 in the data bus for an I/O address of 377h or 3F7h (at read time). When set to "0", this bit specifies no such disabling. This bit defaults to "0" and can be set independently of bit0.

bit6 : In PCMCIA-ATA mode, the value of this bit appears at CA25.

bit5 : In PCMCIA-ATA mode, the value of this bit appears at CA24.

bit4 : In PCMCIA-ATA mode, the value of this bit appears at CA23.

bit3 : In PCMCIA-ATA mode, the value of this bit appears at CA22.

bit2 : In PCMCIA-ATA mode, the value of this bit appears at CA21.

bit1 : In PCMCIA-ATA mode, if this bit is set to "1", the SPKR# input works as an LED input and IRQ12 works as an open drain LED output. Default value is "0".

bit0 : PCMCIA-ATA mode bit. "1" selects PCMCIA-ATA mode and "0" selects PCMCIA mode. Default value is "0".

4.2 Mode Control Register 2

Index : 2Fh Default value : 0000 0000b Read & Write

bit7 to bit6 : DMA Request Selection Bits. DREQ from PC Card is defined according to these 2 bits. Default values are "0".

bit 7 bit 6	01	10	11
DREQ	INPACK#	SPKR#/LED#	IOIS16#

bit5 : If this bit is set to "1", DREQ is "L" active. If this bit is set to "0", DREQ is "H" active. Default value is "0".

bit4 : DMA Mode TC Selection Bit.
If this bit is set to "0", IRQ11 works as TC. If this bit is set to "1", IRQ15 works as TC.

bit3 : Direct 5V/3.3V Switch Enable. If bit4 of Power and RESETDRV Control Register is set to "1", setting this bit to "1" will allow the status of 5VDET/GPI pin to select VCC3EN# or VCC5EN# independently of bit0. Default value is "0".

bit2 : Input Acknowledge Enable. If this bit is set to "1", INPACK# pin function is enabled. If this bit is set to "0", INPACK# is disabled. When the input INPACK# pin signal is active, I/O read data are output to the system data bus only if the input INPACK# pin signal is held at "L". Default value is "0".

bit1 : IREQ# Sense Selection Bit. If this bit is set to "0", IREQ# is "L"active. If this bit is set to "1", IREQ# is "H"active. Default value is "0".

bit0 : Voltage Selection Bit. If bit4 of Power and RESETDRV Control Register is set to "1", setting this bit to "1" will set VCC3EN# "L". If bit4 of Power and RESETDRV Control Register setting this bit to "0" will set VCC5EN# "L". Default value is "0".

5. I/O Address Remapping

This function is available only in RF5C396. I/O offset address can be set in the following registers. Card I/O address is the summation result of system address and I/O offset address.

5.1 Card I/O Offset Address 0 Low Byte Register

Index : 36h Default value : 0000 0000b Read & Write

bit7 : offset address 7
bit6 : offset address 6
bit5 : offset address 5
bit4 : offset address 4
bit3 : offset address 3
bit2 : offset address 2
bit1 : offset address 1
bit0 : always “0”

5.2 Card I/O Offset Address 0 High Byte Register

Index : 37h Default value : 0000 0000b Read & Write

bit7 : offset address 15
bit6 : offset address 14
bit5 : offset address 13
bit4 : offset address 12
bit3 : offset address 11
bit2 : offset address 10
bit1 : offset address 9
bit0 : offset address 8

5.3 Card I/O Offset Address 1 Low Byte Register

Index : 38h Default value : 0000 0000b Read & Write

bit7 : offset address 7
bit6 : offset address 6
bit5 : offset address 5
bit4 : offset address 4
bit3 : offset address 3
bit2 : offset address 2
bit1 : offset address 1
bit0 : always “0”

5.4 Card I/O Offset Address 1 High Byte Register

Index : 39h Default value : 0000 0000b Read & Write

bit7 : offset address 15
bit6 : offset address 14
bit5 : offset address 13
bit4 : offset address 12
bit3 : offset address 11
bit2 : offset address 10
bit1 : offset address 9
bit0 : offset address 8

5.5 Chip Identification Register (Read Only)

Index : 3Ah Default value : 32h (RF5C296), B2h (RF5C396) Read Only
Read only register, 32h is read back from RF5C296, B2h is read back from RF5C396.

5.6 Mode Control Register 3

Index : 3Bh Default value : 0000 0000b Read & Write

bit7 to bit2 : Reserved.

bit1 : DMA Mode Enable Bit.
When this bit is set to "1", the DMA Mode is selected in which DMA-related signals are redefined as described in "DMA Mode". This bit defaults to "0". This bit cannot be set to "1" simultaneously for Slot #0 and Slot #1.

bit0 : PCMCIA Interface Disable Bit.
If this bit is set to "1", signals shown in the below table are set to "Z", all PCMCIA interface signals are disabled and become "Z". The built-in pull-down resistor is disabled for data bus signals. Slot output signals will be caused to transition to high impedance even when bit 0 is set in the Power and RESETDRV Control Register.

Input	CD1#, CD2#, BVD1, BVD2, RDY/BSY#, WAIT#, WP, INPACK#
Output	CA[25 : 0], CD[15 : 0], CE1#, CE2#, CIORD#, CIOWR#, OE#, REG#, RESET, WE#

6. Summary of Internal Register

Slot#0 offset	Slot#1 offset	Register Name	Default Value 7654 to 3210
+00h	+40h	Identification and Revision	1000 0011
+01h	+41h	Interface Status	×011 ××11
+02h	+42h	Power and RESETDRV Control	0000 0000
+03h	+43h	Interrupt and General Control	0000 0000
+04h	+44h	Card Status Change	0000 0000
+05h	+45h	Card Status Change Interrupt Configuration	0000 0000
+06h	+46h	Address Window Enable	0000 0000
+07h	+47h	I/O Control	0000 0000
+08h	+48h	I/O Address 0 Start Low Byte	0000 0000
+09h	+49h	I/O Address 0 Start High Byte	0000 0000
+0Ah	+4Ah	I/O Address 0 Stop Low Byte	0000 0000
+0Bh	+4Bh	I/O Address 0 Stop High Byte	0000 0000
+0Ch	+4Ch	I/O Address 1 Start Low Byte	0000 0000
+0Dh	+4Dh	I/O Address 1 Start High Byte	0000 0000
+0Eh	+4Eh	I/O Address 1 Stop Low Byte	0000 0000
+0Fh	+4Fh	I/O Address 1 Stop High Byte	0000 0000
+10h	+50h	System Memory Address 0 Mapping Start Low Byte	0000 0000
+11h	+51h	System Memory Address 0 Mapping Start High Byte	0000 0000
+12h	+52h	System Memory Address 0 Mapping Stop Low Byte	0000 0000
+13h	+53h	System Memory Address 0 Mapping Stop High Byte	0000 0000
+14h	+54h	Card Memory Offset Address 0 Low Byte	0000 0000
+15h	+55h	Card Memory Offset Address 0 High Byte	0000 0000
+16h	+56h	Card Detect and General Control	0000 0000
+17h	+57h	Reserved	0000 0000
+18h	+58h	System Memory Address 1 Mapping Start Low Byte	0000 0000
+19h	+59h	System Memory Address 1 Mapping Start High Byte	0000 0000
+1Ah	+5Ah	System Memory Address 1 Mapping Stop Low Byte	0000 0000
+1Bh	+5Bh	System Memory Address 1 Mapping Stop High Byte	0000 0000
+1Ch	+5Ch	Card Memory Offset Address 1 Low Byte	0000 0000
+1Dh	+5Dh	Card Memory Offset Address 1 High Byte	0000 0000
+1Eh	+5Eh	Global Control	×××× 0000

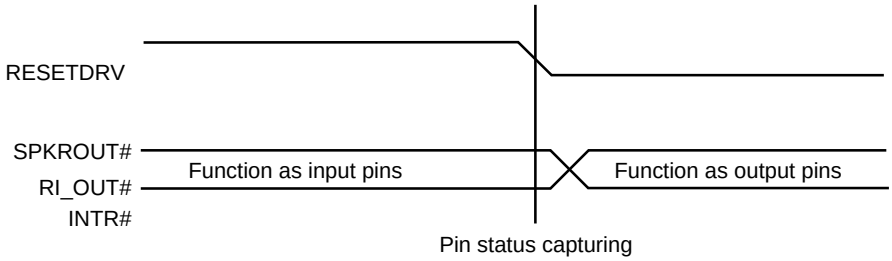
Slot#0 offset	Slot#1 offset	Register Name	Default Value 7654 to 3210
+1Fh	+5Fh	Mode Control 1	0000 0000
+20h	+60h	System Memory Address 2 Mapping Start Low Byte	0000 0000
+21h	+61h	System Memory Address 2 Mapping Start High Byte	0000 0000
+22h	+62h	System Memory Address 2 Mapping Stop Low Byte	0000 0000
+23h	+63h	System Memory Address 2 Mapping Stop High Byte	0000 0000
+24h	+64h	Card Memory Offset Address 2 Low Byte	0000 0000
+25h	+65h	Card Memory Offset Address 2 High Byte	0000 0000
+26h	+66h	Reserved	0000 0000
+27h	+67h	Reserved	0000 0000
+28h	+68h	System Memory Address 3 Mapping Start Low Byte	0000 0000
+29h	+69h	System Memory Address 3 Mapping Start High Byte	0000 0000
+2Ah	+6Ah	System Memory Address 3 Mapping Stop Low Byte	0000 0000
+2Bh	+6Bh	System Memory Address 3 Mapping Stop High Byte	0000 0000
+2Ch	+6Ch	Card Memory Offset Address 3 Low Byte	0000 0000
+2Dh	+6Dh	Card Memory Offset Address 3 High Byte	0000 0000
+2Eh	+6Eh	Reserved	0000 0000
+2Fh	+6Fh	Mode Control 2	0000 0000
+30h	+70h	System Memory Address 4 Mapping Start Low Byte	0000 0000
+31h	+71h	System Memory Address 4 Mapping Start High Byte	0000 0000
+32h	+72h	System Memory Address 4 Mapping Stop Low Byte	0000 0000
+33h	+73h	System Memory Address 4 Mapping Stop High Byte	0000 0000
+34h	+74h	Card Memory Offset Address 4 Low Byte	0000 0000
+35h	+75h	Card Memory Offset Address 4 High Byte	0000 0000
+36h	+76h	Card I/O Offset Address 0 Low Byte	0000 0000
+37h	+77h	Card I/O Offset Address 0 High Byte	0000 0000
+38h	+78h	Card I/O Offset Address 1 Low Byte	0000 0000
+39h	+79h	Card I/O Offset Address 1 High Byte	0000 0000
+3Ah	+7Ah	Chip Identification	×011 0010*
+3Bh	+7Bh	Mode Control 3	0000 0000

*) Chip Identification Register bit7 is read back “0” from RF5C296, “1” from RF5C396.

HARDWARE DESIGN CONSIDERATIONS

1. Initial Value Setting Pins

For the RF5C296 and the RF5C396, the SPKROUT#, RI_OUT#, and INTR# pins function as output pins normally but as input pins whose input status determine internal settings during the time that the RESETDRV pin is held at high level as shown in the diagram below.



Internal settings can be made by pulling up or down these pins to such a degree as not to affect normal operation (on the order of 10kΩ for ordinary circuits).

1.1 SPKROUT# and RI_OUT# Pins

The SPKROUT# and RI_OUT# pins determine an index range for access to the internal registers as shown in the table below :

• RF5C296

RI_OUT#	SPKROUT#	Device bit	Slot bit	Index Range
VDD	VDD	0	0	00 to 3Fh
VDD	GND	0	1	40 to 7Fh
GND	VDD	1	0	80 to BFh
GND	GND	1	1	C0 to EFh

• RF5C396

SPKROUT#	Device bit	Slot bit	Index Range
VDD	0	0	00 to 3Fh
VDD	0	1	40 to 7Fh
GND	1	0	80 to BFh
GND	1	1	C0 to EFh

1.2 INTR# Pin

The INTR# pin determines whether to use external decoding or internal decoding for access to the internal registers. Pulling up and down the INTR# pin specifies internal decoding and external decoding, respectively. For details, see "6. Access to Internal Registers" in "FUNCTIONAL DESCRIPTION".

2. Connections to System Bus

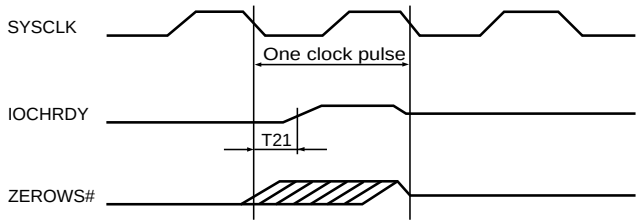
2.1 IOCS16#, MEMCS16#, ZEROWS#, and IOCHRDY Pins

Basically, connections to the ISA bus only require connections to corresponding bus pins.

The IOCS16#, MEMCS16#, ZEROWS#, and IOCHRDY pins are open-drain output pins which require an external pull-up resistor in the absence of any pull-up resistor provided on the ISA bus. These resistors are designed to drive a 300Ω pull-up resistor (for the IOCS16#, MEMCS16#, and ZEROWS# pins) and a 1kΩ pull-up resistor (for the IOCHRDY).

The ZEROWS# and IOCHRDY pins are also caused to transition to "H" level for the maximum duration of one clock pulse upon transition from low level to high impedance as shown in the figure below. Originally, strict regulation of the pull-up resistor for these open-drain output pins is required for the fast rising edge of their pin signals but not recommended in consideration of current consumption.

For the RF5C296 and the RF5C396, such unique designs of the ZEROWS# and IOCHRDY pins allow restriction of current consumption without strict regulation of the pull-up resistor to such a degree as not to affect any other system.



2.2 CS# Pin

The CS# pin is intended to determine an I/O address for access to the control registers for the RF5C296 and the RF5C396 and not directly related to access to the card windows.

As described before, either external decoding or internal decoding can be used to determine an I/O address for access to the control registers. (For details, see "6. Access to Internal Registers" in "FUNCTIONAL DESCRIPTION".)

When external decoding is used, an I/O address for access to the control registers can be determined by decoding the address signals output from the SA15 to the SA1 (or the SA23 to the SA16 for some systems) for input with negative logic to the CS# pin.

When internal decoding is used, access to the internal registers is conditional upon the CS# pin held at "L" and an I/O address of 03E0h or 03E1h. In this case, the CS# pin must receive a signal input which becomes active only when the SA15 to SA10 pins are all caused to transition to "L". This is because the status of the CE# pin affects the Power Down Mode (specified by bit0 in the Global Control Register (Index : 1Eh)). When the Power Down Mode is not in use, therefore, the CE# pin should be held at "L".

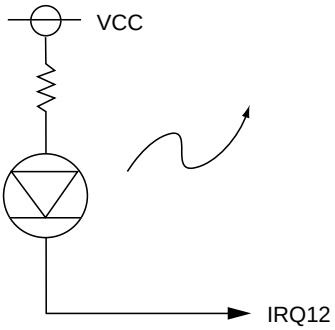
Whether external decoding or internal decoding is used, note that an address for access to the I/O window (not an address to access to the internal registers) is determined by decoding the address signals output from the SA23 to SA16 pins to (0000 0000)b.

2.3 RESETDRV and POWERGOOD Pins

For the RF5C296 and the RF5C396, reset operation is conditional upon the POWERGOOD pin held at "L"and the RESETDRV pin held at "H". When not in use, therefore, the POWERGOOD pin should be held at "L".

2.4 IRQ12 Pin and LED

Besides connection to the ISA bus, the IRQ12 pin is available in connection to the LED in the PCMCIA_ATA Mode. Direct connection to the LED causes so large a current load to the IRQ12 pin that it should be connected in series to a limiting resistor on the order of 300Ω to 1kΩ for connection to the VCC as shown in the figure below. The limiting resistor should be regulated in such a manner that current flowing into the IC core does not exceed 20 mA.



Notes for connecting to System bus except ISA bus

The RF5C296 and the RF5C396 must be connected to any other system bus than the ISA bus in consideration of the following pins:

1) BALE Pin

The BALE pin signal is intended to latch the address signals output from the LA23 to LA17 pins because retention of these pin signals is not guaranteed in the entire instruction cycle on the ISA bus. In practice,they are half-latched. The BALE pin may be held at "H", therefore, when the LA23 to LA17 pin signals are retained in the entire instruction cycle on any other bus in the same manner as the SA16 to SA0

2) AEN Pin

The AEN pin signal indicates the DMA Mode when held at "H". As such, it should be held at "L" when the DMA Mode is not in use.

3) REFRESH# Pin

The REFRESH# pin signal indicates the refresh period of the ISA bus when held at "L". For the RF5C296 and the RF5C396, memory access is conditional upon the REFRESH# pin signal held at "H". The REFRESH# pin signal should be held at "H", therefore, when not in use.

4) SYSCLK Pin

The SYSCLK pin signal normally has a frequency of 8.33MHz on the ISA bus. For the RF5C296 and the RF5C396, the SYSCLK pin signal is used for the following five purposes :

- · Determination of wait time
- · Determination of the pulse width of the INTR# pin signal
- · Determination of the reset pulse width of the card states change register in the explicit write back mode.
- · Bit 0 function of Card Detect and General Control register.
- · Determination of the high-level duration of the ZEROWS# and IOCHRDY pin signals

(For details, see "2.1 IOCS16#, MEMCS16#, ZEROWS#, and IOCHRDY Pins" in "2. Connections to System Bus".)

As long as the above purposes can be achieved, the SYSCLK pin signal may be available at a maximum frequency of 11MHz or in DC form.

3. Connections to PCMCIA Slot

3.1 Pull-up Resistor

The Personal Computer Memory Card Industry Association (PCMCIA) standard requires that some types of pins should be pulled up on the PC card slots. Besides these pins,there are some pins which must be pulled up on the system side. They are listed in the table below.

Pins which must be pulled up	Power supply to which pins are pulled up
RDY/BSY#,INPACK#,WAIT#, WP,BVD1,BVD2	(VCC common to card power supply)
CD1#,CD2#,VS1#	VCC_AT

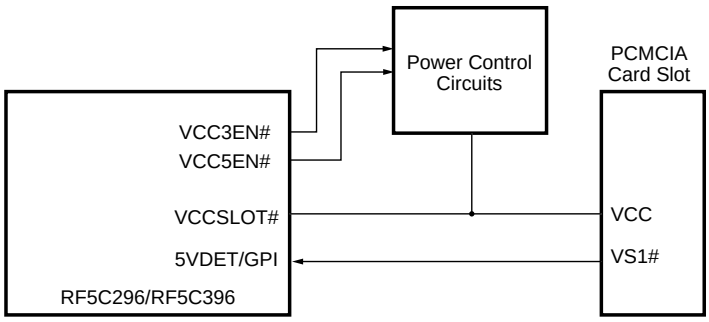
For the RF5C296 and the RF5C396, the VSI# pin, which is connected to the 5VDET/GPI pin internally pulled up, requires no external pull-up resistor while the other pins listed above require an external pull-up resistor. For details, see "3.2 5VDET/GPI and VSI# Pins".

Basically, the CD1# and CD2# pins should be pulled by a power supply which survives after removal of the PC card from the PC card slot and therefore be confined to the VCC_CORE or the VCC_AT.

For the RF5C296 and the RF5C396, in particular, the CD1# and CD2# pins are powered by, and should therefore be pulled up to, the VCC_AT.

3.2 5VDET/GPI and VS1# Pins

Originally, the 5VDET/GPI pin is used as a general-purpose input (GPI) pin capable of generating interrupts upon occurrence of any input change. The VS1# pin is connected to the GND pin on the 3.3V PC card and no connection pin on any other card. The 5VDET/GPI pin, which is internally pulled up as described before, can be connected to the VS1# pin as shown in the figure below to identify whether the PC card supply voltage is 5 or 3.3V.



The 5VDET/GPI pin must be connected to the VS1# pin in consideration of the following :

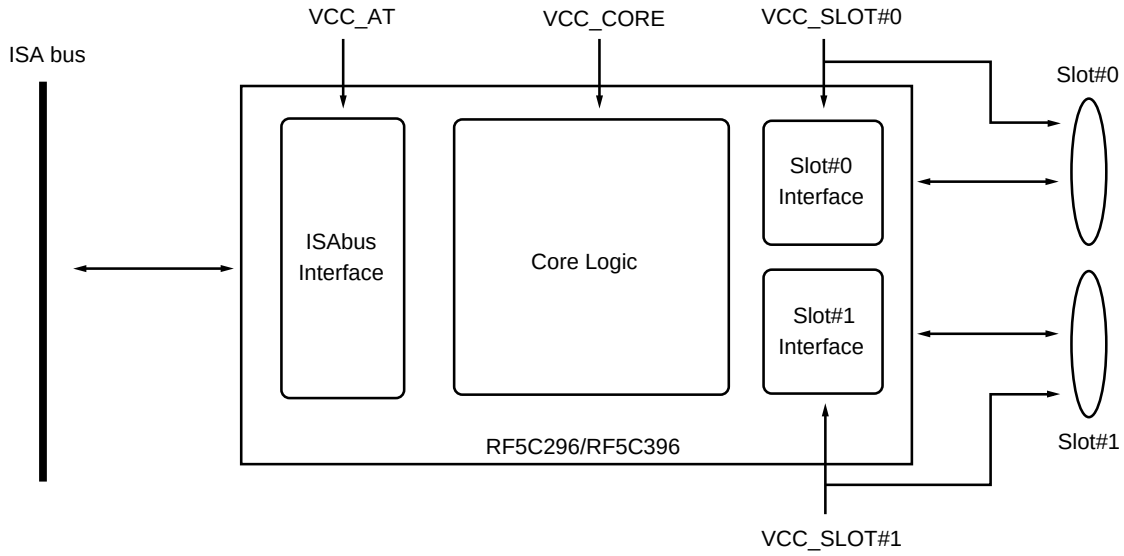
· An inverted signal from the 5VDET/GPI pin is read back to bit7 in the Interface Status Register.
· Bit2 (GPI Enable Bit) must always be set to "0" in the Card Detect and Control Register.

For details on bit7 in the Interface Status Register and bit2 (GPI Enable Bit) in the Card Detect and Control Register, see "6. Access to Internal Registers" in "FUNCTIONAL DESCRIPTION".

4. Connections to Power Supply System

4.1 VCC_CORE, VCC_SLOT, and VCC_AT

The RF5C296 and the RF5C396 are designed to supply separate power for the IC core, the ISA bus interface, and the PC card slots from the VCC_CORE, the VCC_AT, and the VCC_SLOT, respectively, as shown in the figure below :



Available power supply combinations are shown in the table below :

Core (VCC_CORE)	Card Slot#0 (VCC_SLOT#0)	Card Slot#1 (VCC_SLOT#1)	ISA bus Interface (VCC_AT)
5V	5V	5V	5V
3.3V	5V	5V	5V
3.3V	3.3V	5V	5V
3.3V	5V	3.3V	5V
3.3V	3.3V	3.3V	5V
3.3V	5V	5V	3.3V
3.3V	5V	3.3V	3.3V
3.3V	3.3V	5V	3.3V
3.3V	3.3V	3.3V	3.3V

As is clear from the above table, the 5V power supply for the IC core (the VCC_CORE) is available in combination with only the 5V peripheral power supplies (the VCC_SLOT#0 for the Card Slot#0, the VCC_SLOT#1 for the Card Slot#1, and the VCC_AT for the ISA bus interface). On the contrary, the 3.3V power supply for the IC core is available in combination with both the 3.3V and 5V peripheral power supplies.

The RF5C296 and the RF5C396 are designed to have their power supply system controlled by four output pins : VCC3EN#, VCC5EN#, VPP_EN0, and VPP_EN1. Set the VCC3EN# pin to "0" by controlling the internal register in case of that the 3.3V is supplied to the power supply (VCC_SLOT) of the PC card slots. Set the VCC5EN# pin to "0" by controlling the internal register in case of that the 5.0V is supplied to the power supply (VCC_SLOT) of the PC card slots. Both the VCC3EN# and VCC5EN# cannot be set to "0" simultaneously.

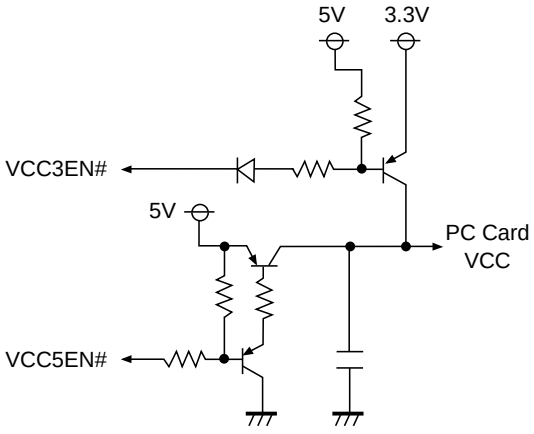
Set the VPP_EN0 pin to "1" by controlling the internal register in case of that the VPP (5V) is supplied to the VPP of the PC card slots. Set the VPP_EN1 pin to "1" by controlling the internal register in case of that the VPP (12V) is supplied to the VPP of the PC card slots. Both the VPP_EN0 and VPP_EN1 pins may be set to "1" simultaneously under certain register settings, thus requiring due attention in either hardware or software design.

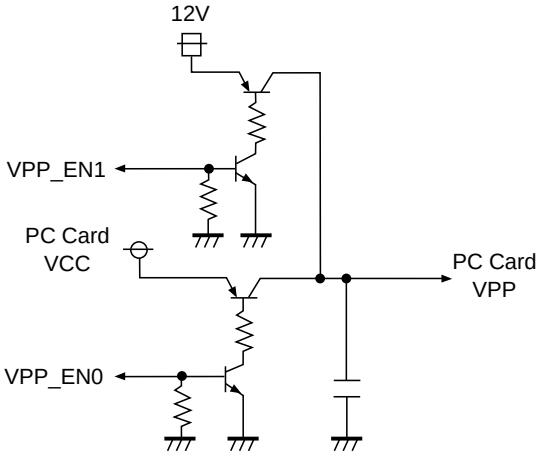
The Intel 82365SL has the four VPP_EN pins and provides separate control over the two power supply pins (VPP1 and VPP2). On the contrary, the RF5C296 and the RF5C396 have the two VPP_EN pins and provide simultaneous control over the VPP1 and VPP2 pins.

As an alternative measure, the RF5C296 and the RF5C396 allow separate control over the VPP1 and VPP2 pins by the VPP_EN0 and VPP_EN1 pins, respectively, provided that both the VPP1 and VPP2 must be provided with either the 5V or 12V power supply without fail.

These four output pins are controlled by the Power and RESETDRV Control Register (Index : 02h) and the Mixed Voltage Control Register (Index : 2Fh).

These pins can be used to configure an external driver for applying voltage to the two power supply pins (VPP1 and VPP2) on the PC card slots. Power supply circuitry for the RF5C296 and the RF5C396 is exemplified in the diagrams below :





5. Connecting Multiple Units of RF5C296 or RF5C396

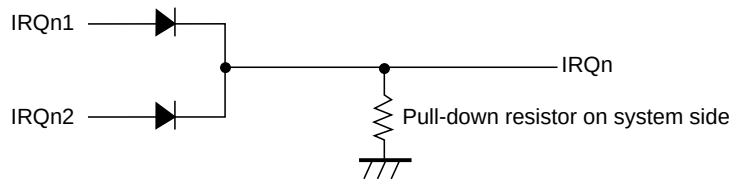
To connect multiple units of the RF5C296 or the RF5C396 to the same system bus, their respective PC card slots must be provided with independent indexes by connecting a pull-up or pull-down resistor to the SPKROUT# and RI_OUT# pins. (For details, see "7. Plural Slot System" in "FUNCTIONAL DESCRIPTION" and "1. Initial Value Setting Pins" in "HARDWARE DESIGN CONSIDERATIONS")

Multiple connections to the system bus are wired OR using the IRQn pins. The IRQn pins should be used in consideration of a conflict between interrupt request signals. Driving software for ordinary PC card controllers assigns the same IRQ number to different interrupt signals derived from the PC card status change. Such assignment causes a conflict between interrupt request signals. This problem can be solved by the following three measures :

(1) Confining IRQn interrupt request signals derived from the PC card status change to any one unit of the RF5C296 or the RF5C396 and applying polling to the other units at the sacrifice of increased overall current consumption resulting from constant system operation.

(2) Re-designing driver software to assign different IRQn pins to interrupt request signals derived from the PC card status change for each IC core at the sacrifice of additional recourse to the IRQn pins which are originally deficient as resources.

(3) Connecting the IRQn pins as shown in the diagram below at the sacrifice of additional hardware installation. Basically, the IRQn pins for assigning the same IRQ number to interrupt request signals derived from the PC card status change would be sufficient to implement the hardware configuration shown in the diagram below. In any ordinary system, however, the same IRQ number cannot always be assigned to interrupt request signals derived from the PC card status change, resulting in many cases where circuit change cannot be confined to the single IRQn pin.



Notice
Under the supply voltage of 3.3V, diode selection requires sufficient care to regulate a voltage drop to a small value.

SOFTWARE DESIGN CONSIDERATIONS

1. Confirmation of Access to Internal Registers

The RF5C296 and the RF5C396 contains about fifty 8bit internal registers. One of these internal registers, the Identification and Revision Register (Index : 00h), which is intended for only reading operation and fixed at 83h, is useful for confirming access to the other internal registers.

2. Identification of PC Card Types

One of the initial requirements in inserting the PC card is to identify whether it is the I/O card or the memory card. Such PC card types can be identified by bit5 in the Interrupt and General Control Register (Index : 03h). This bit indicates the I/0 card and the memory card when set to “1” and “0” , respectively.

3. Address Mapping and Address Window Setting

The RF5C296 and the RF5C396 are designed to interface between the CPU bus, such as the ISA bus, and the PC card bus. Unlike ordinary ICs, therefore, these ICs provides address mapping mainly to establish a correspondence between the CPU bus and the PC card bus.

In view of such differences, therefore, this section provides separate description of “I/O address mapping” and “memory address mapping”.

3.1 I/O Address Space

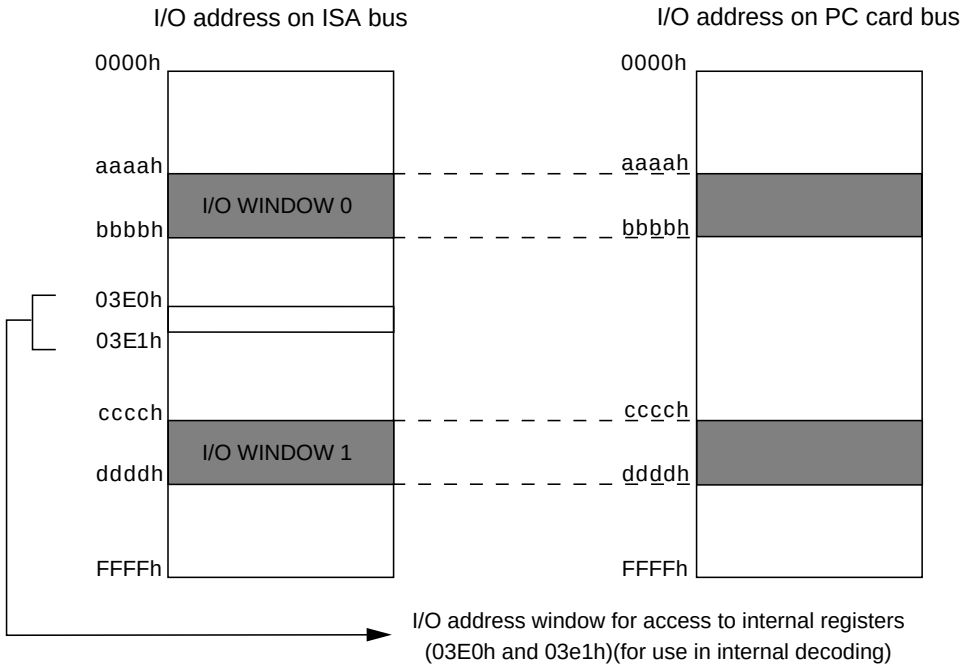
The I/O address space occupies 64kB ranging from “0000h” to “0FFFFh” on the ISA bus. Similarly, the I/O address space occupies 64kB ranging from “0000h” to “0FFFFh” on the PC card bus, too.

The RF5C296 is capable of mapping any given two I/O address windows (ranges) on the ISA bus to the I/O address windows on the PC card bus in units of 1 bytes for each PC card slot in such a manner as to ensure address matching between the ISA bus and the PC card bus.

An I/O address window can be set by setting the low-order 8bits of its starting address in the I/O Address n Start Low Byte Register (Index : 08h (I/O Window 0) and 0Ch (I/O Window 1)) and the high-order 8bits in the I/O Address n Start High Byte Register (Index : 09h (I/O Window 0) and 0Dh (I/O Window 1)) while setting the low-order 8bits of its ending address in the I/O Address n Stop Low Byte Register (Index : 0Ah (I/O Window 0) and 0Eh (I/O Window 1)) and the high-order 8bits in the I/O Address n Stop High Byte Register (Index : 0Bh (I/O Window 0) and 0Fh (I/O Window 1)).

The RF5C296 provides I/O address mapping as shown in the figure below :

• I/O Address Mapping by RF5C296



In the above figure, addresses “03E0h” and “03E1h” form an internal address space for use in internal decoding.

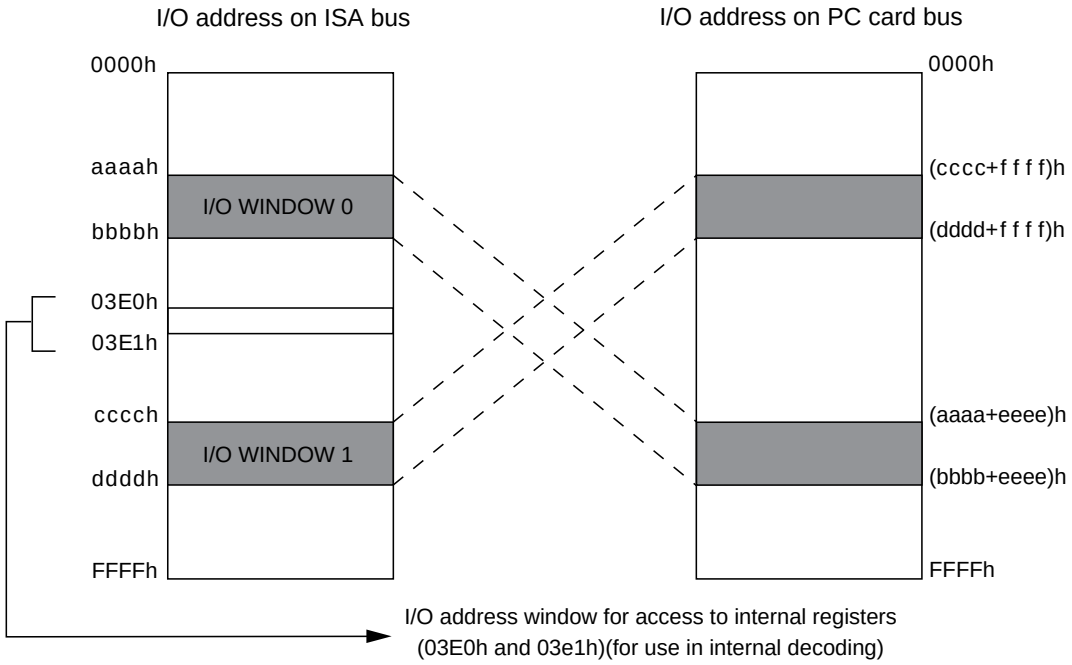
On the other hand, the RF5C396 is capable of I/O address mapping in such a manner as to ensure I/O address mismatching between the ISA bus and the PC card bus.

The above-described settings of the I/O Address n Start/Stop Low/High Byte Registers for the RF5C296 can be added to the settings of the Card I/O Offset Address n Low/High Byte Registers (Index : 36h (Low-byte Window 0), 37h (High-byte Window 0), 38h (Low-byte Window 1), and 39h (High-byte Window 1)) to form two's complement numbers representing I/O addresses on the PC card bus.

The Card I/O Offset Address n Low/High Byte Registers, which always default to “00h”, may be omitted from setting to ensure I/O address matching between the ISA bus and the PC card bus in the same manner as for the RF5C296.

The RF5C396 provides I/O address mapping as shown in the figure below :

• I/O Address Mapping by RF5C296



The settings of the internal registers relating to I/O address window setting are shown in the table on the next page. For details on the individual internal registers, see “INTERNAL REGISTERS”.

• I/O Address Window Setting

		Window 0	Window 1
Start Address	Index	09h : bit7 to 0 08h : bit7 to 0	0Dh : bit7 to 0 0Ch : bit7 to 0
	These bits can be used to specify the starting address of the applicable I/O address window.		
Stop Address	Index	0Bh : bit7 to 0 0Ah : bit7 to 0	0Fh : bit7 to 0 0Eh : bit7 to 0
	These bits can be used to specify the ending address of the applicable I/O address window.		
Off Set Address (Only RF5C396)	Index	37h : bit7 to 0 36h : bit7 to 0	39h : bit7 to 0 38h : bit7 to 0
	These bits can be used to specify the offset address of the applicable I/O address window.		
Wait State	Index	07h : bit3	07h : bit7
	These bits can be used to specify the one wait state (4SYSCLK) 16bit I/O cycle and the standard 16bit I/O cycle when set to "1" and "0", respectively. The 16bit I/O cycle is unavailable in zero wait state form.		
Zero Wait State	Index	07h : bit2	07h : bit6
	These bits can be used to specify the zero wait state 8bit I/O cycle rendering the ZEROWS# pin signal active and the standard 8bit I/O cycle when set to "1" and "0", respectively.		
Data Size	Index	07h : bit0	07h : bit4
	These bits can be used to specify the 8bit mode and the 16bit mode when set to "0" and "1", respectively.		
IOCS16# Source	Index	07h : bit1	07h : bit5
	These bits can be used to specify the dependence of the IOCS16# pin signal on the IOIS16# pin signal from the PC card and on the Data Size Bit when set to "1" and "0", respectively.		
Enable	Index	06h : bit6	06h : bit7
	These bits can be used to specify rendering the applicable I/O window active when set to "1".		

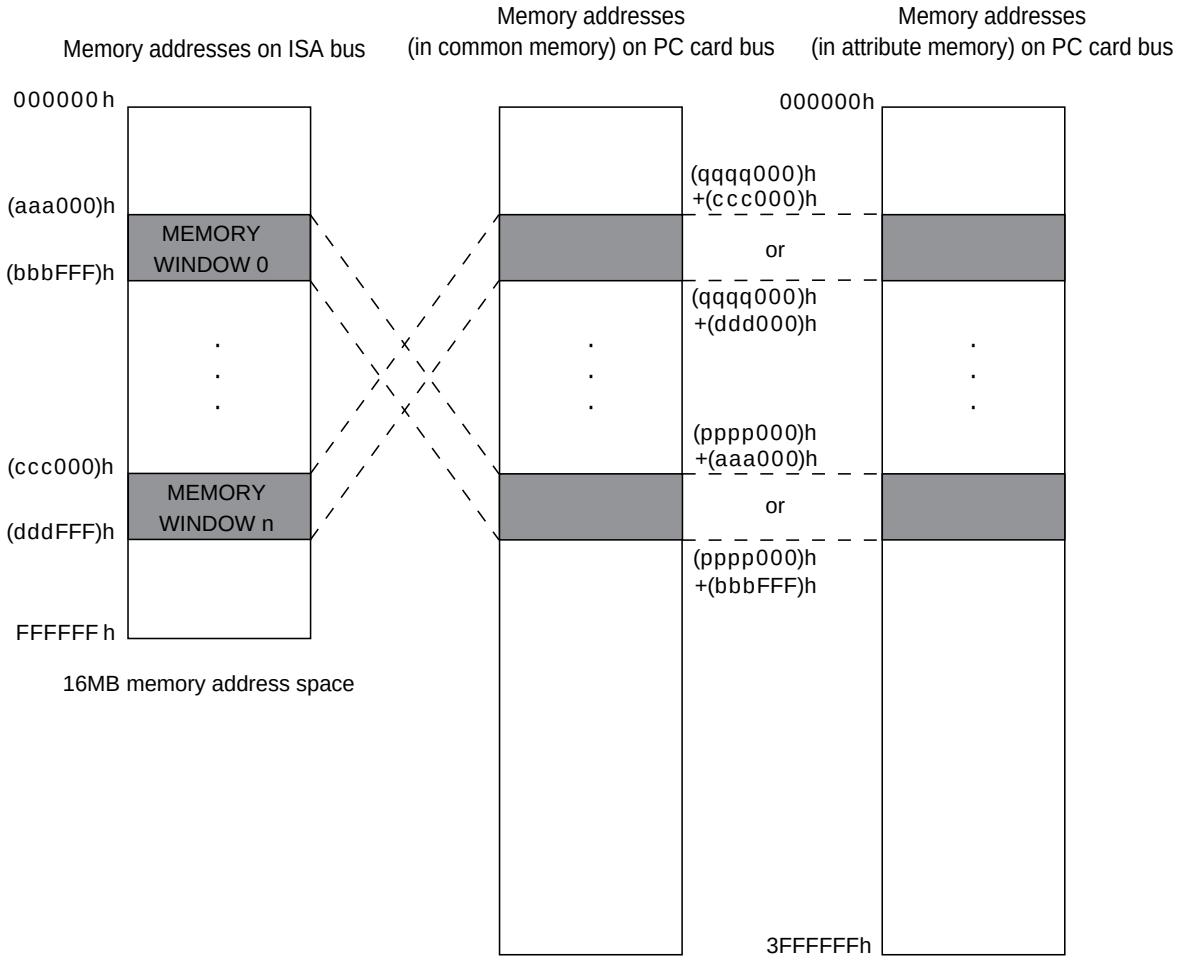
The memory address space occupies 16MB ranging from "000000h" to "0FFFFFFh" on the ISA bus. On the contrary, the memory address space occupies 64MB ranging from "0000000h" to "3FFFFFFh" on the PC card bus.

The RF5C296 and the RF5C396 are capable of mapping any given five memory address windows (ranges) on the ISA bus to the memory address windows on the PC card bus in units of 4kB for each PC card slot. On the ISA bus, each memory address window ranges from the starting address specified by the System Memory Address n Mapping Start High/Low Byte Registers to the ending address specified by the System Memory Address n Mapping Stop High/Low Byte Registers. On the PC card bus, each memory address window equals to its equivalent on the ISA bus plus the setting of the Card Memory Offset Address n Low Byte Register (forming a two's complement number).

Particularly, on the PC card bus, there are two types of memory available : the common memory and the attribute memory, which can be selected by the Card Memory Offset Address n High/Low Byte Registers.

The common memory and the attribute memory are used mainly for ordinary access and for storage of such data as PC card information, respectively. During access to the attribute memory, the REG# pin signal is held at "L".

The RF5C296 and RF5C396 provide memory address mapping as shown in the figure below :



In the above figure, addresses "(aaa000)h" and "(ccc000)h" can be set in the System Memory Address n Mapping Start High/Low Byte Registers, addresses "(bbbFFF)h" and "(dddFFF)h" in the System Memory Address n Mapping Stop High/Low Byte Registers, and addresses "(pppp000)h" and "(qqqq000)h" in the Card Memory Offset Address n High/Low Byte Registers.

The settings of the internal registers relating to memory address window setting are shown in the table below. For details on the individual internal registers, see "INTERNAL REGISTERS".

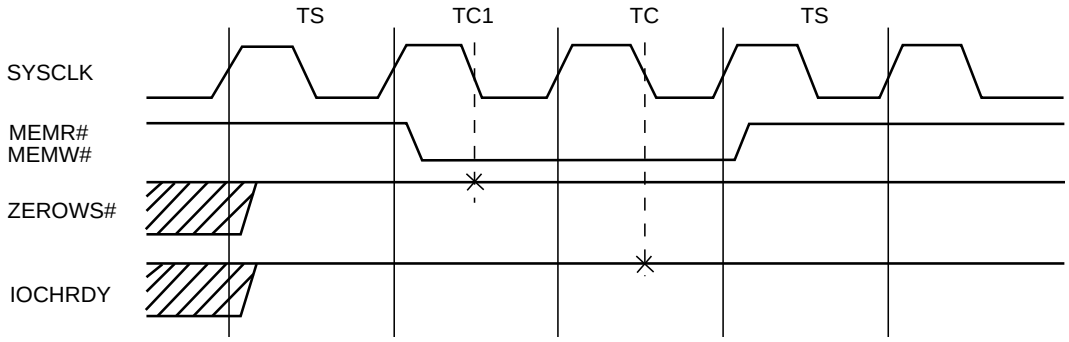
• Memory Address Window Setting

<table>
<tr><th colspan="2"></th><th>Window 0</th><th>Window 1</th><th>Window 2</th><th>Window 3</th><th>Window 4</th></tr>
<tr><td rowspan="2">Start Address</td><td>Index</td><td>11h : bit3 to 0
10h : bit7 to 0</td><td>19h : bit3 to 0
18h : bit7 to 0</td><td>21h : bit3 to 0
20h : bit7 to 0</td><td>29h : bit3 to 0
28h : bit7 to 0</td><td>31h : bit3 to 0
30h : bit7 to 0</td></tr>
<tr><td colspan="6">These bits can be used to specify the starting address of the applicable memory address window. (A23 to A12)</td></tr>
<tr><td rowspan="2">Stop Address</td><td>Index</td><td>13h : bit3 to 0
12h : bit7 to 0</td><td>1Bh : bit3 to 0
1Ah : bit7 to 0</td><td>23h : bit3 to 0
22h : bit7 to 0</td><td>2Bh : bit3 to 0
2Ah : bit7 to 0</td><td>33h : bit3 to 0
32h : bit7 to 0</td></tr>
<tr><td colspan="6">These bits can be used to specify the ending address of the applicable memory address window. (A23 to A12)</td></tr>
<tr><td rowspan="2">Offset Address</td><td>Index</td><td>15h : bit5 to 0
14h : bit7 to 0</td><td>1Dh : bit5 to 0
1Ch : bit7 to 0</td><td>25h : bit5 to 0
24h : bit7 to 0</td><td>2Dh : bit5 to 0
2Ch : bit7 to 0</td><td>35h : bit5 to 0
34h : bit7 to 0</td></tr>
<tr><td colspan="6">These bits can be used to specify the offset address of the applicable memory address window. (A25 to A12)</td></tr>
<tr><td rowspan="2">Zero Wait State</td><td>Index</td><td>11h : bit6</td><td>19h : bit6</td><td>21h : bit6</td><td>29h : bit6</td><td>31h : bit6</td></tr>
<tr><td colspan="6">These bits can be used to specify zero wait state access when set to "1" in the 8bit mode, giving first priority to the WAIT# pin signal from the PC card.</td></tr>
<tr><td rowspan="2">Data Size</td><td>Index</td><td>11h : bit7</td><td>19h : bit7</td><td>21h : bit7</td><td>29h : bit7</td><td>31h : bit7</td></tr>
<tr><td colspan="6">These bits can be used to specify 8bit access and 16bit access when set to "0" and "1", respectively.</td></tr>
<tr><td rowspan="2">Wait State</td><td>Index</td><td>13h : bit7 to 6</td><td>1Bh : bit7 to 6</td><td>23h : bit7 to 6</td><td>2Bh : bit7 to 6</td><td>33h : bit7 to 6</td></tr>
<tr><td colspan="6">These bits can be used to specify memory access cycles, giving first priority to the WAIT# pin signal from the PC card.
<table>
<tr><th>bit7</th><th>bit6</th><th># of additional cycle</th><th># of SYSCLK per access</th></tr>
<tr><td>0</td><td>0</td><td>Standard 16bit cycle
(additional cycle is "0".)</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>6</td></tr>
</table></td></tr>
<tr><td rowspan="2">Write Protect</td><td>Index</td><td>15h : bit7</td><td>1Dh : bit7</td><td>25h : bit7</td><td>2Dh : bit7</td><td>35h : bit7</td></tr>
<tr><td colspan="6">These bits can be used to specify write protection on memory.</td></tr>
<tr><td rowspan="2">Reg Active</td><td>Index</td><td>15h : bit6</td><td>1Dh : bit6</td><td>25h : bit6</td><td>2Dh : bit6</td><td>35h : bit6</td></tr>
<tr><td colspan="6">These bits can be used to specify access to the attribute memory in the IC card when set to "1".</td></tr>
</table>

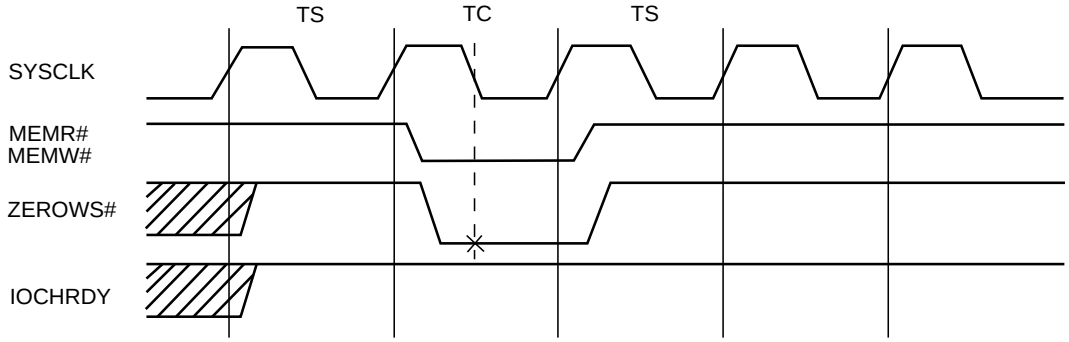
		Window 0	Window 1	Window 2	Window 3	Window 4
MEMCS16#	Index	06h : bit5				
	This bit can be used to specify the generation of the MEMCS16# pin signal through decoding the A23 to A17 pin signals and through decoding the A23 to A12 pin signals when set to “0” and “1”, respectively.					
Window Enable	Index	06h : bit0	06h : bit1	06h : bit2	06h : bit3	06h : bit4
	These bits can be used to specify rendering the applicable memory address window active when set to “1”.					

To enhance understanding of memory access cycles, three types of 16bit memory access cycles are shown in the timing charts below :

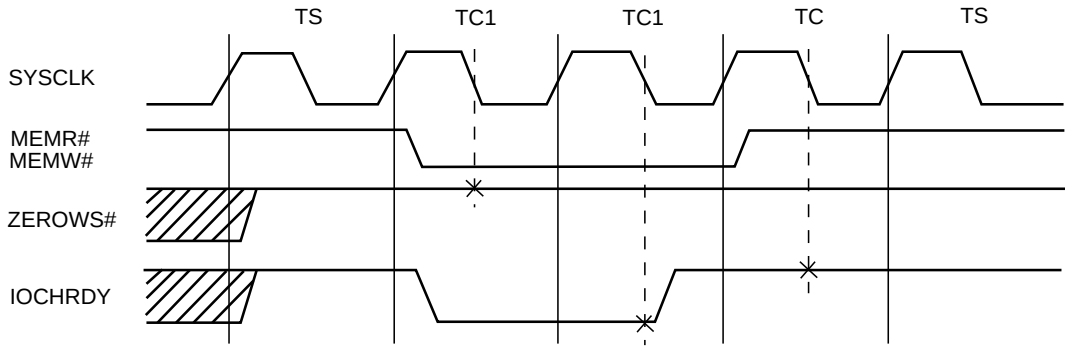
(1) Standard Cycle (3 SYSCLK Cycle)



(2) Zero Wait State Cycle (2 SYSCLK Cycle)



(3) One Wait State Cycle (4 SYSCLK Cycle)



A two or three wait state memory access cycle can be implemented by adding the TC1 in the one wait state memory access cycle of (3). The 16bit memory access cycle is identical to the 16bit I/O cycle in terms of the output timing for the IOCHRDY pin signal except that the latter is unavailable in zero wait state form.

4. Interrupt Processing

The RF5C296 and the RF5C396 generate interrupts derived from the following sources :

For I/O Card : Interrupts derived from the IREQ# pin status change :
PC Card status change : CD1# and/or CD2# pin status change
STSCHG# pin status change (when bit7 is set interrupt and General Control Register (Index : 03h))
5VDET/GPI pin status change

For Memory Card : PC Card status change : CD1# and/or CD2# pin status change
BVD1 and/or BVD2 pin status change
READY#/BUSY# pin status change
5VDET/GPI pin status change

As shown above, interrupt sources fall into two types : interrupts derived from the IREQ# pin and the PC card status change.

Meanwhile, interrupt output destinations available on the ISA bus are the IRQn pins (n = 3, 4, 5, 7, 9, 10, 11, 12, 14, and 15), the INTR# pin, and the RI_OUT# pin (only for interrupts derived from the CD1# and/or CD2# pin status change as specified by bit4 (Card Detect Resume Enable Bit) in the Card Detect and General Control Register (Index : 16h)).

Some of the internal registers provide the following four types of interrupt control :

(1) Control over interrupt sources
(2) Control over interrupt output destinations
(3) Control over interrupt output waveforms
(4) Control over interrupt cancellation

Of the above four types of interrupt control, (1) control over interrupt sources is described in “5. Card Slot Pin Status Indication and Register Setting” while the other three types are described below.

4.1 Control over Interrupt Output Destinations

Interrupts derived from the IREQ# pin particularly for the I/O card can be assigned to the IRQn pins as their output destinations by setting bits3 to 0 in the Interrupt and General Control Register (Index : 03h) as shown in the first table on the next page.

Interrupts derived from the PC card status change for both the I/O card and the memory card can be assigned to the IRQn pins or the INTR# pin as their output destinations by setting bits7 to 4 in the Card Status Interrupt Configuration Register (Index : 05h) or bit4 (INTR# Enable Bit) in the Interrupt and General Control Register (Index : 03h) as shown in the second table on the next page.

Incidentally, the IRQn pins are caused to transition to high impedance unless assigned as interrupt output destinations.

As described above, interrupts derived from the CD1# and/or CD2# pin status change among interrupts derived from the PC card status change can be assigned to the RI_OUT# pin as their output destination.

More specifically, the RI_OUT# pin output can be generated upon occurrence of the CD1# and/or CD2# pin status change by setting bit4 (Card Detect Resume Enable Bit) to “1” in the Card Detect and General Control Register (Index : 16h) and then setting bit3 (Card Detect Enable Bit) to “1” in the Card Status Interrupt Configuration Register (Index : 05h). For details on these registers, see their respective description in “INTERNAL REGISTERS”.

• Output Destination Settings for Interrupts Derived from IREQ#

bit3	bit2	bit1	bit0	IRQn Selection
0	0	0	0	IRQ not Selected
0	0	1	1	IRQ3 Enabled
0	1	0	0	IRQ4 Enabled
0	1	0	1	IRQ5 Enabled
0	1	1	1	IRQ7 Enabled
1	0	0	1	IRQ9 Enabled
1	0	1	0	IRQ10 Enabled
1	0	1	1	IRQ11 Enabled
1	1	0	0	IRQ12 Enabled
1	1	1	0	IRQ14 Enabled
1	1	1	1	IRQ15 Enabled

• Output Destination Setting for Interrupts Derived from PC Card Status Change

INTR# Enable bit	bit7	bit6	bit5	bit4	IRQn Selection
0	0	0	0	0	IRQ not Selected
0	0	0	1	1	IRQ3 Enabled
0	0	1	0	0	IRQ4 Enabled
0	0	1	0	1	IRQ5 Enabled
0	0	1	1	1	IRQ7 Enabled
0	1	0	0	1	IRQ9 Enabled
0	1	0	1	0	IRQ10 Enabled
0	1	0	1	1	IRQ11 Enabled
0	1	1	0	0	IRQ12 Enabled
0	1	1	1	0	IRQ14 Enabled
0	1	1	1	1	IRQ15 Enabled
1	×	×	×	×	redirected to INTR#

4.2 Control over Interrupt Output Waveforms

Interrupts derived from the IRQn pins represent different output waveforms in the Level Mode and the Edge Mode. In the Level Mode, the IRQn pin outputs are caused to transition from high impedance to "L" upon interrupt generation and vice versa upon completion of interrupt processing. In the Edge Mode, the IRQn pin outputs are caused to transition from low level to "H" upon interrupt generation and vice versa upon completion of interrupt processing. The Level Mode and the Edge Mode can be specified by setting bit1 (Level Mode Interrupt Enable Bit) to "1" and "0", respectively, in the Global Control Register (Index : 1Eh).

Of the IRQn pin outputs, the IRQ14 pin output alone allows exceptional waveform control, which can be specified by setting bit3 (IRQ14 Pulse Mode Enable Bit) to "1" in the Global Control Register (Index : 1Eh). Namely, interrupts derived from the IRQ14 pin represent output waveforms in the Level Mode even when the Edge Mode is specified by setting bit1 (Level Mode Interrupt Enable Bit) to "0" in the Global Control Register (Index : 1Eh).

Meanwhile, the INTR# pin output is caused to transition from high level to "L" for the duration of three clock pulses upon interrupt generation and vice versa upon completion of interrupt processing.

4.3 Control over Interrupt Cancellation

Interrupts derived from the IREQ# pin can be canceled by first canceling interrupts on the PC card bus with the IREQ# pin caused to transition to low level and then canceling interrupts on the ISA bus with the IREQ# pin caused to transition to "H".
Interrupts derived from the PC card status change can be canceled by the following two methods :

(1) Reading the Card Status Change Register (Index : 04h)
(2) Setting applicable bits to "1" in the Card Status Change Register (Index : 04h) provided that bit2 (Explicit Write Back Card Status Change Acknowledge Bit) is set to "1" in the Global Control Register (Index : 1Eh).

5. Card Slot Pin Status Indication and Register Setting

The RF5C296 and the RF5C396 have the function of indicating the status of the pins on the PC card slot in various forms to the CPU. This function falls into the following four types :

(1) Reading back the pins on the PC card slot
(2) Making settings upon occurrence of any pin status change on the PC card slot
(3) Generating interrupts upon occurrence of any pin status change on the PC card slot
(4) Performing other processes upon occurrence of any pin status change on the PC card slot

The internal registers contained in the RF5C296 and the RF5C396 are grouped according to their functions to facilitate such processes as interrupt processing. While the internal registers are described in detail under classification by function in "INTERNAL REGISTERS", they are described briefly under classification by pin on the PC card slot in this section.

5.1 CD1# and CD2# Pins

The CD1# and CD2# pins are grounded within the PC card and pulled up on the PC card slot. Both the CD1# and CD2# pins are caused to transition to "L" upon insertion of the PC card into the PC card slot. Note that some of the internal registers are designed to control the CD1# and CD2# pins upon occurrence of both the CD1# and CD2# status change and others upon occurrence of either the CD1# or CD2# status change.

· Interface Status Register (Index : 01h) : bit3 (for the CD2# pin) and bit2 (for the CD1# pin)

These bits can be used to specify reading back of the CD1# and CD2# pin inputs.

· Card Status Change Register (Index : 04h) : bit3 (Card Detect Change bit)

This bit will be set to "1" upon occurrence of either the CD1# or CD2# pin status change (insertion or removal of the PC card into or from the PC card slot).

· Card Status Interrupt Configuration Register (Index : 05h) : bit3 (Card Detect Enable bit)

This bit can be used to specify generation of interrupts from the IRQn pins or the INTR# pin upon occurrence of either the CD1# or CD2# pin status change.

· Card Detect and General Control Register (Index : 16h) : bit4 (Card Detect Resume Enable bit)

This bit can be used to specify generation of interrupts from the RI_OUT# pin upon occurrence of either the CD1# or CD2# pin status change.

· Card Detect and General Control Register (Index : 16h) : bit5 (Software Card Detect Interrupt bit)

This bit can be set to "1" to specify software-controlled generation of interrupts derived from the CD1# and/orCD2# pin status change.

· Card Detect and General Control Register (Index : 16h) : bit1 (Configuration Reset Enable bit)

This bit can be set to "1" to specify generation of reset pulses upon transition of both the CD1# and CD2# pins to "H" (removal of the PC card from the PC card slot), thus resetting the internal registers relating to address windows or interrupts. (For details on the internal registers thus reset, see "1. Chip Control" in "INTERNAL REGISTERS".)

5.2 BVD1 and BVD2 Pins

The BVD1 and BVD2 pins function as input pins for battery voltage detection when the PC card is the memory card (bit5 is set to "0" in the Interrupt and General Control Register (Index : 03h)). Based on output signals from the PC card, the BVD1 and BVD2 pin signals are defined as shown in the table below :

BVD1	BVD2	Battery voltage conditions
0	0	Faulty battery voltage conditions requiring battery replacement and not guaranteeing data retention.
0	1	Faulty battery voltage conditions requiring battery replacement and not guaranteeing data retention.
1	0	Faulty battery voltage conditions requiring battery replacement but guaranteeing data retention.
1	1	Normal battery voltage conditions.

· Interface Status Register (Index : 01h) : bit1 (for the BVD2 pin) and bit0 (for the BVD1 pin)

These bits can be used to specify reading back the BVD1 and BVD2 pins.

· Card Status Change Register (Index : 04h) : bits1 and 0

Bit1 will be se to "1" upon detection of the battery warning condition, respectively.

Bit0 will be set to "0" upon detection of the battery dead condition, respectively.

· Card Status Interrupt Configuration Register (Index : 05h) : bit1 and bit0

Bit1 can be set to "1" to specify generation of interrupts upon detection of the battery warning conditions, respectively.

Bit0 can be set to "1" to specify generation of interrupts upon detection of the battery dead conditions, respectively.

5.3 STSCHG#/RI# Pin

The STSCHG#/RI# pin functions as an input pin for the Card Status Change# and Ring Indicate# signals when the PC card is the I/O card (bit5 is set to "1" in the Interrupt and General Control Register (Index : 03h)).

The internal registers described below also function as those relating to the STSCHG#/RI# pin status on the condition that the PC card is the I/O card.

· Interface Status Register (Index : 01h) : bit0 (Battery Voltage Detect 1 Bit)

This bit can be used to specify reading back the STSCHG#/RI# pin.

· Card Status Change Register (Index : 04h) : bit0

This bit will be set to "1" upon transition of the Card Status Change# and RI# signals to "0" when bit7 (Ring Indicate Enable Bit) is set to "0" in the Interrupt and General Control Register (Index : 03h).

· Interrupt and General Control Register (Index : 03h) : bit7 (Ring Indicate Enable Bit)

This bit can be set to "1" to specify output of the RING INDICATE# signal to the RI_OUT# pin.

5.4 5VDET/GPI Pin

The GPI pin, as its full name "general-purpose input pin" suggests, functions as an input pin for general purpose use. Further, it can also be connected to the VS1# pin on the PC card slot to detect the 5V PC card. (For details, see "3.2 5VDET/GPI and VS1# Pins" in "3. Connections to PCMCIA Slot" in "HARDWARE DESIGN CONSIDERATIONS".)

· Interface Status Register (Index : 01h) : bit7

This bit can be used to specify reading back the 5VDET/GPI pin.

· Card Status Change Register (Index : 04h) : bit4 (GPI Change Bit)

This bit will be set to "1" upon generation of interrupts derived from the GPI pin status change when bit2 (GPI Enable Bit) is set to "1" in the Card Detect and General Control Register (Index : 16h).

· Card Detect and General Control Register (Index : 16h) : bit3 (GPI Transmission Control Bit)

This bit can be set to "1" and "0" to specify generation of interrupts upon transition of the GPI pin from "H" to "L" and vice versa, respectively.

· Card Detect and General Control Register (Index : 16h) : bit2 (GPI Enable Bit)

This bit can be used to enable interrupts from the GPI pin and set to "1" to specify generation of interrupts upon the GPI input status change.

5.5 READY#/BUSY# Pins

The internal registers described below function as those relating to the READY#/BUSY# pin status on the condition that the PC card is the memory card.

· Interface Status Register (Index : 01h) : bit5 (Ready/Busy# Bit)

This bit can be set to "0" and "1" to specify reading back the READY#/BUSY# pins, respectively (specify reading back the IREQ# pin when the PC card is the I/O card).

· Card Status Change Register (Index : 04h) : bit2 (Ready Change Bit)

This bit will be set to "1" upon transition of the READY#/BUSY# pins from "L" to "H".

· Card Status Interrupt Configuration Register (Index : 05h) : bit2 (Ready Enable Bit)

This bit can be set to "1" to specify generation of interrupts upon transition of the READY#/BUSY# pins from "L" to "H".

5.6 Other Pins

WP Pin

· Interface Status Register (Index : 01h) : bit4 (Memory Write Protect Bit)

This bit an be used to specify reading back the WP pin. Note that write protection will not be enabled even when the WP pin is set to "1" unless Write Protect Bit is set to "1" for each memory address window.

Power Supply Status

· Interface Status Register (Index : 01h) : bit6 (PC card Power Active Bit)

This bit an be used to indicate the status of power supply to the PC card slot and set to "0" and "1" to indicate the power-off state (in which both the VCC3VEN# and VCC5VEN# pins are held at high level) and the power-on state, respectively.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Condition	Ratings	Unit
V_{CC}	Power Supply Voltage	GND=0V	–0.3 to 7	V
Vte	Terminal Voltage	GND=0V	–0.3 to V_{CC}+0.3	V
Topr	Operating Temperature		–40 to +85	˚C
Tstg	Storage Temperature		–55 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

DC ELECTRICAL CHARACTERISTICS (Vcc=5V)

Vcc=5V±10%, Ta=0 to 70˚C

Symbol	Item	Measuring Condition	Limits			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" Input Voltage		2.0		V_{CC}+0.3	V
V_{IL}	"L" Input Voltage		–0.3		0.8	V
V_{OH1}*1	"H" Output Voltage	I_{OH}=–12mA	2.4			V
V_{OH2}*2	"H" Output Voltage	I_{OH}=–8mA	2.4			V
V_{OH3}*3	"H" Output Voltage	I_{OH}=–4mA	2.4			V
V_{OL1}*1	"L" Output Voltage	I_{OL}=12mA			0.4	V
V_{OL2}*2	"L" Output Voltage	I_{OL}=8mA			0.4	V
V_{OL3}*3	"L" Output Voltage	I_{OL}=4mA			0.4	V
V_{OL4}*4	"L" Output Voltage	I_{OL}=16mA			0.4	V
I_{ILK}	Input Leakage Current	V_{IN}=0 to V_{CC}	–10		+10	µA
I_{IL1}*5	Input Current (Pull-up)	V_{IN}=0	–200	–50		µA
I_{IL2}*6	Input Current (Pull-down)	V_{IN}=V_{CC}		25	100	µA
I_{IL3}*7	Input Current (Pull-down)	V_{IN}=V_{CC}		50	200	µA
I_{OZ}	Off Output Leakage Current	V_{OUT}=0 to V_{CC}	–10		+10	µA
Iccstd	Stand-by Current	V_{IN}=0V or V_{CC}			10	µA
I_{CC}	Operating Current	V_{IN}=0V or V_{CC} (V_{CC}=5V) V_{CC}, fsysclk=10MHz	RF5C296		12	mA
			RF5C396		20	

*1) SD15 to SD0, ZEROWS#
*2) IRQn, CA25 to CA0, CD15 to CD0, CE1#, CE2#, CIORD#, CIOWR#, OE#, WE#
*3) SPKROUT#, RI_OUT#, INTR#, GPI, VCC3EN#, VCC5EN#, VPP_EN0, VPP_EN1, REG#, RESET
*4) IOCS16#, MEMCS16#, IOCHRDY
*5) GPI
*6) CD15 to CD0
*7) RESETDRV

DC ELECTRICAL CHARACTERISTICS (Vcc=3.3V)

Vcc=3.3V±0.3V, Ta=0 to 70°C

Symbol	Item	Measuring Condition	Limits			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" Input Voltage		2.0		V_{CC}+0.3	V
V_{IL}	"L" Input Voltage		–0.3		0.6	V
V_{OH1}*1	"H" Output Voltage	I_{OH}=–6mA	2.4			V
V_{OH2}*2	"H" Output Voltage	I_{OH}=–4mA	2.4			V
V_{OH3}*3	"H" Output Voltage	I_{OH}=–2mA	2.4			V
V_{OL1}*1	"L" Output Voltage	I_{OL}=6mA			0.4	V
V_{OL2}*2	"L" Output Voltage	I_{OL}=4mA			0.4	V
V_{OL3}*3	"L" Output Voltage	I_{OL}=2mA			0.4	V
V_{OL4}*4	"L" Output Voltage	I_{OL}=8mA			0.4	V
I_{ILK}	Input Leakage Current	V_{IN}=0 to V_{CC}	–10		+10	µA
I_{IL1}*5	Input Current (Pull-up)	V_{IN}=0	–100	–25		µA
I_{IL2}*6	Input Current (Pull-down)	V_{IN}=V_{CC}		10	50	µA
I_{IL3}*7	Input Current (Pull-down)	V_{IN}=V_{CC}		25	100	µA
I_{OZ}	Off Output Leakage Current	V_{OUT}=0 to V_{CC}	–10		+10	µA
Iccstd	Stand-by Current	V_{IN}=0V or V_{CC}			10	µA
I_{CC}	Operating Current	V_{IN}=0V or V_{CC} (V_{CC}=3.3V) V_{CC}, fsysclk=10MHz	RF5C296		6	mA
			RF5C396		10	

*1) SD15 to SD0, ZEROWS#
*2) IRQn, CA25 to CA0, CD15 to CD0, CE1#, CE2#, CIORD#, CIOWR#, OE#, WE#
*3) SPKROUT#, RI_OUT#, INTR#, GPI, VCC3EN#, VCC5EN#, VPP_EN0, VPP_EN1, REG#, RESET
*4) IOCS16#, MEMCS16#, IOCHRDY
*5) GPI
*6) CD15 to CD0
*7) RESETDRV

AC ELECTRICAL CHARACTERISTICS

1. 8/16bit Memory Cycle

V_{CC}=5V±10%(3.3V±0.3V)*2, Ta=0 to 70˚C, C_L=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
Tckl	SYSCLK “L” pulse width	45		ns
Tckh	SYSCLK “H” pulse width	45		ns
T1	LA <23 : 17> setup time to BALE falling	45		ns
T2	BALE pulse width	50		ns
T3	LA <23 : 17> hold time from BALE	15		ns
T7a	LA <23 : 17>, SA <17 : 12>, SA0 and SBHE# setup time to MEMR#, MEMW#	23		ns
T35	MEMR#, MEMW# active to falling edge of SYSCLK	15		ns
T12	SA <16 : 0> and SBHE# hold from MEMR#, MEMW#	25		ns
T5a	MEMCS16# valid from LA <23 : 17>		40*1	ns
T5b	MEMCS16# valid from SA <16 : 12>		24(35)*1	ns
T6a	MEMCS16# hold from LA <23 : 17>	0		ns
T6b	MEMCS16# tri-state from SA <16 : 12>		24(35)	ns
T6c	MEMCS16# tri-state from LA <23 : 17>		40	ns
T21a	IOCHRDY active from falling edge of SYSCLK		24(35)*1	ns
T20	IOCHRDY low from MEMR#, MEMW#		32*1	ns
T17	ZEROWS# active from SA <16 : 12>		60	ns
T29a	ZEROWS# hold from MEMR#, MEMW#	0		ns
T29b	ZEROWS# tri-state from SA <16 : 12>		55	ns
T29c	ZEROWS# tri-state from MEMR#, MEMW#		35	ns
T41	WAIT# active to IOCHRDY inactive		20(30)*1	ns
T42	WAIT# inactive to IOCHRDY active	0	20(30)*1	ns
T30a	CA <25 : 0> valid delay from LA <23 : 17>, SA <16 : 0>		50	ns
T40	CA <25 : 0> hold from LA <23 : 17>, SA <16 : 0>	5		ns
T32a	OE#, WE# valid from MEMR#, MEMW# with memory delay inhibit		27	ns
T32b	OE#, WE# valid from MEMR#, MEMW# 16bit windows	T35	T35+28	ns
T38	OE#, WE# valid from MEMR#, MEMW active	0	24	ns
T31	CE#, REG# valid from LA <23 : 17>, SA <16 : 0>		47(55)	ns

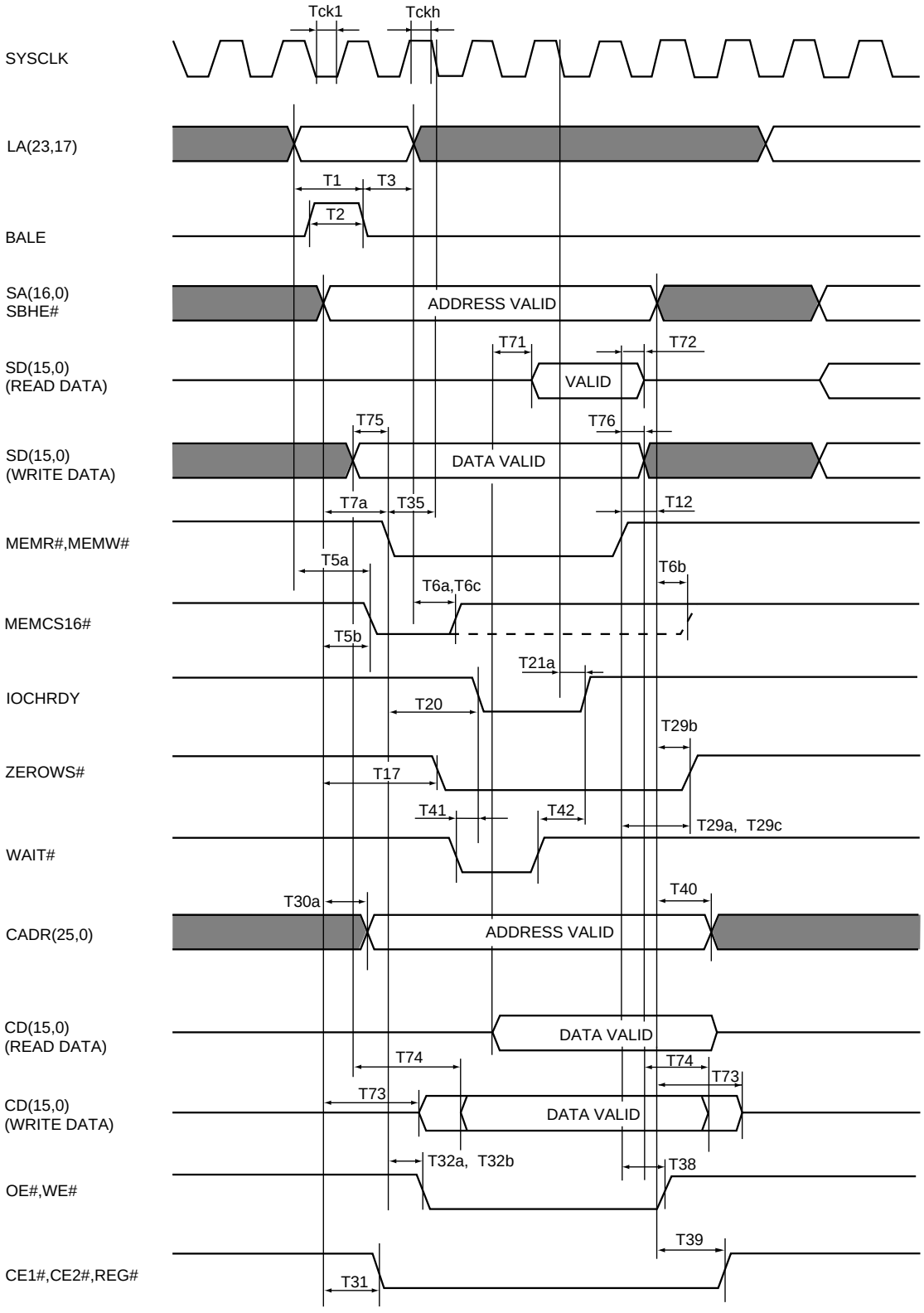
V_{CC}=5V±10%(3.3V±0.3V)*2, Ta=0 to 70°C, CL=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T39	CE#, REG# invalid from LA <23 : 17>, SA <16 : 0>	0	47 (55)	ns
T71	CD <23 : 17> valid delay from SD <15 : 0> when I/O read		50	ns
T72	SD <15 : 0> hold from MEMR#	10		ns
T73	CD <15 : 0> active from LA <23 : 17>, SA <16 : 0>		47 (55)	ns
T74	CD <15 : 0> valid delay from SD <15 : 0> when I/O write		50	ns
T75	SD <15 : 0> setup time from falling edge of MEMW#	0		ns
T76	SD <15 : 0> hold time from MEMW#	25		ns

*1) This Timing assumes a load capacitance of 50pF.

*2) In the above table, the parenthesized specifications apply when Vcc=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether Vcc=5V±10% or 3.3±0.3V.

• 8/16bit Memory Cycle



2. 8/16bit I/O Cycle

V_{CC}=5V±10% (3.3V±0.3V)*2, Ta=0 to 70°C, CL=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T1	LA <23 : 17> setup time from to BALE falling	45		ns
T2	BALE pulse width	50		ns
T45	AEN setup time to IOR#, IOW#	45		ns
T46	AEN hold time to IOR#, IOW#	25		ns
T7	LA <23 : 17>, SA <17 : 0> and SBHE setup time to IOR#, IOW#	45		ns
T12	IOCS16# hold time from SA <15 : 0>	25		ns
T5a	IOCS16# active from LA <23 : 17>		40	ns
T5b	IOCS16# active from SA <16 : 0>		24(35)	ns
T19a	IOCS16# hold time from SA <15 : 0>	0		ns
T19b	IOCS16# tri-state from SA <15 : 0>		40	ns
T20	IOCHRDY low from IOR#, IOW#		32*1	ns
T21	IOCHRDY active from falling edge of SYSCLK		24(35)*1	ns
T41	WAIT# active to IOCHRDY inactive		20(30)*1	ns
T42	WAIT# inactive to IOCHRDY active	0	20(30)*1	ns
T28	ZEROWS# active from 8bit IOR#, IOW#		25 (35)	ns
T29a	ZEROWS# hold time from IOR#, IOW#	0		ns
T29c	ZEROWS# tri-state from IOR#, IOW# active		35	ns
T30b	CA <25 : 0> valid delay from LA <23 : 17>, SA <17 : 0>		50	ns
T40	CA <25 : 0> hold time from LA <23 : 17>, SA<17 : 0>	5		ns
T33	CIORD#, CIOWR# valid from IOR#, IOW#		25	ns
T38	CIORD#, CIOWR# inactive from IOR#, IOW# inactive	0	24	ns
T31a	CE#, REG# valid from LA <23 : 17>, SA <17 : 0>		47 (55)	ns
T31b	CE#, REG# valid from SA <15 : 0> I/O with IOIS16# generated		75	ns
T39	CE#, REG# invalid from LA <23 : 17>, SA <17 : 0>	0	45 (55)	ns
T34	CA <25 : 0> to IOIS16#		35	ns

*1) This Timing assumes a load capacitance of 50pF.
*2) In the above table, the parenthesized specifications apply when V_{CC}=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether V_{CC}=5V±10% or 3.3±0.3V.

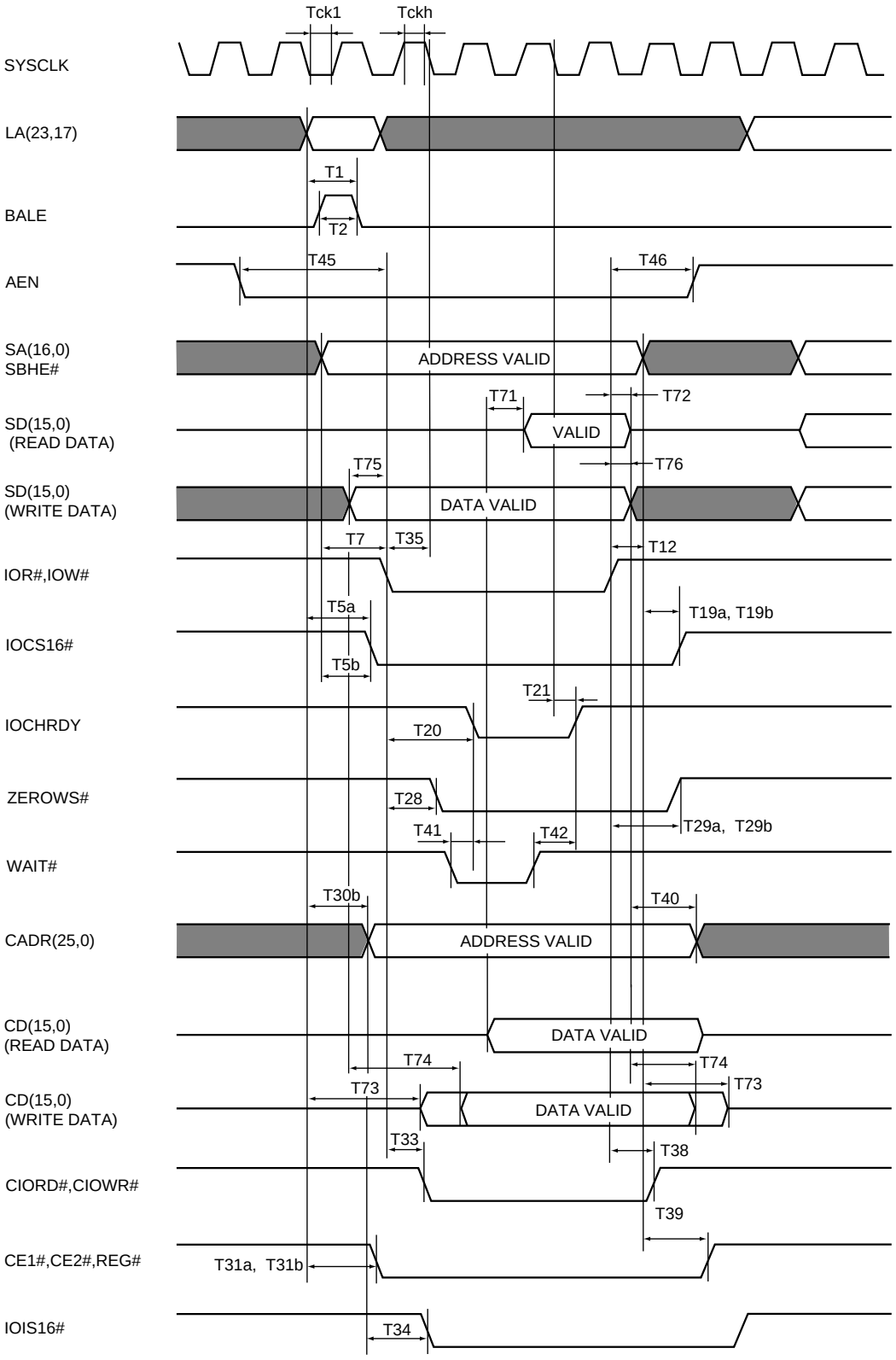
Symbol	Item	Limits		Unit
		MIN.	MAX.	
T71	CD <15 : 0> valid delay from SD <15 : 0> when I/O read		50	ns
T72	SD <15 : 0> hold time IOR#	10		ns
T73	CD <15 : 0> active from LA <23 : 17>, SA <17 : 0>		45 (55)	ns
T74	CD <15 : 0> valid delay from SD <15 : 0> when I/O read		50	ns
T75	SD <15 : 0> setup time to IOW# active	0		ns
T76	SD <15 : 0> hold time IOW#	25		ns

*1) This Timing assumes a load capacitance of 50pF.
*2) In the above table, the parenthesized specifications apply when V_{CC}=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether V_{CC}=5V±10% or 3.3±0.3V.

NOTE

Setup time of data to falling edge of CIOWR# (tdsu) depends on setup time of address to IOW# of system (Stdsu).
tdsu (min.)=Stdsu-30ns.m

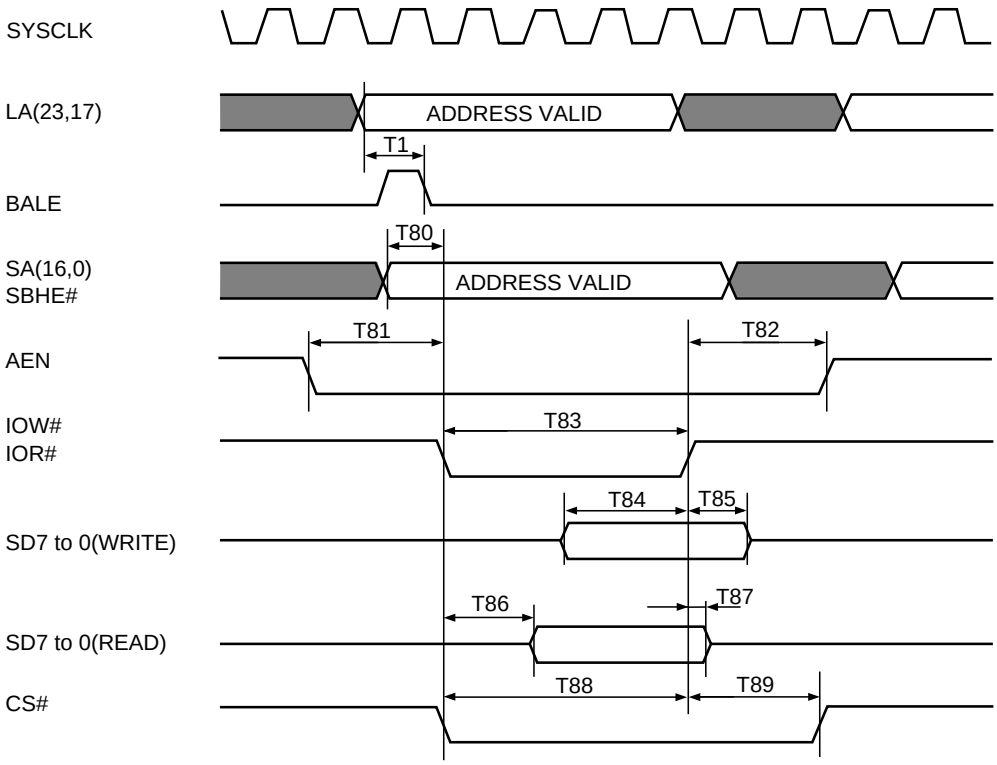
• 8/16bit I/O Cycle



3. Internal 8bits Register Access Cycle

V_{CC}=5V±10%(3.3V±0.3V),Ta=0 to 70°C, CL=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T80	SA <16 : 0>, SBHE# setup time	45		ns
T81	AEN setup time	45		ns
T82	AEN hold time	25		ns
T83	I/O command pulse width	100		ns
T84	SD <7 : 0> write data setup time	40		ns
T85	SD <7 : 0> write data hold time	10		ns
T86	SD <7 : 0> read data delay		70	ns
T87	SD <7 : 0> read data hold time	0		ns
T88	CS# setup time	100		ns
T89	CS# hold time	0		ns

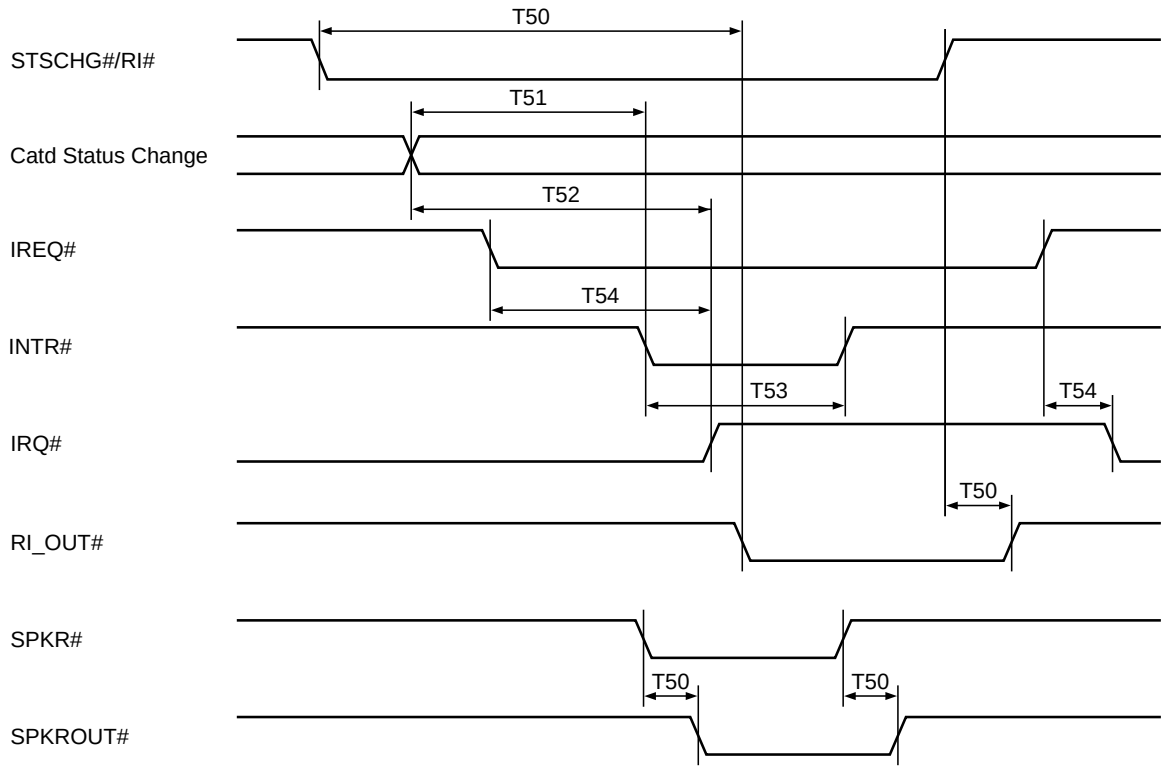


4. Interrupt, Ring Indicate Speaker

V_{CC}=5V±10%(3.3V±0.3V)*1,Ta=0 to 70°C, CL=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T50	RI# to RI_OUT# delay, SPKR# to SPKROUT# delay		30	ns
T51	Card Status Change, INTR# valid delay		2×Tclkp*2	ns
T52	Card Status Change, IRQn valid delay		50	ns
T53	INTR# pulse width	3×Tclkp*2		ns
T54	IREQ# to IRQn delay		50	ns

*1) In the above table, the parenthesized specifications apply when V_{CC}=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether V_{CC}=5V±10% or 3.3±0.3V.
*2) Tclkp means the clock cycle period.



5. Reset from POWERGOOD

Vcc=5V±10%(3.3V±0.3V),Ta=0 to 70˚C, CL=100pF

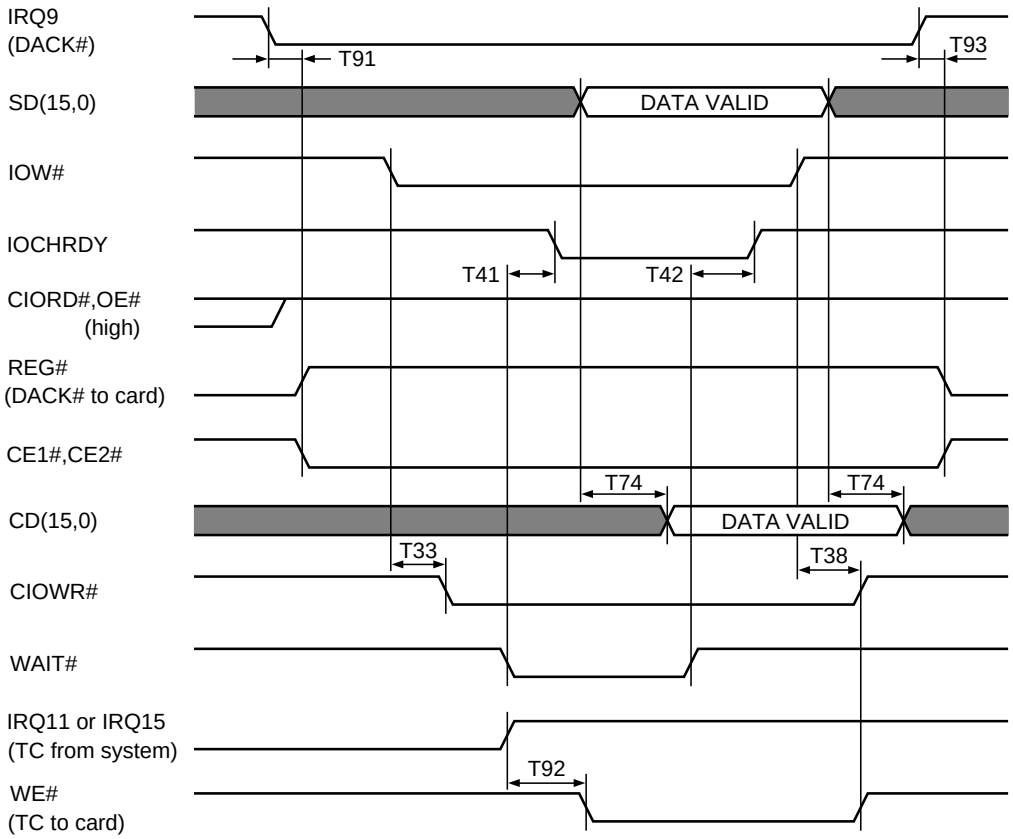
Symbol	Item	Limits		Unit
		MIN.	MAX.	
T60	RESETDRV setup time to POWERGOOD	200		ns
T61	RESETDRV falling edge from rising edge POWERGOOD	5		ns

6. DMA Read Cycle Timing

V_{CC}=5V±10%(3.3V±0.3V)*2, Ta=0 to 70˚C, C_L=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T41	IOCHRDY inactive from WAIT# active		20(30)*1	ns
T42	IOCHRDY active to WAIT# inactive	0	20(30)*1	ns
T33	CIOWE# active from IOW#		25	ns
T38	IOW# inactive to rising edge of CIOWR#, TC (WE#)	0	24	ns
T74	SD <15 : 0> valid to CD <15 : 0> valid		50	ns
T91	DACK# (IRQ9) active to DMA cycle begin		40 (50)	ns
T92	system TC (IRQ11 or IRQ15) to card TC (WE#)		40 (50)	ns
T93	rising edge of DACK# (IRQ9) to CE#, REG#		40 (50)	ns

*1) This Timing assumes a load capacitance of 50pF.
*2) In the above table, the parenthesized specifications apply when V_{CC}=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether V_{CC}=5V±10% or 3.3±0.3V.

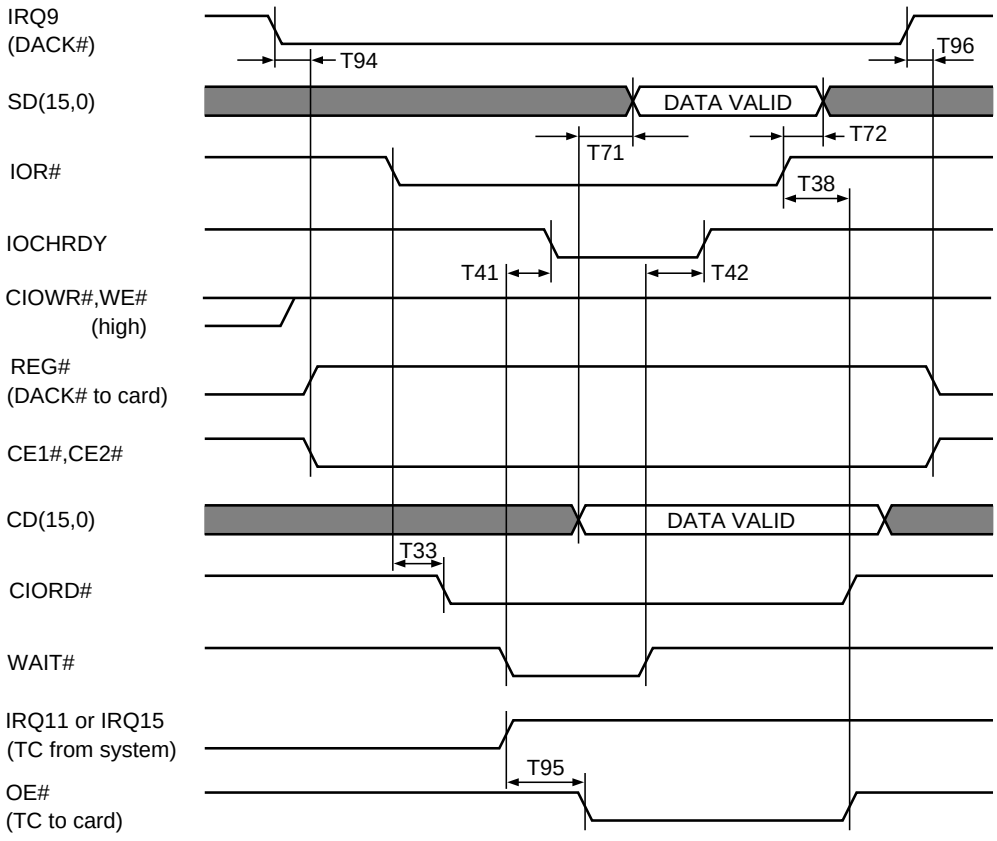


7. DMA Write Cycle Timing

V_{CC}=5V±10%(3.3V±0.3V)*2, Ta=0 to 70°C, C_L=100pF

Symbol	Item	Limits		Unit
		MIN.	MAX.	
T41	IOCHRDY inactive from WAIT# active		20(30)*1	ns
T42	IOCHRDY active from WAIT# inactive	0	20(30)*1	ns
T33	CIORD# active from IOR#		25	ns
T38	IOR# inactive to rising edge of CIORD#, TC (OE#)	0	24	ns
T71	SD <15 : 0> valid to CD <15 : 0> valid		50	ns
T72	SD <15 : 0> hold from IOR#, MEMR#	10		ns
T94	DACK# (IRQ9) active to DMA cycle begin		40 (50)	ns
T95	system TC (IRQ11 or IRQ15) to card TC (WE#)		40 (50)	ns
T96	rising edge of DACK# (IRQ9) to CE#, REG#		40 (50)	ns

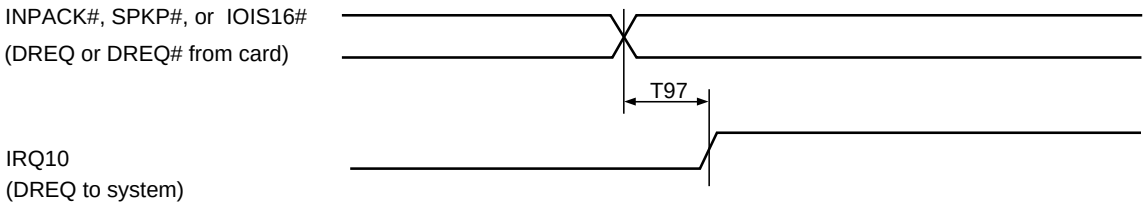
*1) This Timing assumes a load capacitance of 50pF.
*2) In the above table, the parenthesized specifications apply when V_{CC}=3.3±0.3V. Accordingly, the non-parenthesized specifications alone apply whether V_{CC}=5V±10% or 3.3±0.3V.



8. DMA Request Timing

V_{CC}=5V±10%(3.3V±0.3V), Ta=0 to 70°C, CL=100pF

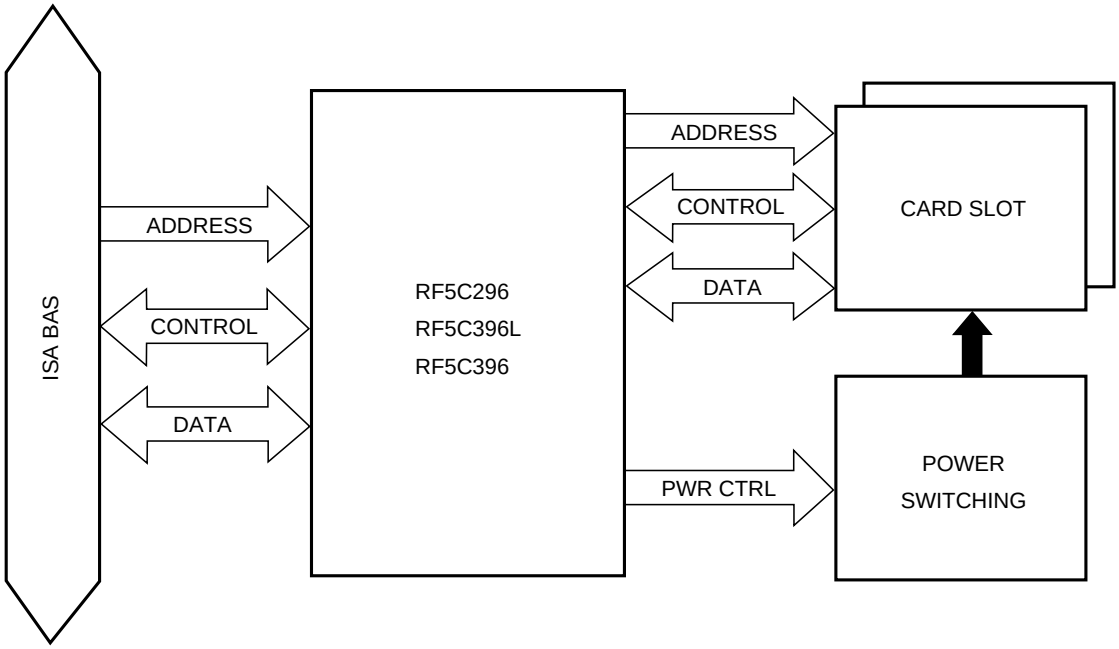
Symbol	Item	Limits		Unit
		MIN.	MAX.	
T97	DMA request from card to system		40	ns



Notice

For the RF5C296 and the RF5C396, the relation between the Read/Write timings for the DATA and ADDRESS signals and those for the CIOWR#, CIORD#, WE#, and OE# signals is not specified, and dependent on the input timings for the relevant signals from the system bus and on the internal delay time of the named signals.
It is recommended that the above should be included in the considerations of timing conditions for the JEIDA4.2 (or PCMCIA2.1) system.

BUS SYSTEM



SUPPORT ENVIRONMENT

- Driver Soft

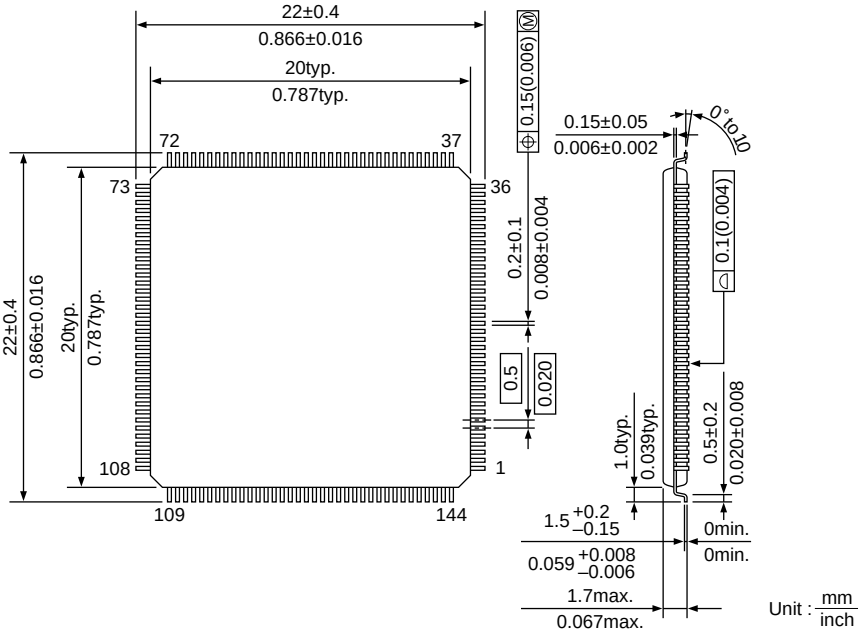
Phoenix Technologies,Ltd.(U.S.A.)	PhoenixCARD Manager Plus™
SystemSoft Corporation(U.S.A.)	SystemSoft's Card Soft™

- Demonstration board

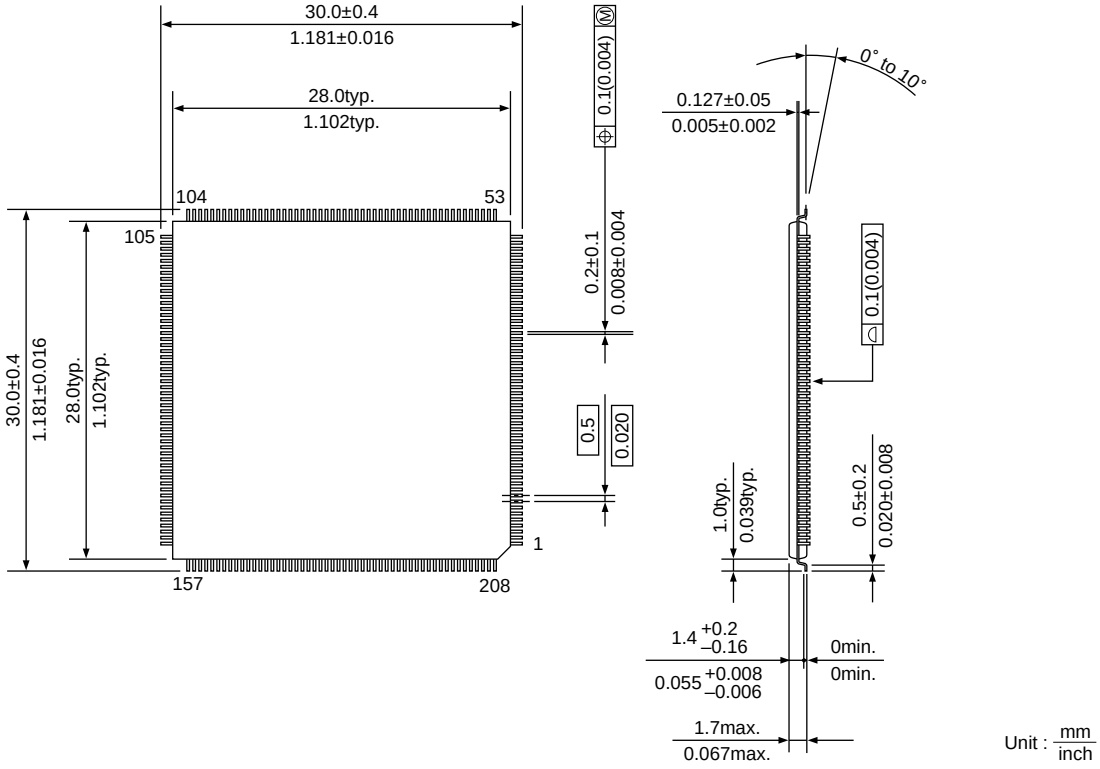
Demonstration board for RF5C396

PACKAGE DIMENSIONS

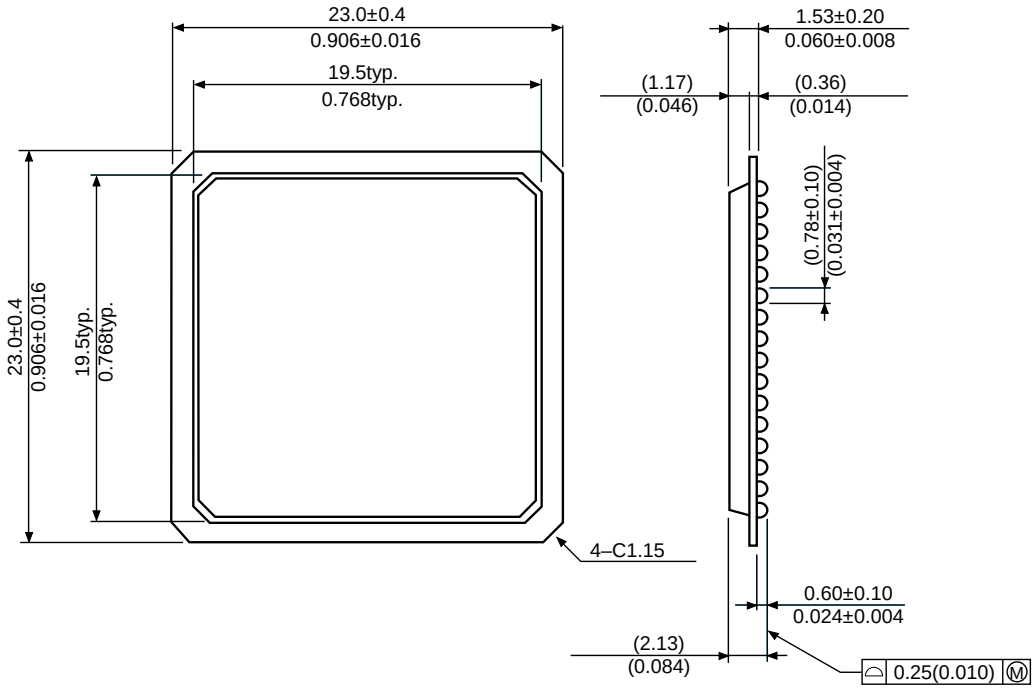
• RF5C296
144pin LQFP
(LQFP-144-P1)

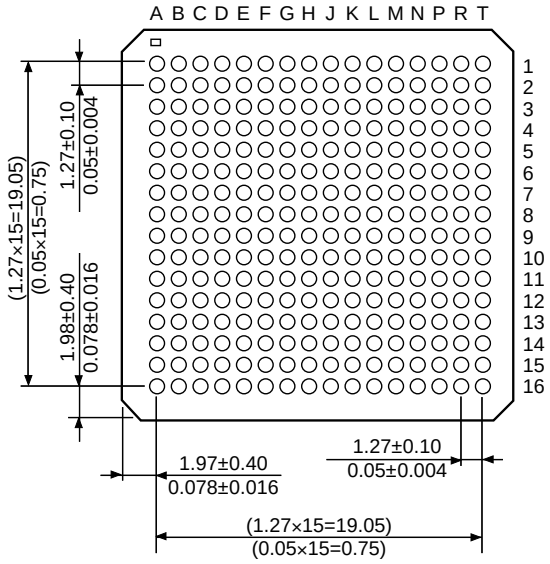


• RF5C396L
208pin LQFP
(LQFP-208-P1)



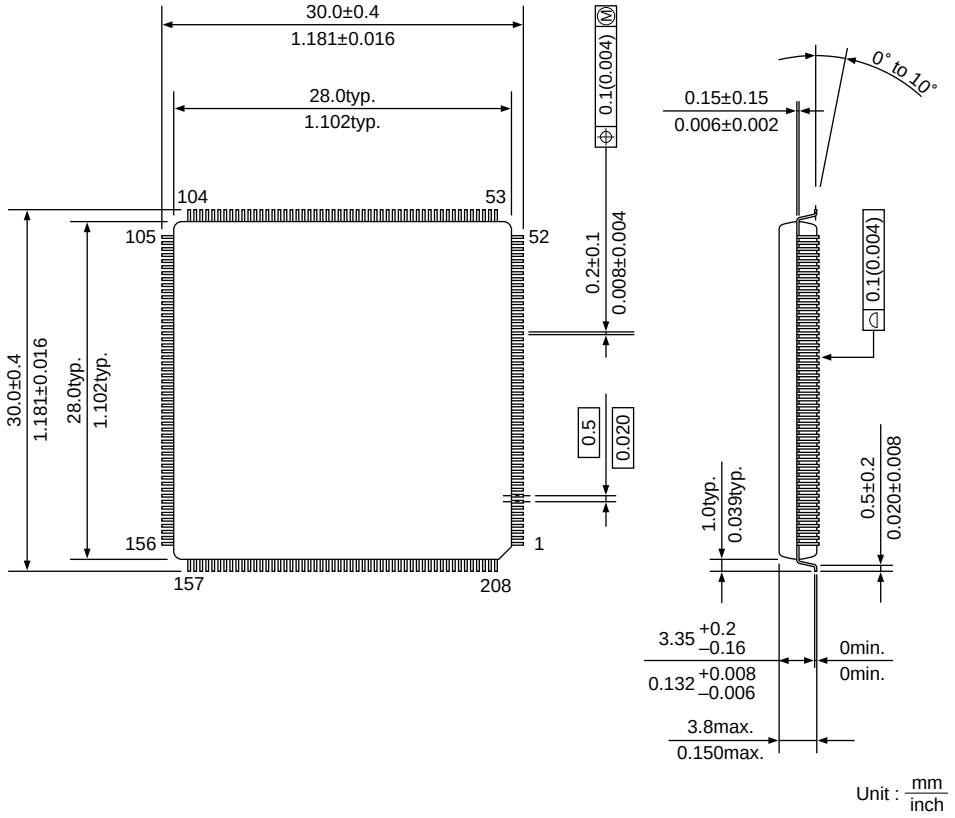
• RB5C396
256pin PBGA
(BGA-256-P1)





Unit : mm / inch

• **RF5C396**
208pin QFP
(QFP-208-P1)



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