



# Product Specification

AU OPTRONICS CORPORATION

( V ) Preliminary Specifications

( ) Final Specifications

<b>Module</b>	15.4" WXGA+ Color TFT-LCD
<b>Model Name</b>	B154PW01 V0

<b>Customer</b>	<b>Date</b>
_____	_____
<b>Checked &amp; Approved by</b>	
_____	_____
Note: This Specification is subject to change without notice.	

<b>Approved by</b>	<b>Date</b>
_____	_____
<b>Prepared by</b>	
_____	_____
MDBU Marketing Division / AU Optronics corporation	



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## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2005/12/01	All	First Edition for Customer		
0.2 2006/02/06	31		Add EDID description	
0.3 2006/03/10	29	HW: 1A	HW:0A	



## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

## 2. General Description

B154PW01 V1 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+



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(1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B154PW01 V1 is designed for a display unit of notebook style personal computer and industrial machine.

## 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.4W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1440x3(RGB) x 900
Pixel Pitch	[mm]	0.23025X0.23025
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (I <sub>CCFL</sub> =6.0mA) Note: I <sub>CCFL</sub> is lamp current	[cd/m <sup>2</sup> ]	300 typ. (5 points average) 275 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ
Optical Rise Time/Fall Time	[msec]	4/12 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	6.0 max.(without inverter)
Weight	[Grams]	535 max.
Physical Size	[mm]	344.0 typ. x 222.0 typ. x 6.1 max.
Electrical Interface		2 channel LVDS
Surface Treatment		Glare, Hardness 3H, Reflectance 1.5%
Support Color		262K colors ( RGB 6-bit )
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance



# Product Specification

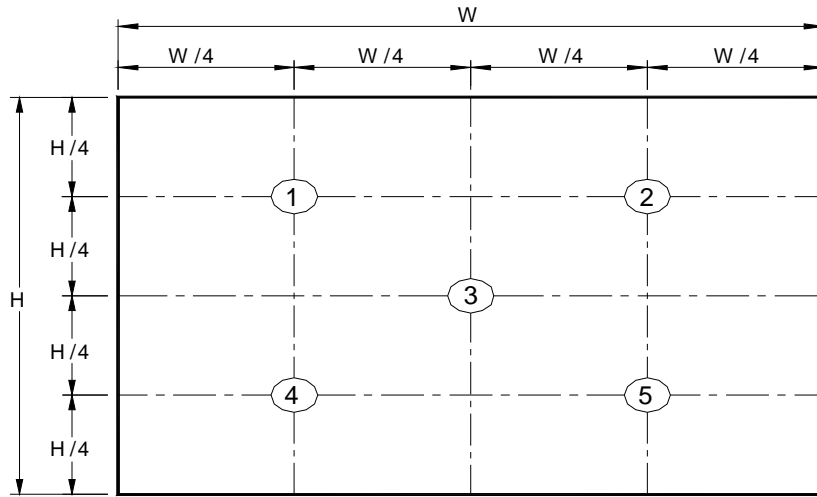
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## 2.2 Optical Characteristics

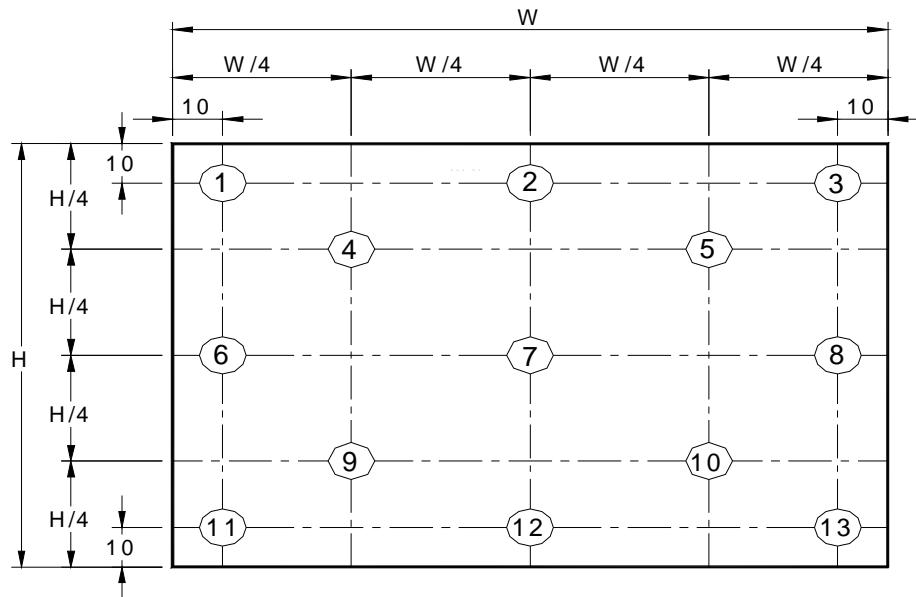
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance I <sub>CCFL</sub> =6.0mA	[cd/m <sup>2</sup> ]	5 points average	275	300	-	1, 4, 5.
Viewing Angle	[degree]	Horizontal (Right)	60	70	-	9
	[degree]	CR = 10 (Left)	60	70	-	
	[degree]	Vertical (Upper)	50	60	-	
	[degree]	CR = 10 (Lower)	50	60	-	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			1.50	2
CR: Contrast Ratio			300	400	-	6
Cross talk	%				4	7
Response Time	[msec]	Rising	-	4	8	8
	[msec]	Falling	-	12	17	
	[msec]	Rising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.590	0.620	2,8
		Red y	0.315	0.345	0.375	
		Green x	0.285	0.315	0.345	
		Green y	0.520	0.555	0.580	
		Blue x	0.125	0.155	0.185	
		Blue y	0.115	0.145	0.175	
		White x	0.290	0.313	0.343	
		White y	0.299	0.329	0.350	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)



Note 2: 13 points position



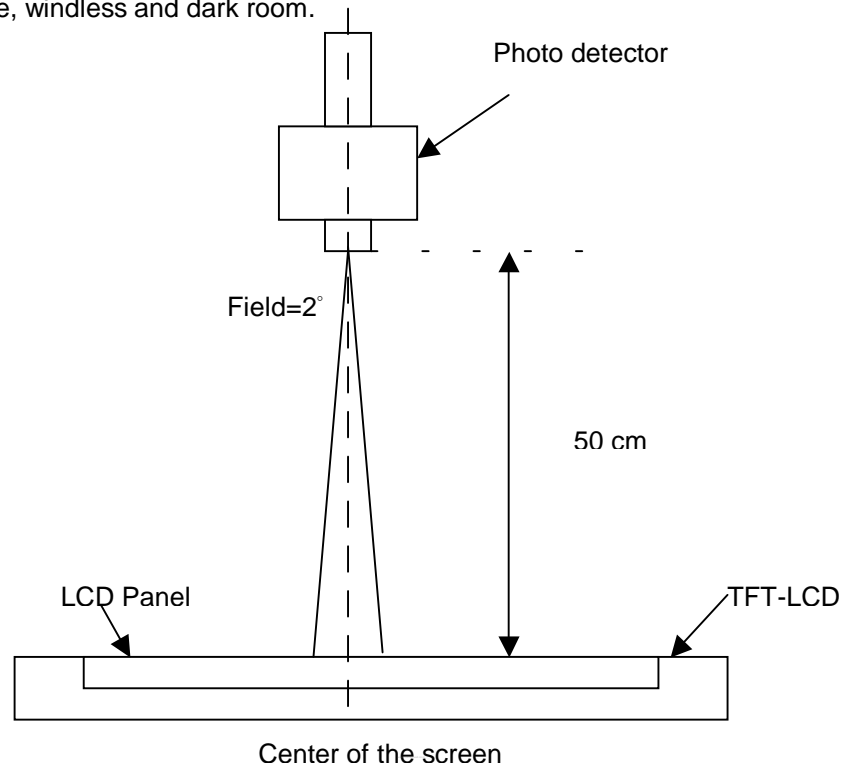
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5 : Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

Note 7 : Definition of Cross Talk (CT)

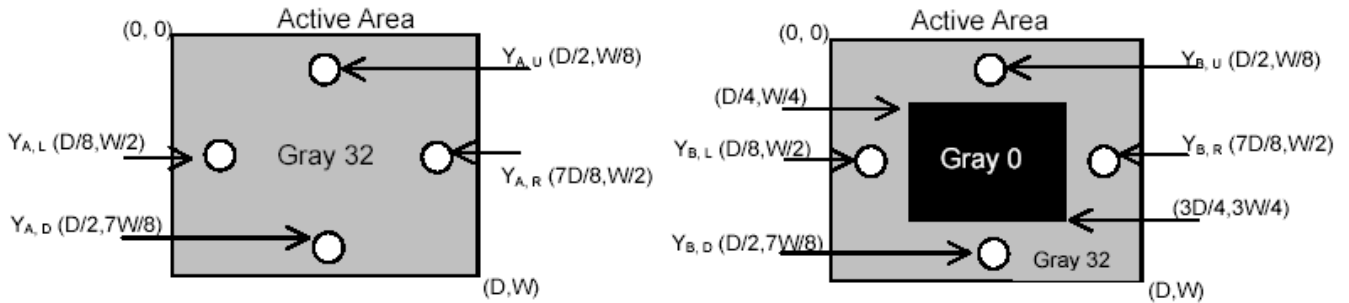
$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

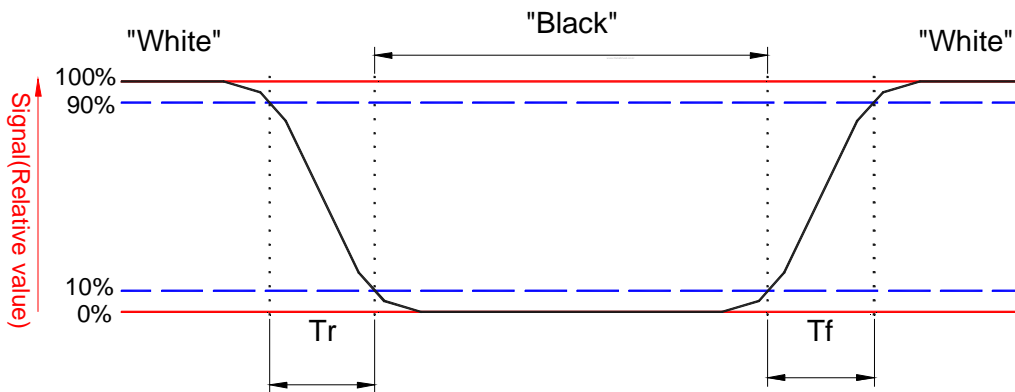


$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



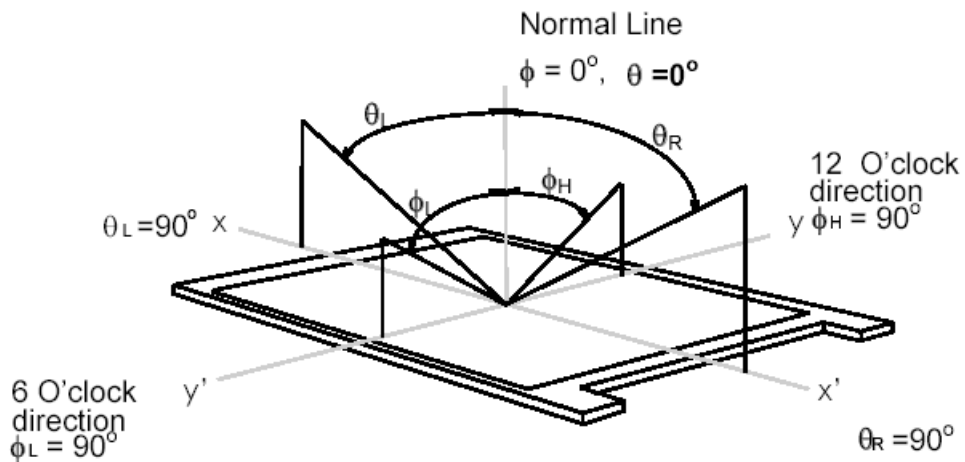
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



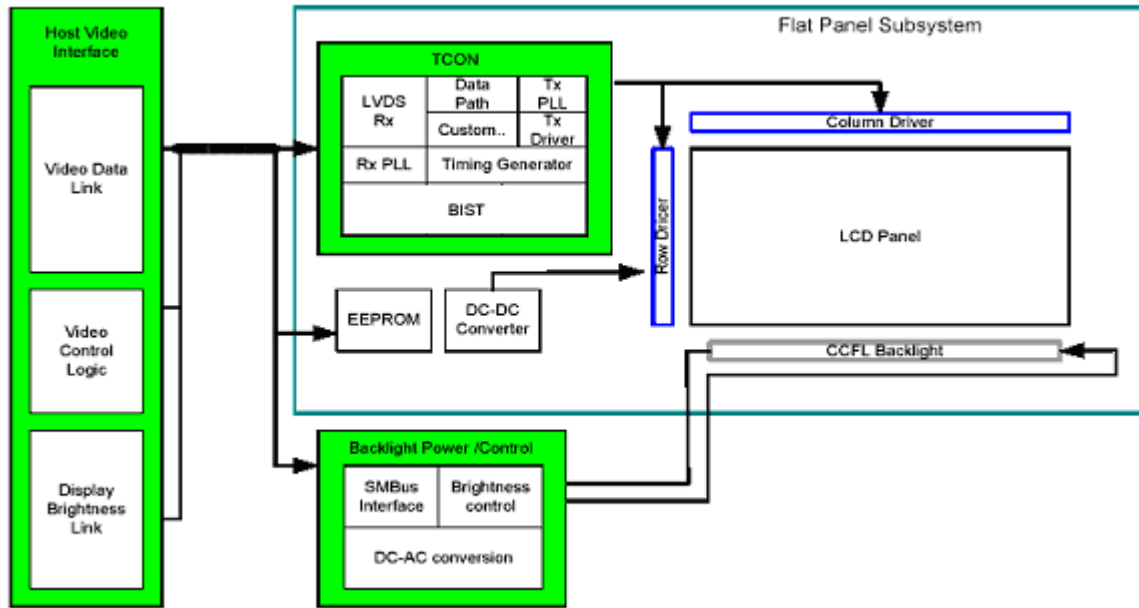
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° ( $\theta$ ) horizontal left and right and 90° ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 15.4WXGA+ TFT/LCD Module:



## 4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

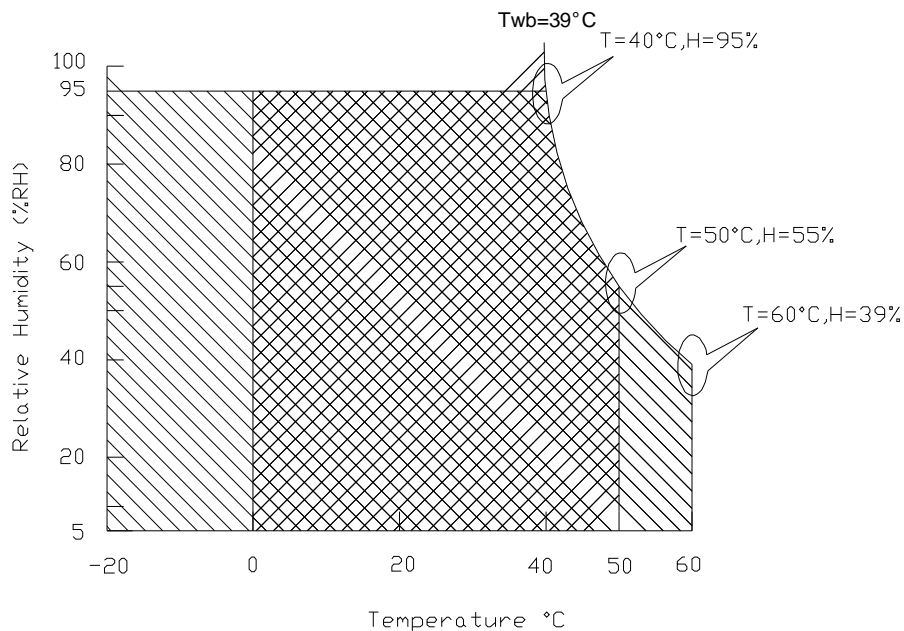
### 4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	--	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

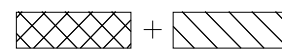
Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range



## 5. Electrical characteristics

### 5.1 TFT LCD Module

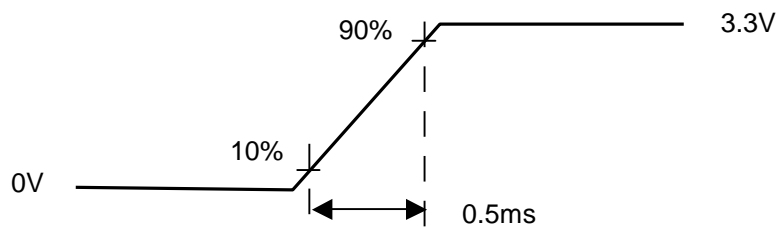
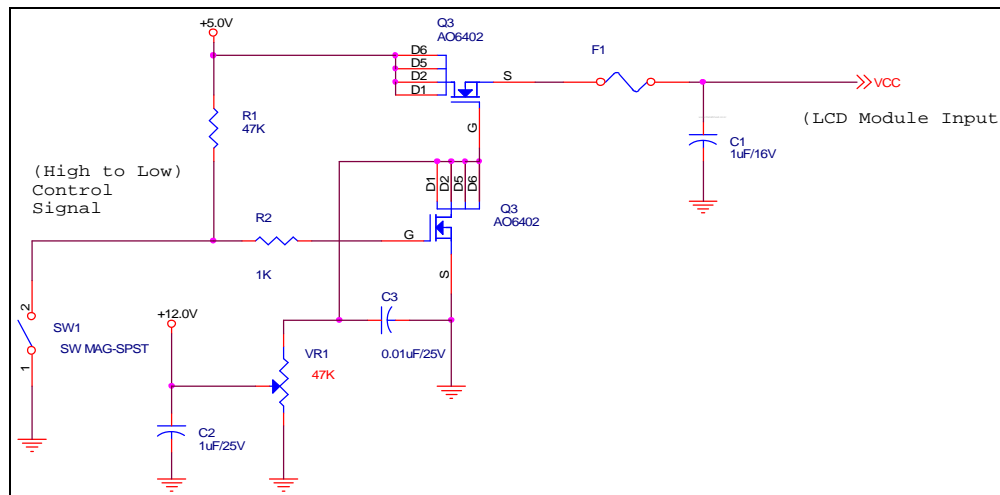
#### 5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.7	[Watt]	Note 1
IDD	IDD Current		400	500	[mA]	Note 1
IRush	Inrush Current			2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern

Note 2 : Measure Condition



Vin rising time

## 5.1.2 Signal Electrical Characteristics

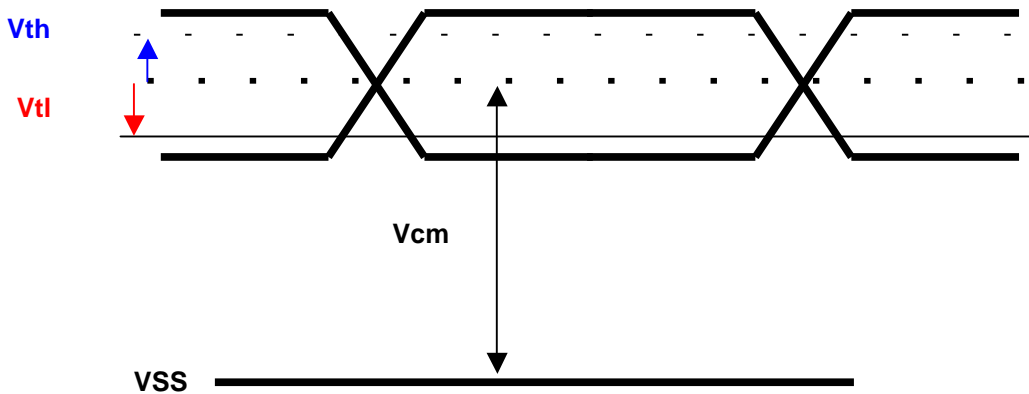
Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





## 5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	275	300	-	[cd/m <sup>2</sup> ]	(Ta=25°C)
CCFL current(I <sub>CCFL</sub> )	2.0	6.0	7.0	[mA] rms	(Ta=25°C) Note 2
CCFL Frequency(F <sub>CCFL</sub> )	45	52	65	[KHz]	(Ta=25°C) Note 3,4
CCFL Ignition Voltage(Vs)	1340			[Volt] rms	(Ta= 0°C) Note 5
CCFL Ignition Voltage(Vs)	1030			[Volt] rms	(Ta= 25°C) Note 5
CCFL Voltage (Reference) (V <sub>CCFL</sub> )	620	720	910	[Volt] rms	(Ta=25°C) Note 6
CCFL Power consumption (P <sub>CCFL</sub> )	-	4.30	4.70	[Watt]	(Ta=25°C) Note 6

Note 1: Typ are AUO recommended Design Points.

\*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

\*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully.

Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

\*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

\*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

\*5 CCFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

\*6 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has "Duty Dimming", if ICCFL is less than 4mA.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 1,340 voltage. Lamp units need 1,300 voltage minimum for ignition.

Note 6: Calculator value for reference ( $I_{CCFL} \times V_{CCFL} = P_{CCFL}$ )

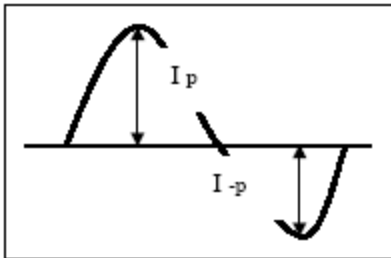
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within  $\sqrt{2} \pm 10\%$ .

\* Inverter output waveform had better be more similar to ideal sine wave.



\* Asymmetry rate:

$$\frac{|I_p - I_{-p}|}{I_{rms}} * 100\%$$

\* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$





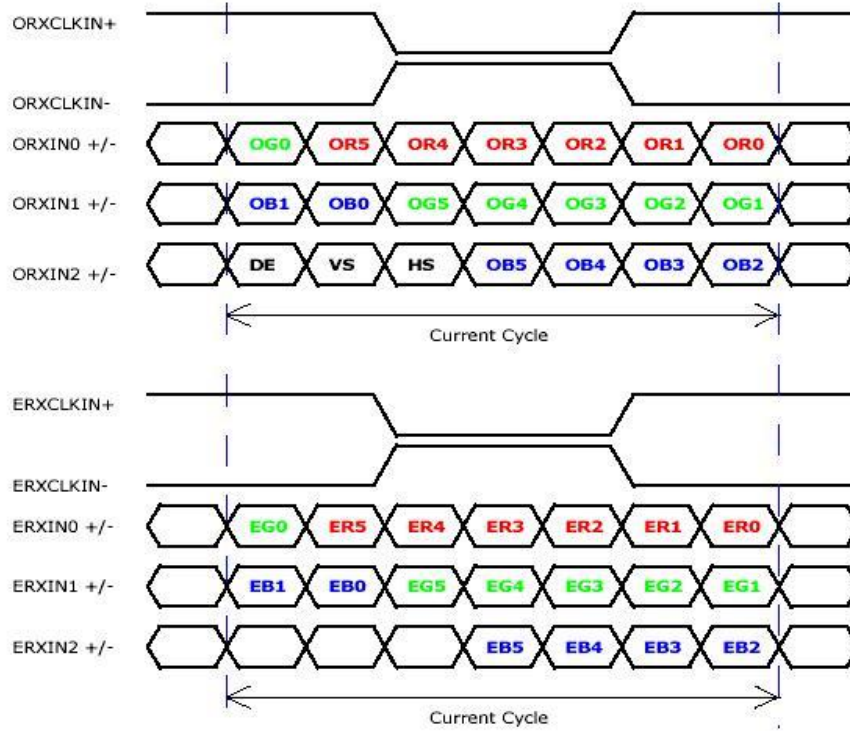
## 6. Signal Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

	1		2												1439		1440					
1st Line	R	G	B	R	G	B	.....										R	G	B	R	G	B
	.	.	.	.	.	.	.....										.	.	.	.	.	.
	.	.	.	.	.	.	.....										.	.	.	.	.	.
	.	.	.	.	.	.	.....										.	.	.	.	.	.
	.	.	.	.	.	.	.....										.	.	.	.	.	.
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	.	.	.	.	.	.	.....										.	.	.	.	.	.
	.	.	.	.	.	.	.....										.	.	.	.	.	.
900th Line	R	G	B	R	G	B	.....										R	G	B	R	G	B

## 6.2 The input data format



Signal Name	Description
V <sub>EDID</sub>	+3.3V EDID Power
CLK <sub>EDID</sub>	EDID Clock Input
DATA <sub>EDID</sub>	EDID Data Input
ORXIN0-, ORXIN0+	Odd LVDS differential data input(ORed0-ORed5, OGreen0)
ORXIN1-, ORXIN1+	Odd LVDS differential data input(OGreen1-OGreen5, OBlue0-ORed1)
ORXIN2-, ORXIN2+	Odd LVDS differential data input(OBlue2-OBlue5, Hsync, Vsync, DE)
ORXCLKIN-, ORXCLKIN+	Odd LVDS differential clock input
ERXIN0-, ERXIN0+	Even LVDS differential data input(ERed0-ERed5, EGreen0)
ERXIN1-, ERXIN1+	Even LVDS differential data input(EGreen1-EGreen5, EBlue0-EBlue1)
ERXIN2-, ERXIN2+	Even LVDS differential data input(EBlue2-EBlue5)
ERXCLKIN-, ERXCLKIN+	Even LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

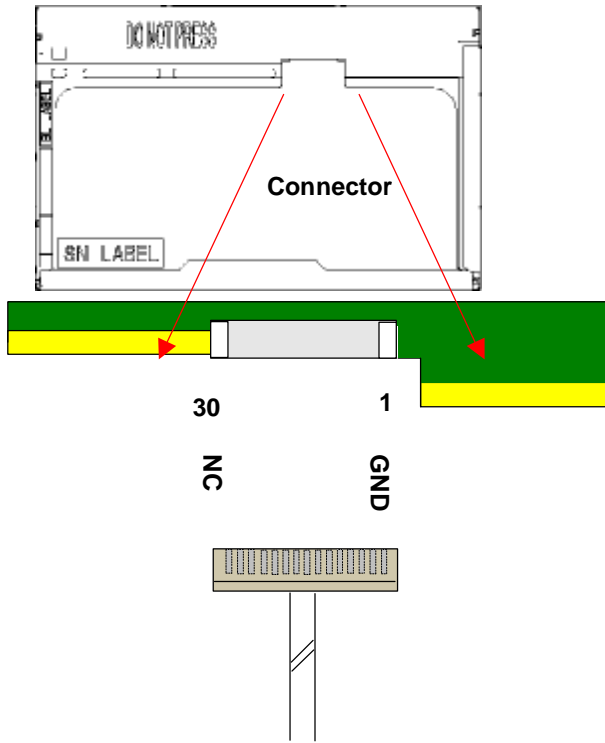


## 6.3 Signal Description/Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN #	SIGNAL NAME	DESCRIPTION
1	VSS	Power Ground
2	VDD	+ 3.3V Power Supply
3	VDD	+ 3.3V Power Supply
4	V <sub>EDID</sub>	+ 3.3V EDID Power
5	AGING	Aging Mode Power Supply
6	CLK <sub>EDID</sub>	EDID Clock Input
7	DATA <sub>EDID</sub>	EDID Data Input
8	Odd_Rin0-	-LVDS Differential Data Input
9	Odd_Rin0+	+LVDS Differential Data Input
10	VSS	Power Ground
11	Odd_Rin1-	-LVDS Differential Data Input
12	Odd_Rin1+	+LVDS Differential Data Input
13	VSS	Power Ground
14	Odd_Rin2-	-LVDS Differential Data Input
15	Odd_Rin2+	+LVDS Differential Data Input
16	VSS	Power Ground
17	Odd_ClkIN-	-LVDS Differential Clock Input
18	Odd_ClkIN+	+LVDS Differential Clock Input
19	VSS	Power Ground
20	Even_Rin0-	-LVDS Differential Data Input
21	Even_Rin0+	+LVDS Differential Data Input
22	VSS	Power Ground
23	Even_Rin1-	-LVDS Differential Data Input
24	Even_Rin1+	+LVDS Differential Data Input
25	VSS	Power Ground
26	Even_Rin2-	-LVDS Differential Data Input
27	Even_Rin2+	+LVDS Differential Data Input
28	VSS	Power Ground
29	Even_ClkIN-	-LVDS Differential Clock Input
30	Even_ClkIN+	+LVDS Differential Clock Input

Note1: Start from right side





## 6.4 Interface Timing

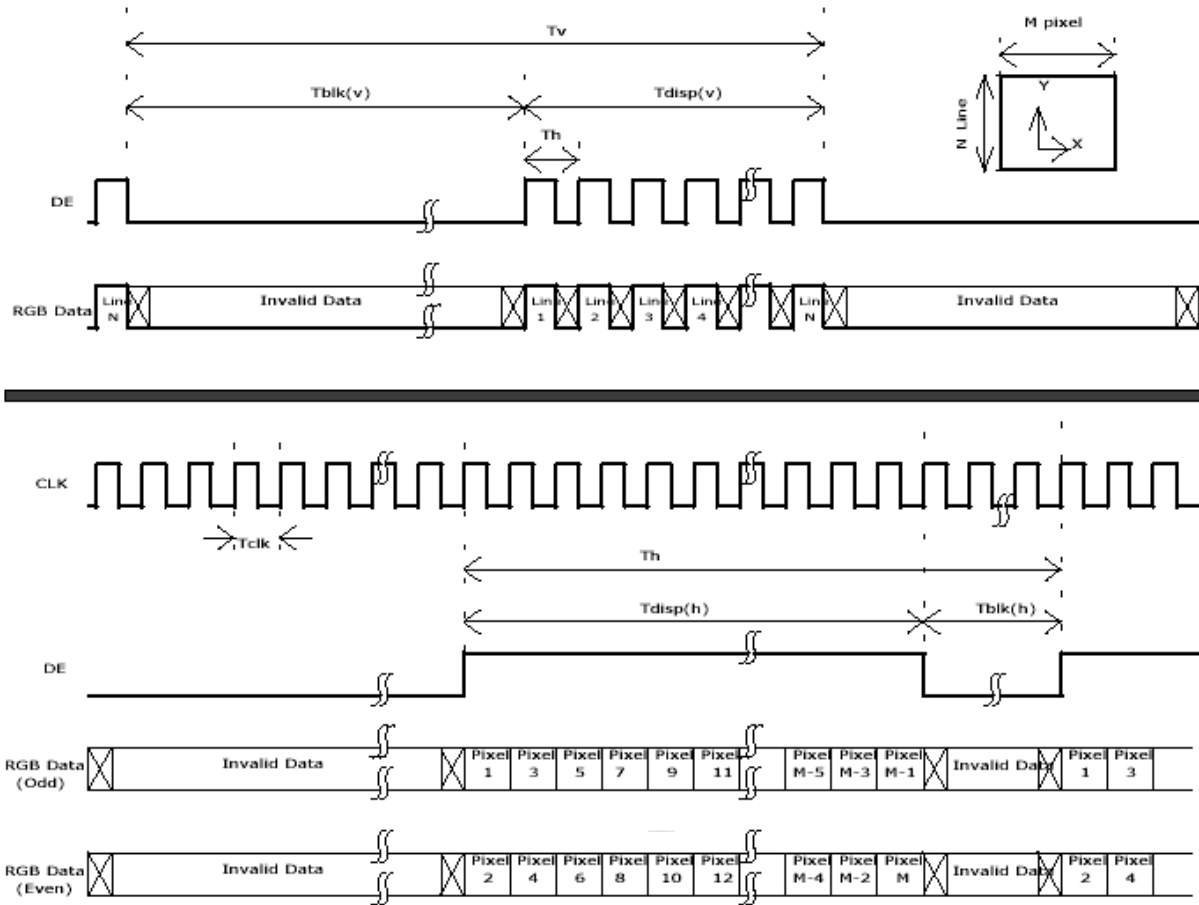
### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1440X900 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	50	60	-	Hz	
Clock frequency	$1/ T_{\text{Clock}}$	50	48.2	60.2	MHz	
Vertical Section	Period	$T_V$	904	912	2048	$T_{\text{Line}}$
	Active	$T_{VD}$	900	900	900	
	Blanking	$T_{VB}$	4	12	-	
Horizontal Section	Period	$T_H$	760	880	1024	$T_{\text{Clock}}$
	Active	$T_{HD}$	720	720	720	
	Blanking	$T_{HB}$	40	160	-	

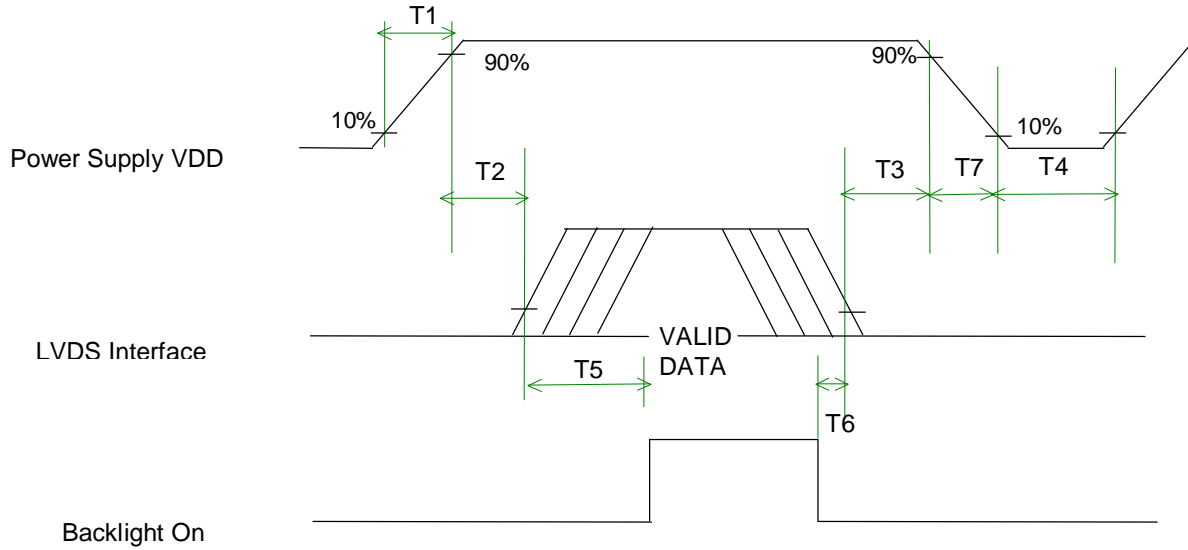
Note : DE mode only

## 6.4.2 Timing diagram



## 6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



### Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	5	-	50	(ms)
T3	0.5	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)



## 7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

### 7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H or compatible

### 7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

### 7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage





## 8. Vibration and Shock Test (Stand alone)

### 8.1 Vibration Test

**Test Spec:**

- I Test method: Non-Operation
- I Acceleration: 1.5G
- I Frequency: 26 - 500Hz Random
- I Sweep: 30 Minutes each Axis (X, Y, Z)

### 8.2 Shock Test Spec:

**Test Spec:**

- I Test method: Non-Operation
- I Acceleration: 260 G , Half sine wave
- I Active time: 2 ms
- I Pulse: X,Y,Z .one time for each side



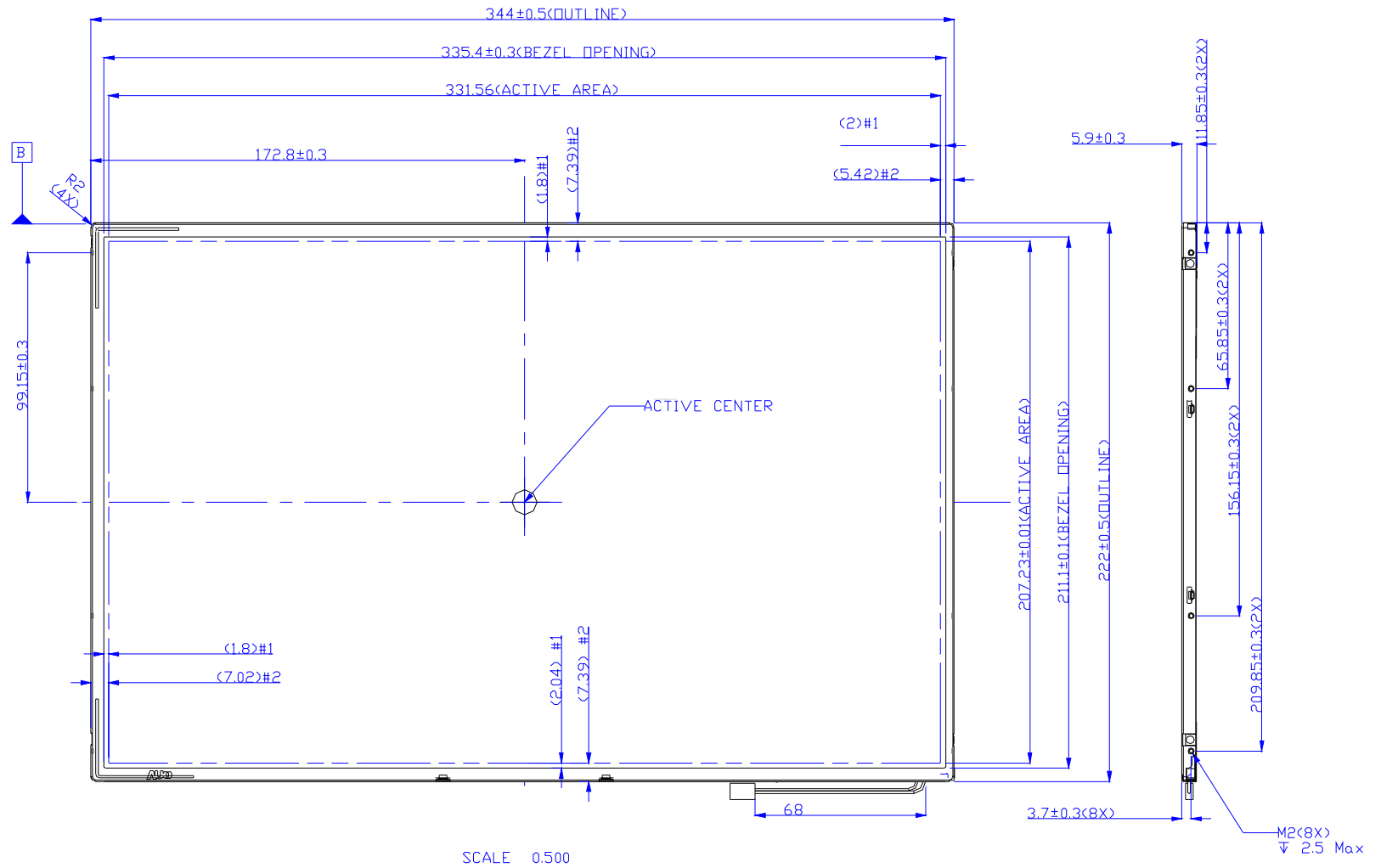
## 9. Reliability

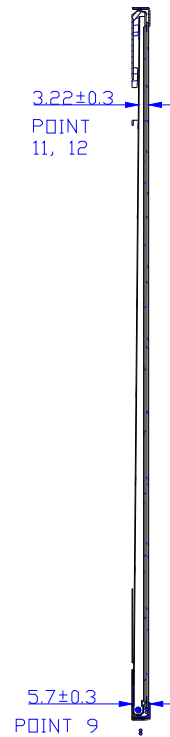
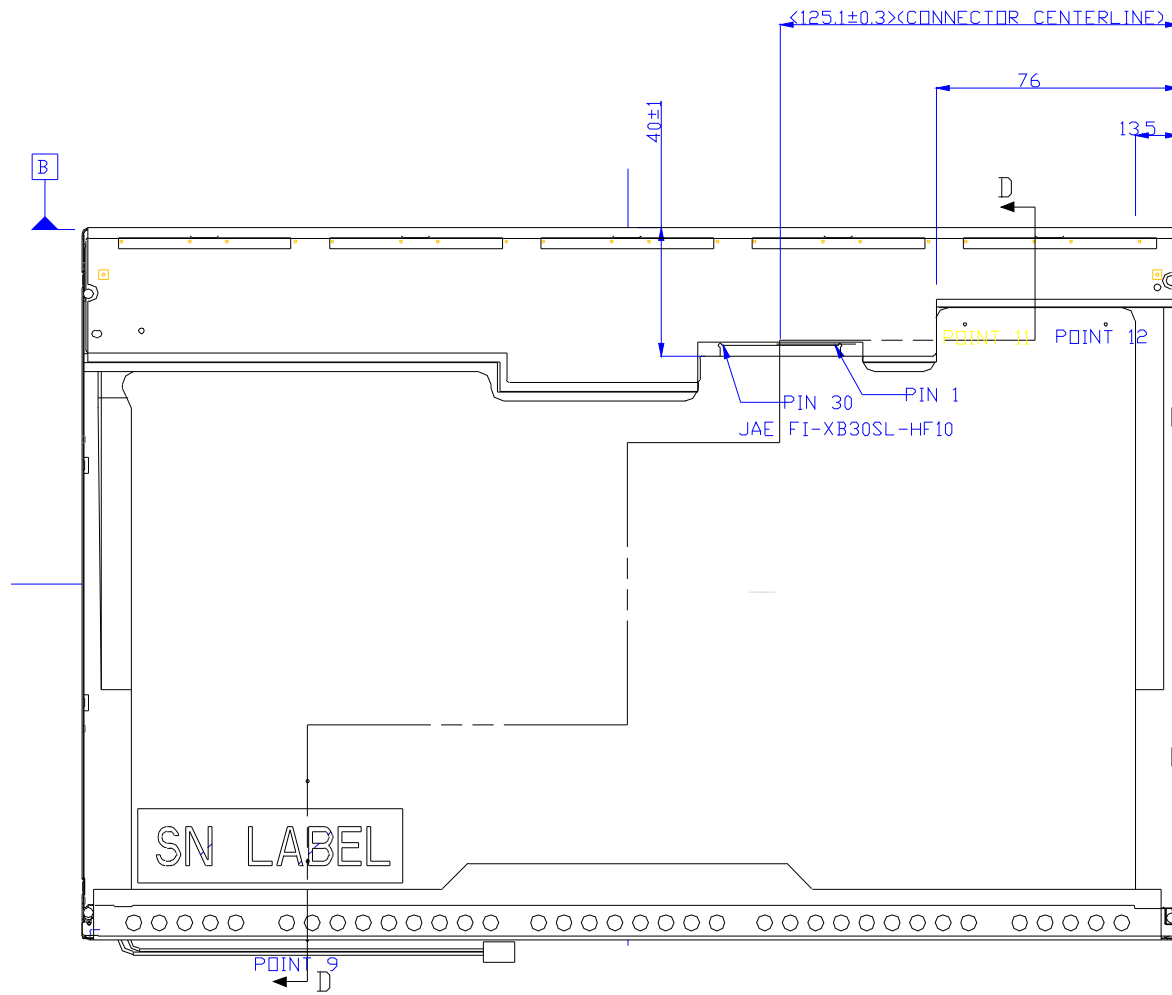
Items	Required Condition	Note
Temperature Humidity Bias	40°C /95%,300Hrs	
High Temperature Operation	50°C /Dry,300Hrs	
Low Temperature Operation	0°C ,300Hrs	
On/Off Test	25°C ,150hrs(ON/30 sec. OFF/30sec., 10,000 cycles)	
Hot Storage	65°C /20% RH ,300 hours	
Cold Storage	-25°C /50% RH ,300 hours	
Thermal Shock Test	-25°C /30 min ,65°C /30 min 100cycles non-OP	
Shock Test (Non-Operating)	260G, 2ms, Half-sine wave, +/- X, Y,Z direction,1 cycle	
Vibration Test (Non-Operating)	Sinusoidal vibration, 3.0 G zero-to-peak, 10 to 150 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Image sticking	10X10 checker pattern, 10 hrs, 25°C . The persisting pattern should be disappeared in 5 minutes	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost  
. Self-recoverable. No hardware failures.

# 10. Mechanical Characteristics

## 10.1 LCM Outline Dimension

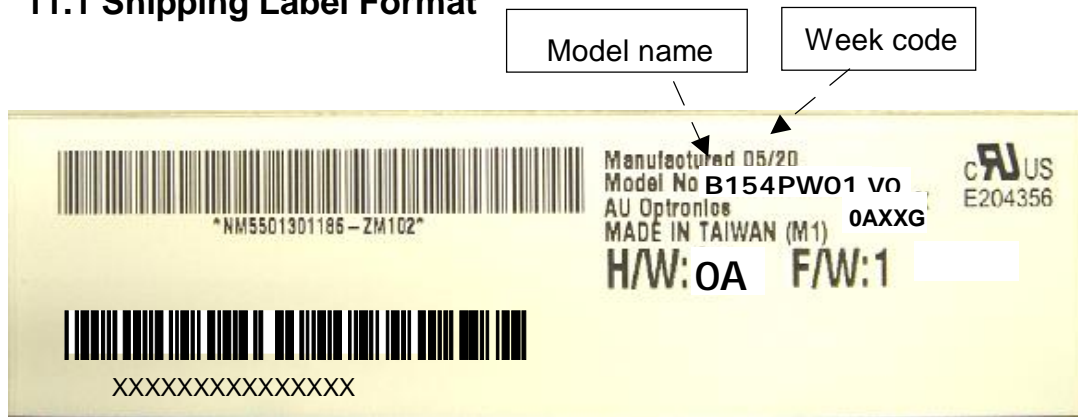




SECTION D-D

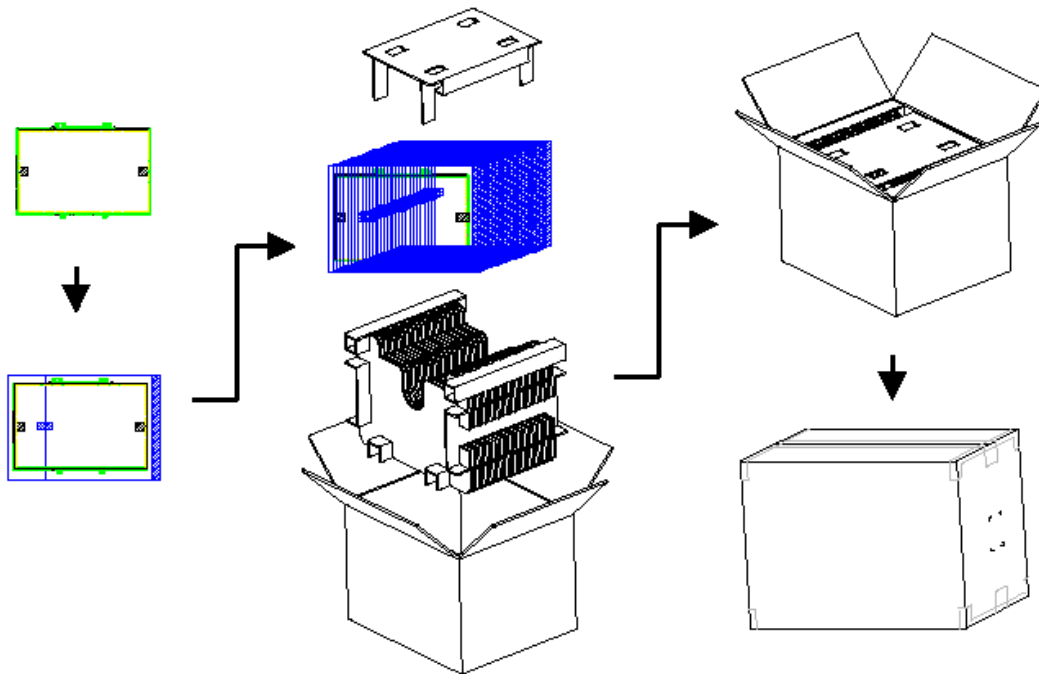
# 11. Shipping and Package

## 11.1 Shipping Label Format

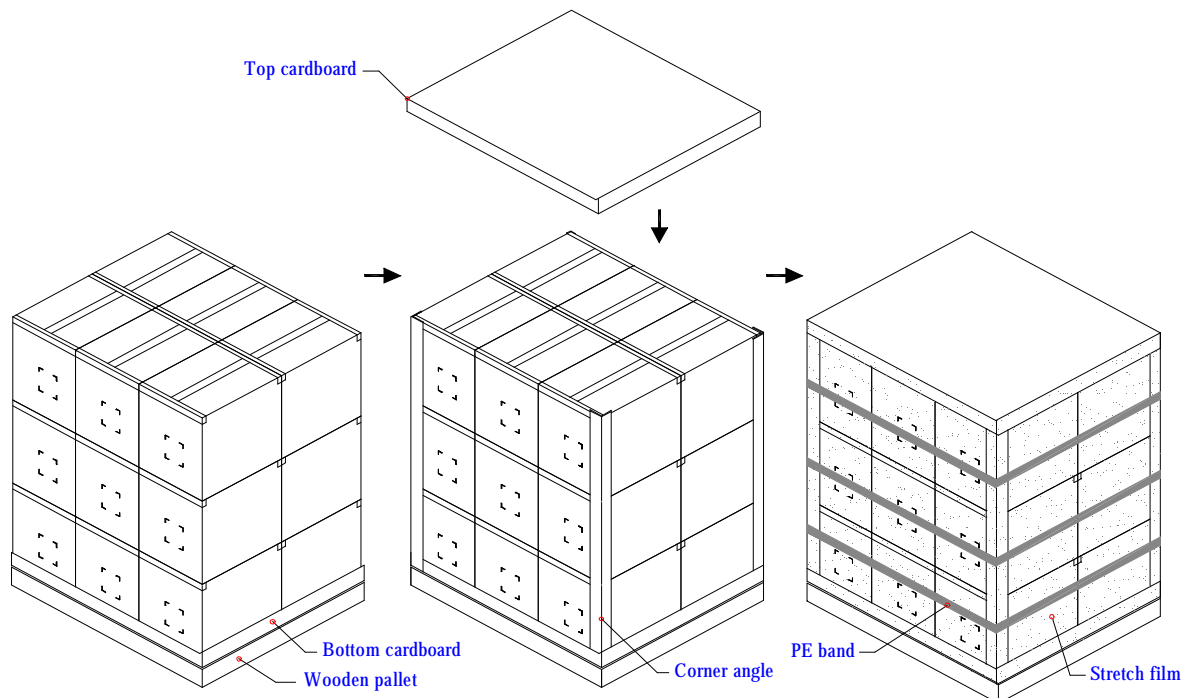


## 11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



## 11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

## 12. Appendix: EDID description

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC	Notes
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	10	00010000	16	
0A	Product Code	60	01100000	96	
0B	hex, LSB first	9C	10011100	156	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	04	00000100	4	Week 4
11	Year of manufacture	10	00010000	16	2006
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input definition	80	10000000	128	
15	Max H image size	22	00100010	34	34cm
16	Max V image size	16	00010110	22	22cm
17	Display Gamma	78	01111000	120	Gamma 2.2
18	Feature support	0A	00001010	10	
19	Red/green low bits	1C	00011100	28	
1A	Blue/white low bits	F5	11110101	245	
1B	Red x/ high bits	97	10010111	151	
1C	Red y	58	01011000	88	
1D	Green x	50	01010000	80	
1E	Green y	8E	10001110	142	
1F	Blue x	27	00100111	39	
20	Blue y	27	00100111	39	
21	White x	50	01010000	80	

22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1
2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Detailed timing/monitor	9F	10011111	159
37	descriptor #1	25	00100101	37
38		A0	10100000	160
39		40	01000000	64
3A		51	01010001	81
3B		84	10000100	132
3C		0C	00001100	12
3D		30	00110000	48
3E		40	01000000	64
3F		20	00100000	32
40		33	00110011	51
41		00	00000000	0
42		4B	01001011	75
43		CF	11001111	207
44		10	00010000	16
45		00	00000000	0
46		00	00000000	0



47		19	00011001	25	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		01	00000001	1	
4C		00	00000000	0	
4D		06	00000110	6	
4E		10	00010000	16	
4F		30	00110000	48	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		0A	00001010	10	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	Ascii Data String
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F		42	01000010	66	
60		31	00110001	49	
61		35	00110101	53	
62		34	00110100	52	
63		50	01010000	80	
64		57	01010111	87	
65		30	00110000	48	
66		31	00110001	49	
67		20	00100000	32	
68		56	01010110	86	
69		30	00110000	48	
6A		0A	00001010	10	

<b>6B</b>		20	00100000	32	
<b>6C</b>	Detailed timing/monitor	00	00000000	0	Monitor Name: Color LCD
<b>6D</b>	descriptor #4	00	00000000	0	
<b>6E</b>		00	00000000	0	
<b>6F</b>		FC	11111100	252	
<b>70</b>		00	00000000	0	
<b>71</b>		43	01000011	67	C
<b>72</b>		6F	01101111	111	o
<b>73</b>		6C	01101100	108	l
<b>74</b>		6F	01101111	111	o
<b>75</b>		72	01110010	114	r
<b>76</b>		20	00100000	32	
<b>77</b>		4C	01001100	76	L
<b>78</b>		43	01000011	67	C
<b>79</b>		44	01000100	68	D
<b>7A</b>		0A	00001010	10	
<b>7B</b>		20	00100000	32	
<b>7C</b>		20	00100000	32	
<b>7D</b>		20	00100000	32	
<b>7E</b>	Extension Flag	00	00000000	0	
<b>7F</b>	Checksum	BC	10111100	188	

