TOSHIBA Field Effect Transistor Silicon P, N Channel MOS Type (U-MOS Ⅲ / π-MOS Ⅵ)

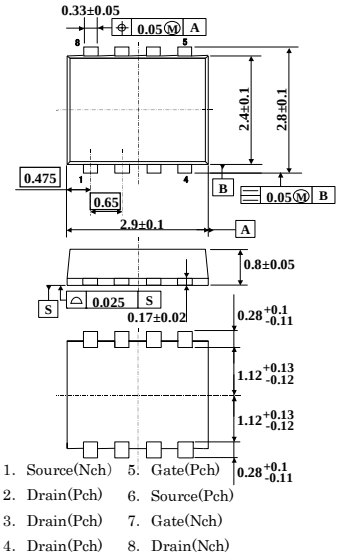
TPCP8401

○ Switching Regulator Applications

○ Load Switch Applications

- Lead(Pb)-Free
- Multi-chip discrete device; built-in P channel MOS FET for main switch and N Channel MOS FET for drive
- Small footprint due to small and thin package
- Low drain-source ON resistance
  : P Channel $R_{DS\ (ON)}$ = 31 mΩ (typ.)
- Low drain-source ON resistance
  High forward transfer admittance
  : P Channel $|Y_{fs}|$ = 13 S (typ.)
- Low leakage current
  : P Channel I_{DSS} = −10 μA (V_{DS} = −12 V)
- Enhancement−mode
  : P Channel V_{th} = −0.5 to −1.2 V (V_{DS} = −10 V, I_D = −200 μA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3V1G

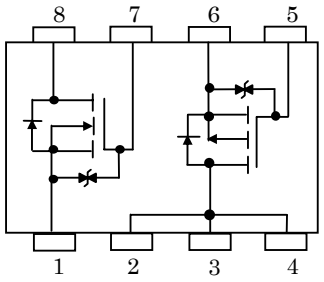
Weight: 0.017 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

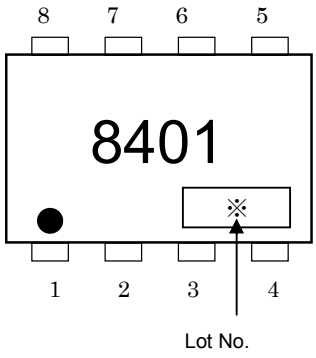
P-ch

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−12	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−12	V
Gate-source voltage		V_{GSS}	±8	V
Drain current	DC (Note 1)	I_D	−5.5	A
	Pulse (Note 1)	I_{DP}	−22.0	
Drain power dissipation (t = 5 s) (Note 2a)		P_D	1.96	W
Drain power dissipation (t = 5 s) (Note 2b)		P_D	1.0	W
Single pulse avalanche energy (Note 3)		E_{AS}	5.3	mJ
Avalanche current		I_{AR}	−2.8	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.22	mJ
Channel temperature		T_{ch}	150	°C

Circuit Configuration



Marking (Note5)



N-ch

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	20	V
Gate-source voltage			V_{GSS}	±10	V
Drain current	DC	(Note 1)	I_D	0.1	A
	Pulse	(Note 1)	I_{DP}	0.2	
Channel temperature			T_{ch}	150	°C
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)			E_{AR}	0.12	mJ
Channel temperature			T_{ch}	150	°C

This transistor is an electrostatic-sensitive device. Handle with caution.

Common Absolute Maximum Ratings (Ta=25°C)

Characteristics	Symbol	Rating	Unit
Storage temperature range	T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	63.8	°C/W
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	125	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

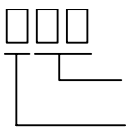
Note 2: (a) Mounted on FR4 board (glass epoxy, 0.8mm thick, Cu area: 25.4mm2) (t = 5s)

(b) Mounted on FR4 board (glass epoxy, 0.8mm thick, printed minimum pad dimensions: 25.4mm2) (t = 5s)

Note 3: V_{DD} = −10 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = −2.75 A

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: “●” on the lower left of the marking indicates pin 1.
“∗” shows the lot number, which consists of three digits. The first digit denotes the year of manufacture, expressed as the last digit of the calendar year; the next two digits denote the week of manufacture.

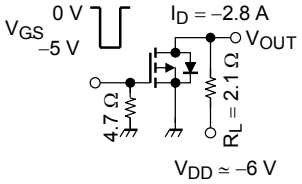


Week of manufacture
(01 for the first week of year, continuing up to 52 or 53)

Year of manufacture
(The last digit of the calendar year)

Electrical Characteristics (Ta = 25°C)

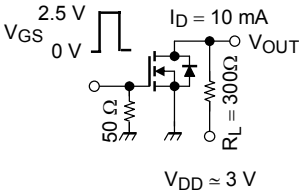
P-ch

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = −12 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−12	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−4	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −200 μA	−0.5	—	−1.2	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −1.8 V, I_D = −1.4 A	—	66	103	mΩ
			V_{GS} = −2.5 V, I_D = −2.8 A	—	44	58	
			V_{GS} = −4.5 V, I_D = −2.8 A		31	38	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.8 A	6.5	13	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	1520	—	pF
Reverse transfer capacitance		C_{rss}		—	330	—	
Output capacitance		C_{oss}		—	380	—	
Switching time	Rise time	t_r		—	9.5	—	ns
	Turn-on time	t_{on}		—	16	—	
	Fall time	t_f		—	28	—	
	Turn-off time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	74	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −10 V, V_{GS} = −5 V, I_D = −5.5 A	—	20	—	nC
Gate-source charge 1		Q_{gs1}		—	15	—	
Gate-drain (“miller”) charge		Q_{gd}		—	5	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current (pulse) (Note 1)	I_{DRP}	—	—	—	−22	A
Forward voltage (diode)	V_{DSF}	I_{DR} = −5.5 A, V_{GS} = 0 V	—	—	1.2	V

N-ch

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	20	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 1.5 V, I_D = 1 mA	—	5.2	15	Ω
			V_{GS} = 2.5 V, I_D = 10 mA	—	2.2	4	
			V_{GS} = 4 V, I_D = 10 mA	—	1.5	3	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	40	—	—	mS
Switching time	Turn-on time	t_{on}	 Duty ≦ 1%, t_w = 10 μs	—	70	—	ns
	Turn-off time	t_{off}		—	125	—	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	—	9.3	—	pF
Reverse transfer capacitance		C_{rss}		—	4.5	—	
Output capacitance		C_{oss}		—	9.8	—	

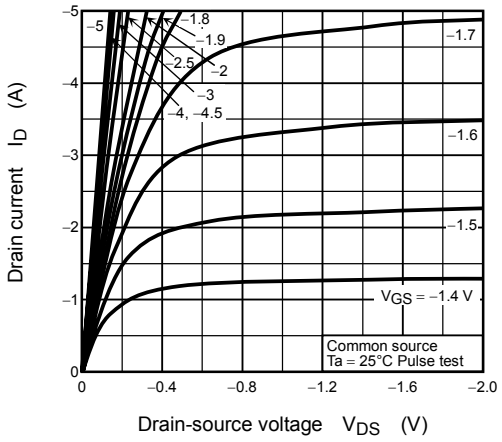
Precaution

V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

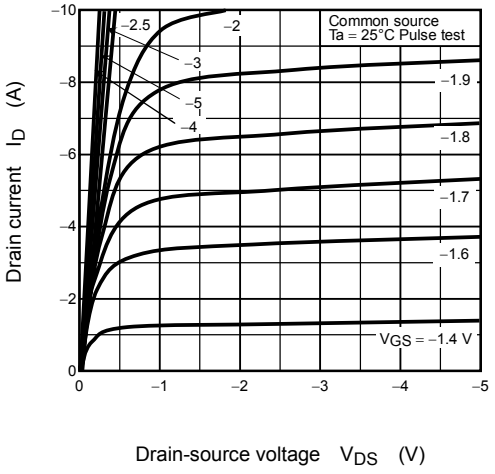
Be sure to take this into consideration when using the device. The V_{GS} recommended voltage for turning on this product is 1.5 V or higher.

Pch

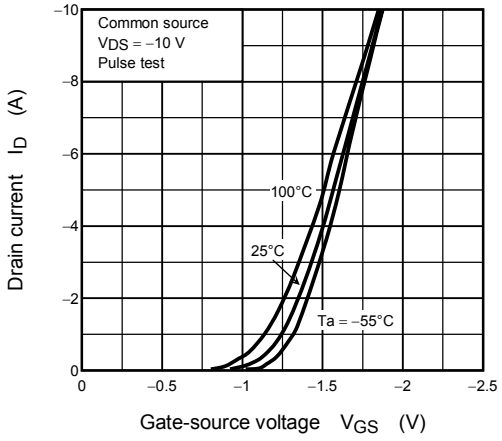
$I_D - V_{DS}$



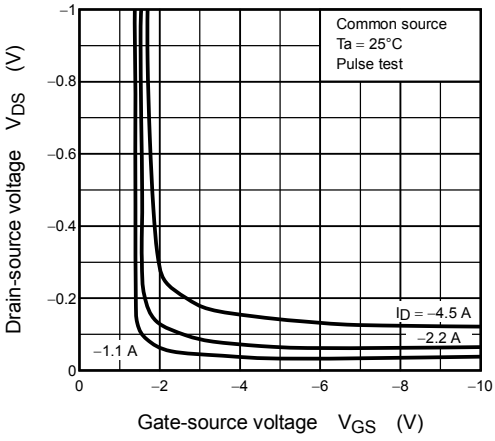
$I_D - V_{DS}$



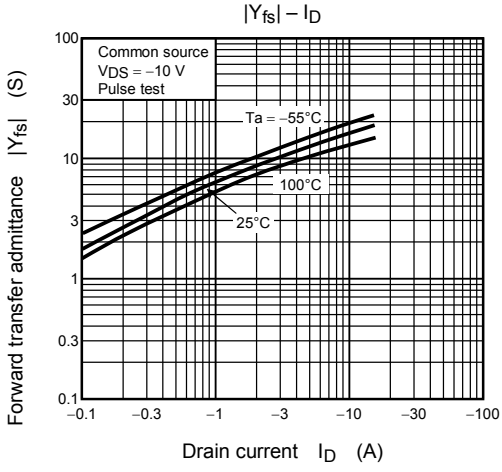
$I_D - V_{GS}$



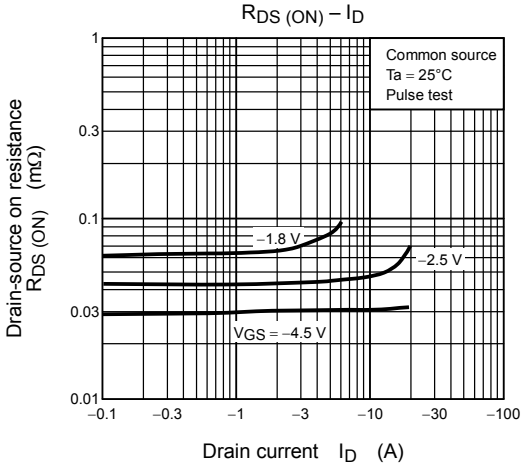
$V_{DS} - V_{GS}$



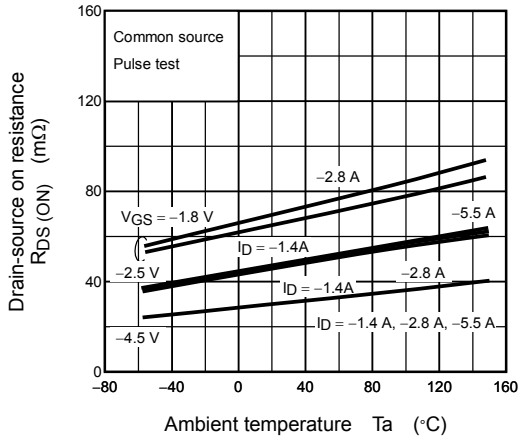
$|Y_{fs}| - I_D$



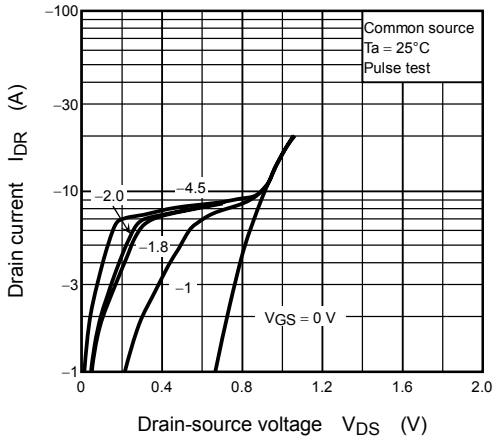
$R_{DS\ (ON)} - I_D$



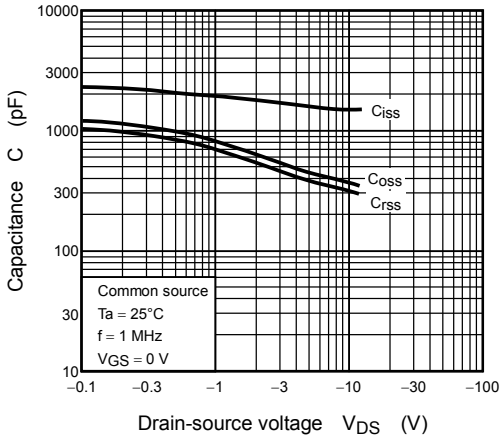
$R_{DS\ (ON)}$ – Ta



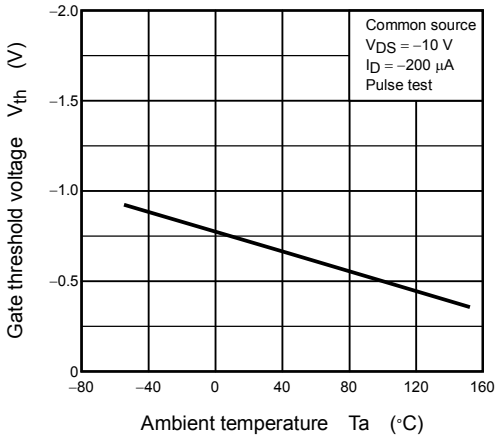
I_{DR} – V_{DS}



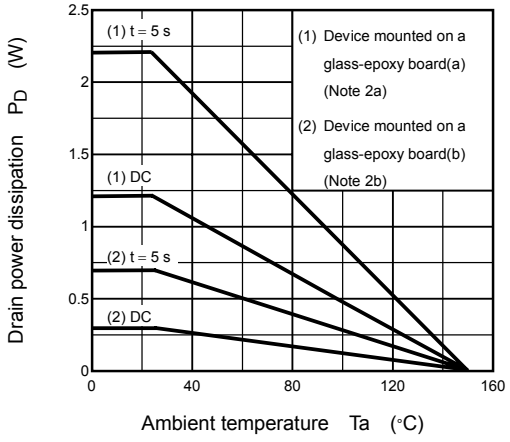
Capacitance – V_{DS}



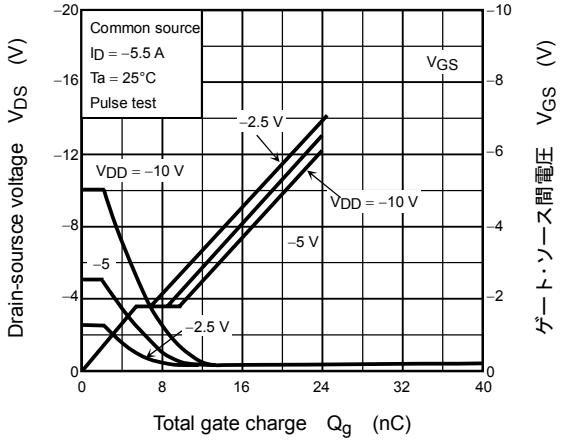
V_{th} – Ta



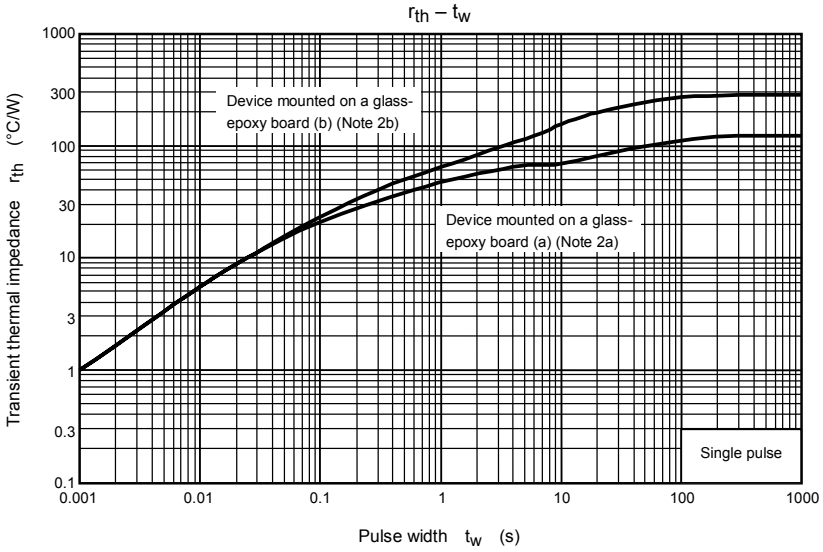
P_D – Ta



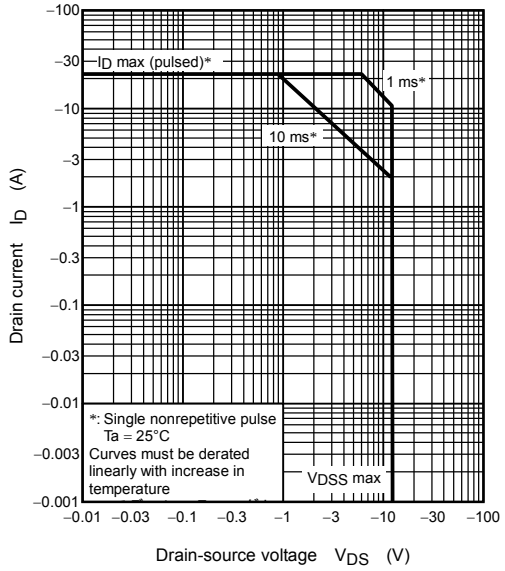
Dynamic input/output characteristics



$r_{th} - t_w$

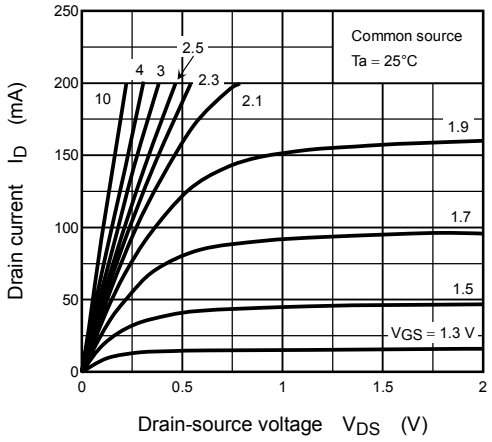


Safe operating area

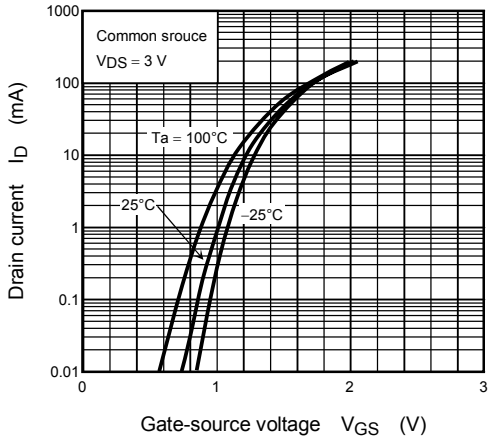


Nch

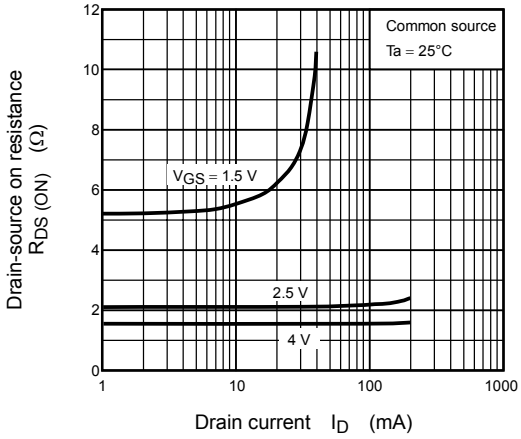
$I_D - V_{DS}$



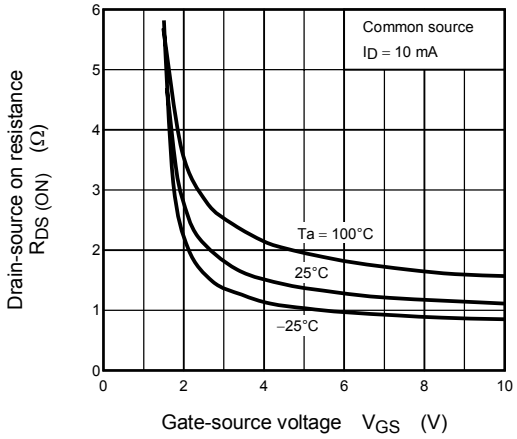
$I_D - V_{GS}$



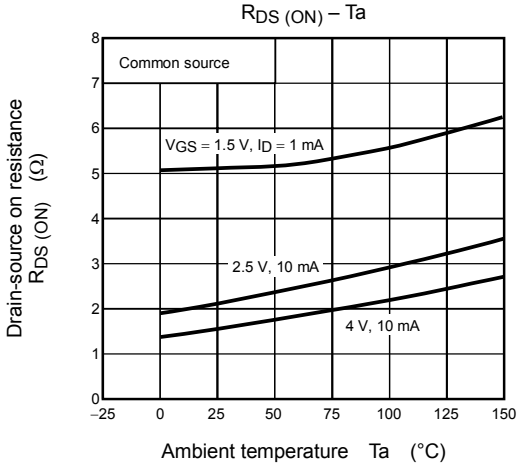
$R_{DS\ (ON)} - I_D$



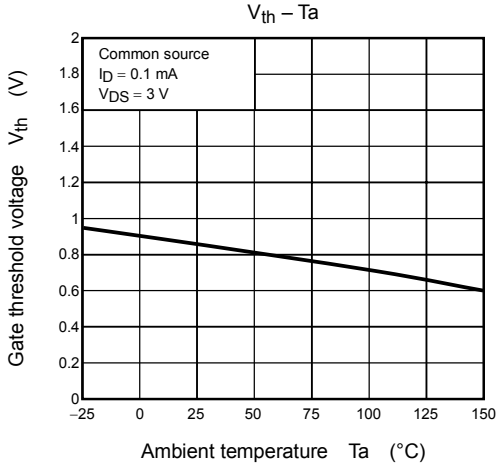
$R_{DS\ (ON)} - V_{GS}$



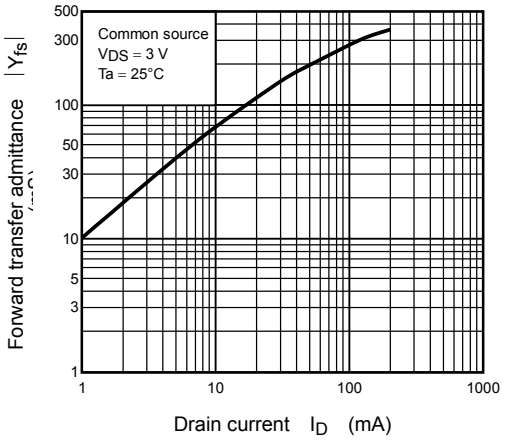
$R_{DS\ (ON)} - Ta$



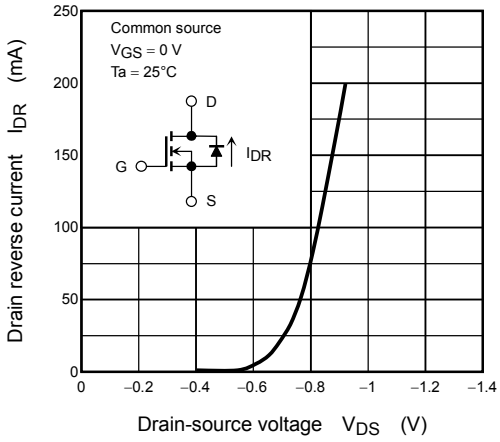
$V_{th} - Ta$



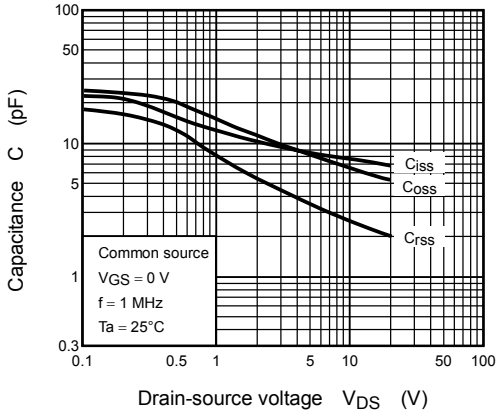
$|Y_{fs}| - I_D$



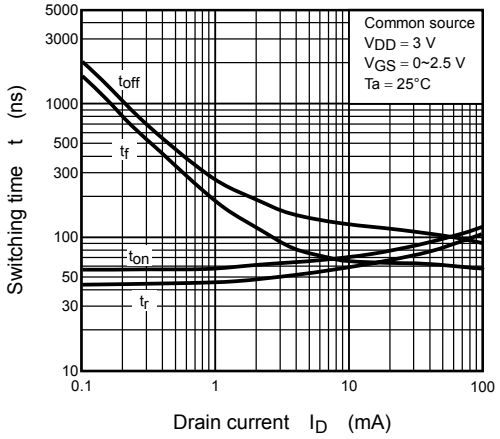
$I_{DR} - V_{DS}$



Capacitance – V_{DS}



$t - I_D$



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