DSP56603

Product Preview

16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56603 is a member of the DSP56600 core family of programmable CMOS Digital Signal Processors (DSPs). The DSP56600 core can execute one instruction per clock cycle. The 60 MHz chip includes a mixture of peripherals and large memories (3 K × 24 Program ROM, 16.5 K × 24 Program RAM, and 8 K × 16 X- and Y-data RAM each) optimized for processing-intensive, cost-effective, low power consumption digital mobile communications applications. A special Switch mode allows reconfiguration of on-chip memory. The DSP56600 core includes the Data Arithmetic Logic Unit (ALU), Address Generation Unit, Program Controller, Program Patch Detector, Bus Interface Unit, On-Chip Emulation (OnCE™)/JTAG port, and a Phase Lock Loop (PLL) based clock generator. The DSP56603 expansion area includes program and data memories, a triple timer module, an 8-bit Host Interface (HI08) port, and two 16-bit Synchronous Serial Interface (SSI) ports (see **Figure 1**). The DSP56603 also provides three to thirty-four GPIO lines, depending on which user-enabled peripherals are used, and four external dedicated interrupt lines. The DSP56603 is designed specifically for low-power digital handset wireless applications and can perform a wide variety of fixed-point digital signal processing algorithms. Because of its large RAM size, the DSP56603 supports rapid code development, shortening time to market. The ROM-based DSP56602 is the more cost-effective solution for mass production.

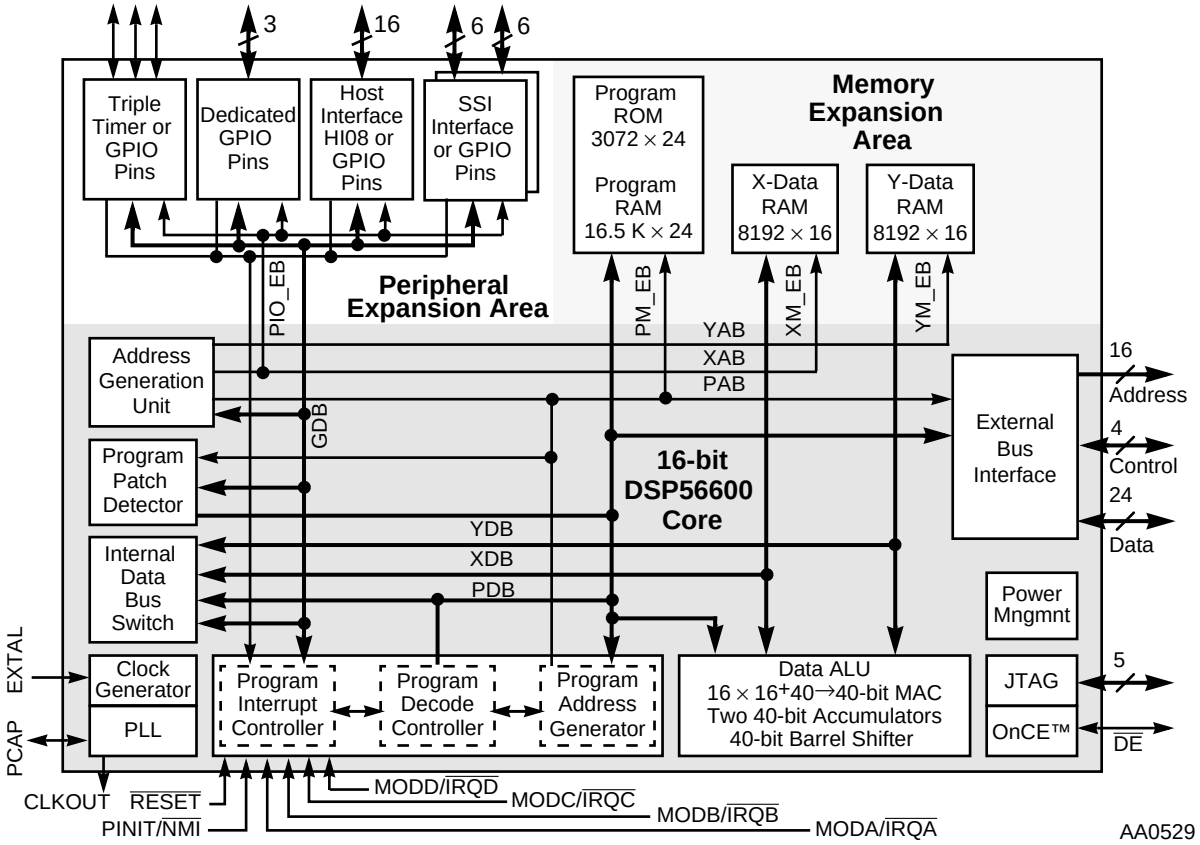

Figure 1 DSP56603 Block Diagram

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FEATURES

- Digital Signal Processing Core
  - High-performance DSP56600 core
  - Up to 60 Million Instructions Per Second (MIPS) at 2.7 V–3.3 V
  - Fully pipelined 16 × 16-bit parallel multiply-accumulator
  - Two 40-bit accumulators, including extension bits
  - 40-bit parallel barrel shifter
  - Highly parallel instruction set with unique DSP addressing modes
  - Code-compatible with the DSP56300 core
  - Position-independent code support
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip support for software patching and enhancements
  - On-chip PLL circuit
  - Real-time trace capability via external address bus
  - OnCE module and JTAG port
- Memory
  - Switch mode reconfigures program, X-data, and Y-data RAM sizes
    - Default configuration (Switch mode off)
      - 16.5 K × 24-bit Program RAM
      - 8 K × 16-bit X-data RAM
      - 8 K × 16-bit Y-data RAM
    - Switch mode on
      - 11.5 K × 24-bit Program RAM
      - 10.5 K × 16-bit X-data RAM
      - 10.5 K × 16-bit Y-data RAM
  - 3 K × 24-bit Program ROM
  - Off-chip expansion for both program fetch and program data transfers
  - Glueless interface to external SRAM

- Peripheral Circuits
  - Three dedicated General Purpose Input/Output (GPIO) pins and up to thirty-one additional GPIO pins (user-selectable as peripherals or GPIO pins)
  - Host Interface (HI08) support: One 8-bit parallel port (or up to sixteen additional GPIO pins)
    - Direct interface to Motorola HC11, Hitachi H8, 8051 family, Thomson P6 family
    - Minimal logic interface to standard ISA bus, Motorola 68K family, and Intel x86 microprocessor family
  - Synchronous Serial Interface (SSI) support: Two 6-pin ports (or twelve additional GPIO pins)
    - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola-SPI-compliant peripherals
    - Independent transmitter and receiver sections and a common SSI clock generator
    - Network mode using frame sync and up to 32 time slots
    - 8-bit, 12-bit, and 16-bit data word lengths
  - Three programmable timers (or up to three additional GPIO pins)
  - Four external interrupt/mode control lines
  - One external reset pin for hardware reset
- Energy Efficient Design
  - Operating voltage range: 1.8 V to 3.3 V
  - Very low power CMOS design
    - < 0.85 mA/MIPS at 2.7 V
    - < 0.55 mA/MIPS at 1.8 V
  - Low power wait for Interrupt standby mode
  - Ultra low power Stop standby mode (< 50 μA)
  - Fully static, HCMOS design for operating frequencies from 60 MHz down to DC
  - Special power management circuitry

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56603 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 Reference Documentation

Document Name	Description	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core architecture, 16-bit DSP core processor, and the instruction set	DSP56600FM/AD
DSP56603 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56603UM/AD
DSP56603 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56603/D

How to reach us:

USA/Europe:
Motorola Literature Distribution
P.O. Box 20912
Phoenix, Arizona 85036
1 (800) 441-2447

MFAX:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609

Hong Kong:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-2662928

Technical Resource Center:
1 (800) 521-6274

DSP Helpline:
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
Tatsumi-SPD-JLDC
Toshikatsu Otsuki
6F Seibu-Butsuryu-Center
3-14-2 Tatsumi Koto-Ku
Tokyo 135, Japan
03-3521-8315

Internet:
http://www.motorola-dsp.com

MOTOROLA