ADVANCE INFORMATION

87C51FA/87C51FB/87C51FC/87C51FC-20
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Automotive

- **FX Core Architecture Device**
- **Extended Automotive Temperature Range (−40°C to +125°C Ambient)**
- **Available in 12 MHz, 16 MHz and 20 MHz Versions**
- **High Performance CHMOS EPROM**
- **Three 16-Bit Timer/Counters**
  - **— Timer 2 (Up/Down Counter)**
- **Programmable Counter Array with:**
  - **— High Speed Output,**
  - **— Compare/Capture,**
  - **— Pulse Width Modulator,**
  - **— Watchdog Timer Capabilities**
- **One-to-Three Level Program Lock System on EPROM**
- **8K On-Chip User Programmable EPROM in 87C51FA**
- **16K On-Chip User Programmable EPROM in 87C51FB**
- **32K On-Chip User Programmable EPROM in 87C51FC**
- **256 Bytes of On-Chip Data RAM**
- **Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **7 Interrupt Sources**
- **Four Level Interrupt Priority**
- **Programmable Serial Channel with:**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS®-51 Fully Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **RFI Reduction Mode**
- **Available in PLCC and PDIP Packages**

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the 87C51FA On-Chip EPROM. Up to 16 Kbytes of the program memory can reside in the 87C51FB on-chip EPROM. Up to 32 Kbytes of the program memory can reside in the 87C51FC on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51FA/87C51FB/87C51FC is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS EPROM technology. Being a member of the MCS-51 family, the 87C51FB/87C51FC uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products. The 87C51FA is an enhanced version of the 87C51. The 87C51FB is an enhanced version of the 87C51FA. The 87C51FC is an enhanced version of the 87C51FB. With 8 Kbytes of program memory in the 87C51FA and 16 Kbytes of program memory in the 87C51FB and 32 Kbytes of program memory in the 87C51FC, it is an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O, and up/down counting capabilities such as brake and traction control.

For the remainder of this document, the 87F51FA, 87C51FB and 87C51FC will be referred to as the 87C51FA/FB/FC.

September 1993 **Order Number: 270961-003**

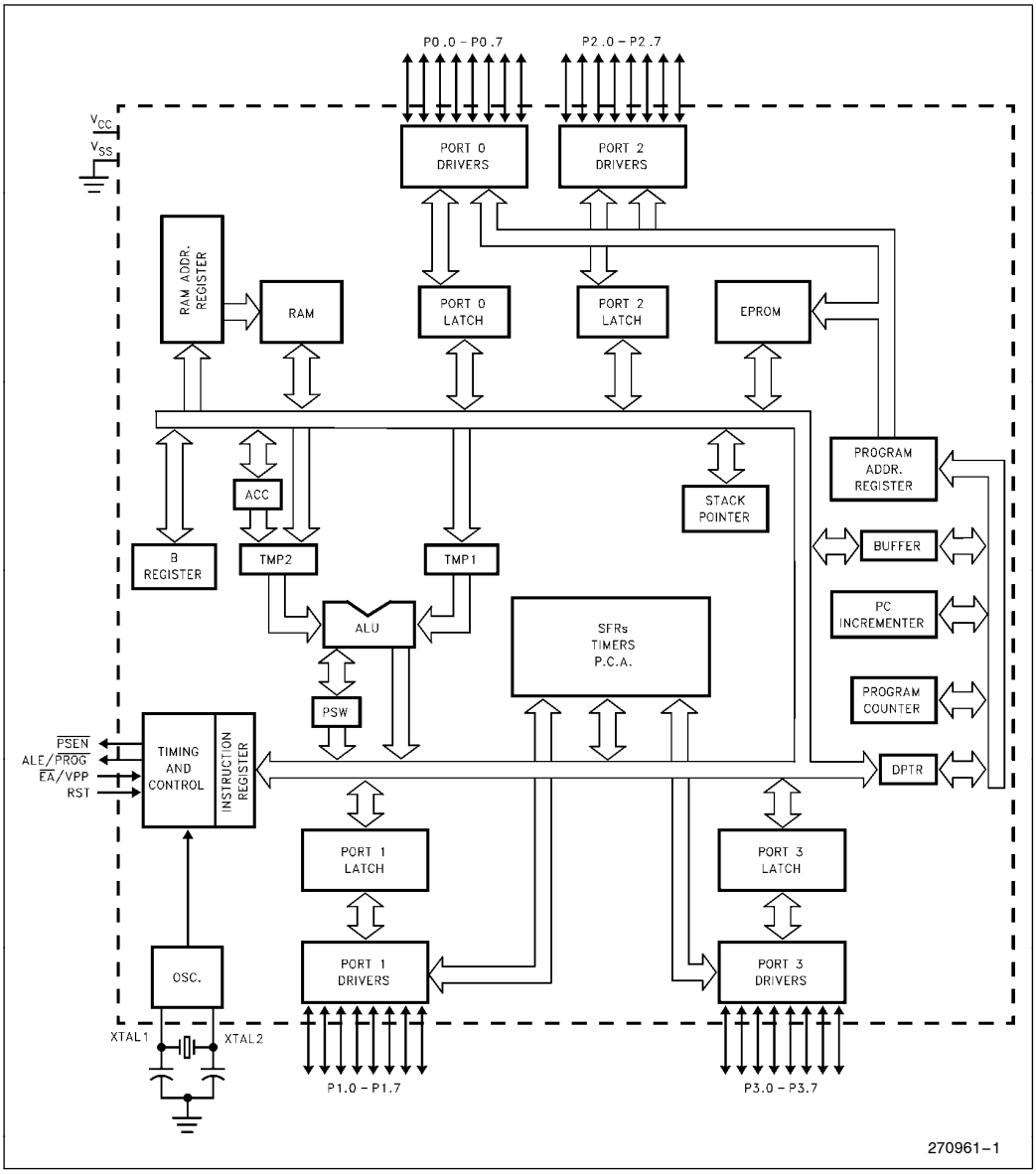


Figure 1. 87C51FB/FC Block Diagram

87C51FA/FB/FC PRODUCT OPTIONS

Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over the temperature

range of −40°C to +85°C ambient. For the automotive temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +125°C ambient. The automotive, extended, and commercial temperature versions of the MCS-51 product families are available with or without burn-in options.

As shown in Figure 2 temperature, burn-in, and package options are identified by a one- or two-letter prefix to the part number.

PIN DESCRIPTIONS

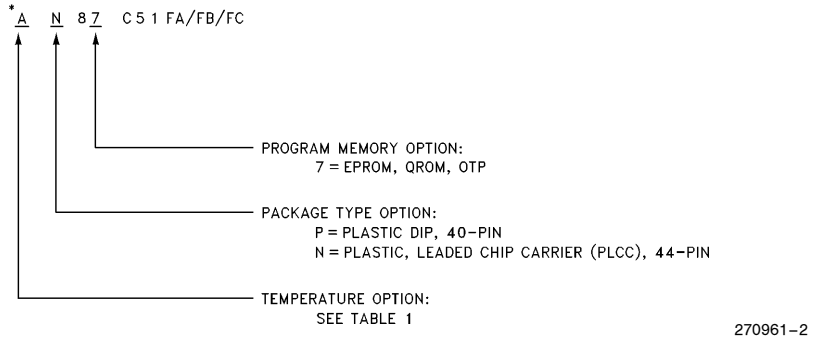
V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

V_{SS1}: Secondary ground (in PLCC only). Provided to reduce ground bounce and improve power supply by-passing.

NOTE:
This pin is NOT a substitute for V_{SS} pin (pin 22).

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.



***Example:**
AN87C51FA/FB/FC indicates an automotive temperature range version of the 87C51FA/FB/FC in a PLCC package with 16 Kbyte/32 Kbyte EPROM program memory.

Figure 2. Package Options

Table 1. Temperature Options

Temperature Classification	Temperature Designation	Operating Temperature °C Ambient	Burn-In Options
Extended	T	−40 to +85	Standard
	L	−40 to +85	Extended
Automotive	A	−40 to +125	Standard
	B	−40 to +125	Extended

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 87C51FB/FC:

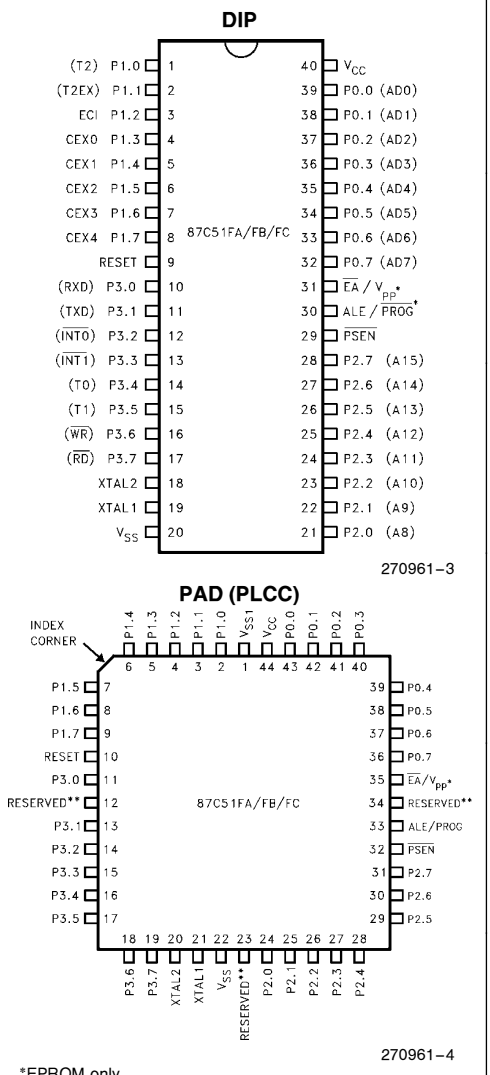
Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/Counter 2)
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

PACKAGES

Part	Prefix	Package Type
87C51FA/FB/FC	P N	40-Pin Plastic DIP 44-Pin PLCC



*EPROM only
**Do not connect reserved pins.

Diagrams are for pin reference only. Package sizes are not to scale.

Figure 3. Pin Connections (Top View)

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} is applied, whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the 87C51FA/FB/FC.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 87C51FA/FB/FC is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

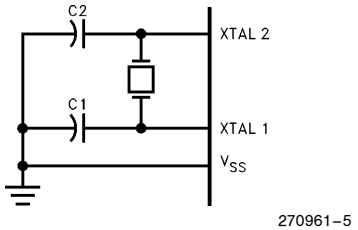
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, ''Oscillators for Microcontrollers'', and in Application Note AP-486, *''Oscillator Design for Microcontrollers''.*

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 4. Oscillator Connections

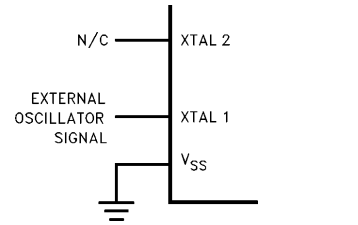


Figure 5. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 87C51FA/FB/FC either a hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt. INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator (the oscillator must be allowed time to stabilize after start up, before this pin is released high) but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the 87C51FA/FB/FC without removing it from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51FA/FB/FC is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

RFI REDUCTION MODE

The RFI reduction feature can be used only if external program memory is not required since this mode disables the ALE pin during instruction code fetches. By writing a logical one to the LSB of the Auxiliary Register (address 08EH), the ALE is disabled for instruction code fetches and the output is weakly held high. When a logical zero is written, the ALE pin is enabled allowing it to generate the Address Latch Enable signal. This bit is cleared by reset. Once disabled, ALE remains disabled until it is reset by software or until a hardware reset occurs.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Applications Handbook, and Application Note AP-252, ''Designing with the 80C51BH.''

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias −40°C to +125°C

Storage Temperature .....−65°C to +150°C

Voltage on EA/V_{PP} Pin to V_{SS} .....0V to +13.0V

Voltage on Any Other Pin to V_{SS} ..−0.5V to +6.5V

I_{OL} Per I/O Pin .....15 mA

Power Dissipation.....1.5W
(Based on package heat transfer limitations, not device power consumption)

Typical Junction Temperature .....+135°C
(Based on ambient temperature at +125°C)

Typical Thermal Resistance Junction-to-Ambient (θ_{JA}):
PDIP .....45°C/W
PLCC .....46°C/W

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

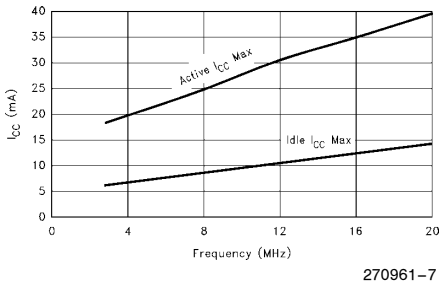
ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

DC CHARACTERISTICS: (T_A = −40°C to +125°C; V_{CC} = 5V ± 20%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ (Note 4)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST, $\overline{EA}$)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage **(Note 5)** (Ports 1, 2 and 3)			0.3	V	I_{OL} = 100 μA (Note 1)
				0.45	V	I_{OL} = 1.6 mA (Note 1)
				1.0	V	I_{OL} = 3.5 mA (Note 1)
V_{OL1}	Output Low Voltage **(Note 5)** (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA (Note 1)
				0.45	V	I_{OL} = 3.2 mA (Note 1)
				1.0	V	I_{OL} = 7.0 mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2 and 3)	V_{CC} − 0.3			V	I_{OH} = −10 μA
		V_{CC} − 0.7			V	I_{OH} = −30 μA
		V_{CC} − 1.5			V	I_{OH} = −60 μA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	V_{CC} − 0.3			V	I_{OH} = −200 μA
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)			−75	μA	V_{IN} = 0.45V
I_{LI1}	Input Leakage Current ($\overline{Port\ 0}$)			±10	μA	0.45V < V_{IN} < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			−750	μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	40		225	KΩ	
CIO	Pin Capacitance		10		pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Running at 16/20 MHz (Figure 6) Idle Mode at 16/20 MHz (Figure 6) Power Down Mode		 26/28 5 15	 35/40 12/14 100	 mA mA μA	(Note 3)

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with Schmitt triggers or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2V.
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (1.25 × Osc Freq) + 15
Idle Mode
I_{CC} Max = (0.5 × Osc Freq) + 4
Where Osc Freq is in MHz, I_{CC} is in mA.

Figure 6. I_{CC} vs Frequency

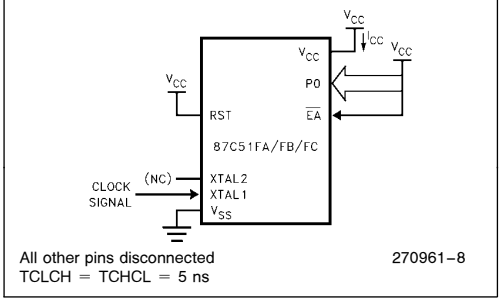


Figure 7. I_{CC} Test Condition, Active Mode

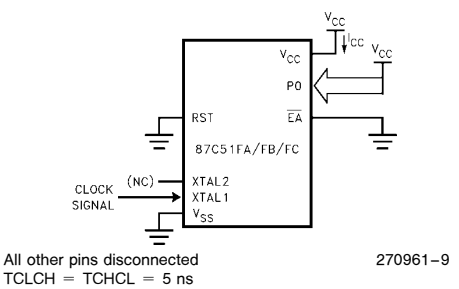


Figure 8. I_{CC} Test Condition Idle Mode

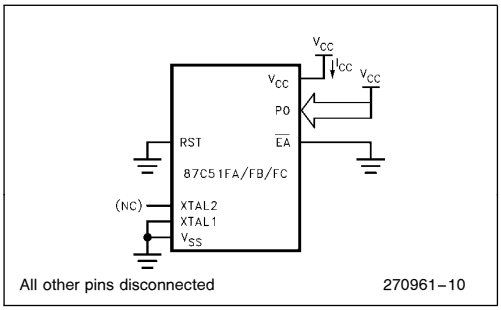


Figure 9. I_{CC} Test Condition, Power Down Mode. V_{CC} = 2.0V to 5.5V.

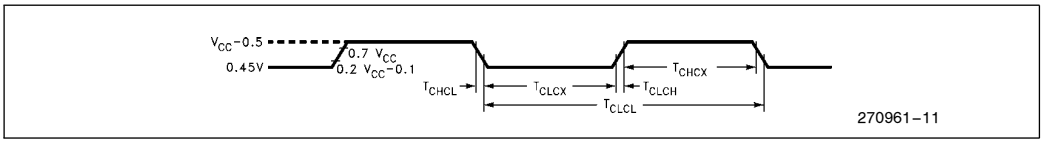


Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

T_{AVLL} = Time from Address Valid to ALE Low
T_{LLPL} = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS ($T_A = -40°C$ to $+125°C$, $V_{CC} = 5V \pm 20\%$, $V_{SS} = 0V$, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and $\overline{\text{PSEN}}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	87C51FA/FB/FC/87C51FC-20		
				Min	Max	
$1/T_{CLCL}$	Oscillator Frequency			3.5	16/20	MHz
T_{LHLL}	ALE Pulse Width	127		$2T_{CLCL} - 40$		ns
T_{AVLL}	Address Valid to ALE Low	43		$T_{CLCL} - 40$		ns
T_{LLAX}	Address Hold After ALE Low	53		$T_{CLCL} - 30$		ns
T_{LLIV}	ALE Low to Valid Instruction In		234		$4T_{CLCL} - 100$/ $4T_{CLCL} - 75$*	ns
T_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	53		$T_{CLCL} - 30$		ns
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3T_{CLCL} - 45$		ns
T_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3T_{CLCL} - 105$/ $3T_{CLCL} - 90$*	ns
T_{PXIX}	Input Inst. Hold After $\overline{\text{PSEN}}$ Trans	0		0		ns
T_{PXIZ}	Input Inst. Float After $\overline{\text{PSEN}}$ Trans		59		$T_{CLCL} - 25$/ $T_{CLCL} - 20$*	ns
T_{AVIV}	Address Valid to Valid Instruction In		312		$5T_{CLCL} - 105$	ns
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
T_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6T_{CLCL} - 100$		ns
T_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6T_{CLCL} - 100$		ns

AC CHARACTERISTICS (T_A = −40°C to +125°C, V_{CC} = 5V ± 20%, V_{SS} = 0V, Load Capacitance for Port 0, ALE/$\overline{PROG}$ and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF) (Continued)

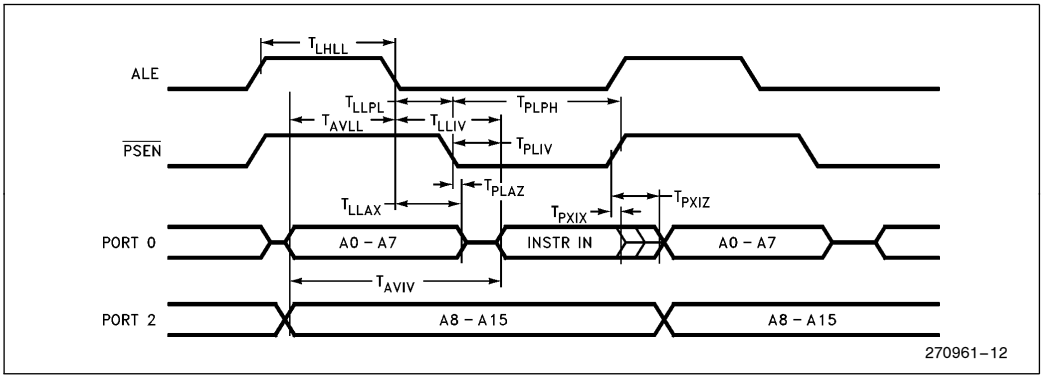
ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

EXTERNAL PROGRAM MEMORY CHARACTERISTICS (Continued)

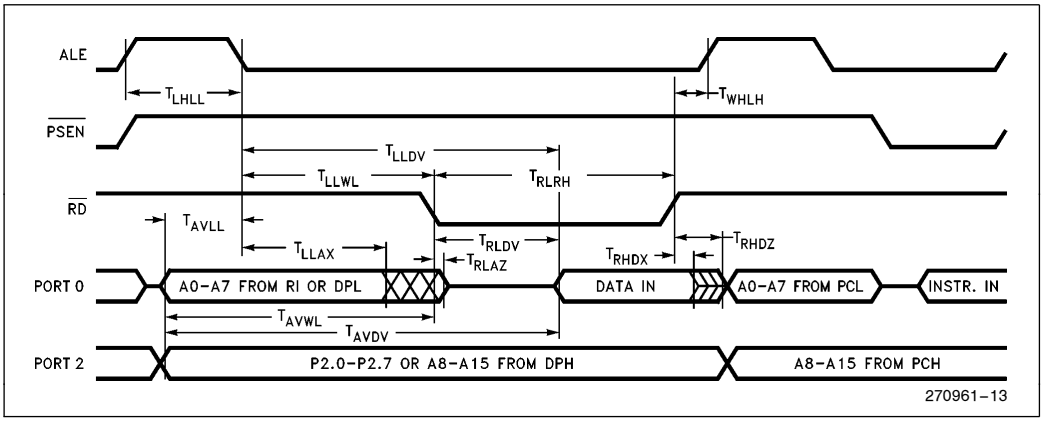
Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
				87C51FA/FB/FC/87C51FC-20		
		Min	Max	Min	Max	
T_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5T_{CLCL} - 165$/ $5T_{CLCL} - 95$*	ns
T_{RHDX}	Data Hold After $\overline{RD}$ High	0		0		ns
T_{RHDZ}	Data Float After $\overline{RD}$ High		107		$2T_{CLCL} - 60$	ns
T_{LLDV}	ALE Low to Valid Data In		517		$8T_{CLCL} - 150$/ $8T_{CLCL} - 90$*	ns
T_{AVDV}	Address Valid to Valid Data In		585		$9T_{CLCL} - 165$/ $9T_{CLCL} - 90$*	ns
T_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3T_{CLCL} - 50$	$3T_{CLCL} + 50$	ns
T_{AVWL}	Address Valid to $\overline{WR}$ Low	203		$4T_{CLCL} - 130$/ $4T_{CLCL} - 90$*		ns
T_{QVWX}	Data Valid before $\overline{WR}$ Low	33		$T_{CLCL} - 50$/ $T_{CLCL} - 35$*		ns
T_{WHQX}	Data Hold after $\overline{WR}$ High	33		$T_{CLCL} - 50$/ $T_{CLCL} - 40$*		ns
T_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7T_{CLCL} - 150$/ $7T_{CLCL} - 70$*		ns
T_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	$T_{CLCL} - 40$	$T_{CLCL} + 40$	ns

NOTE:
*Timings specified for the 87C51FC-20 are valid at 20 MHz only. For timing information below 20 MHz, use the 87C51FA/FB/FC timings.

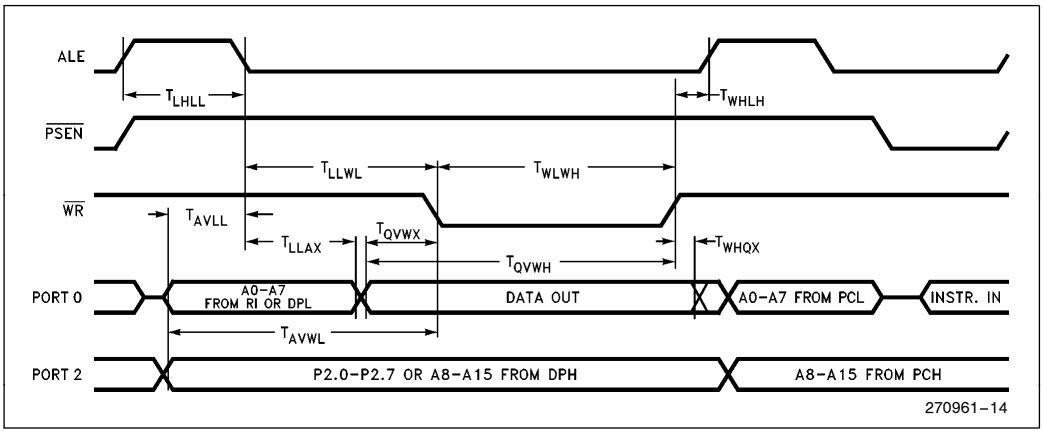
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

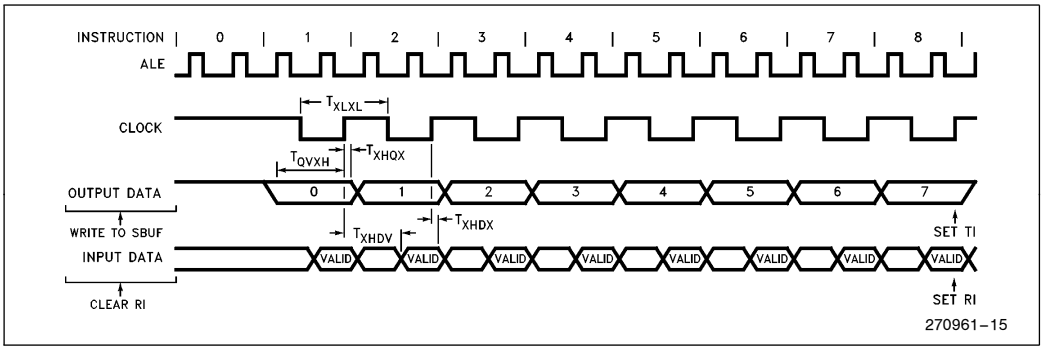


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5V \pm 20\%$; $V_{SS} = 0V$; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1		$12T_{CLCL}$		μs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10T_{CLCL} - 133$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	50		$2T_{CLCL} - 117$		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10T_{CLCL} - 133$	ns

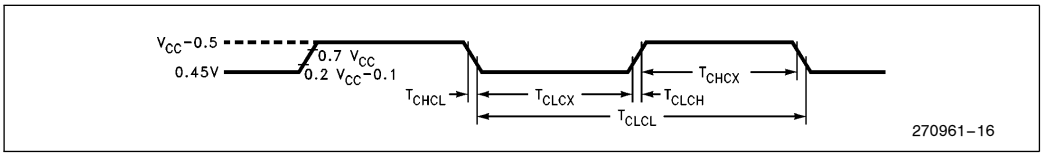
SHIFT REGISTER MODE TIMING WAVEFORMS



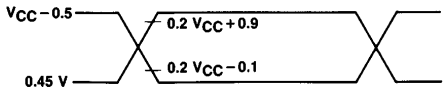
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency 87C51FA/FB/FC	3.5	16/20	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORMS



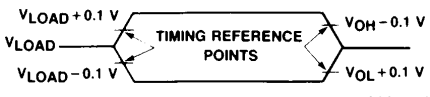
AC TESTING INPUT, OUTPUT WAVEFORMS



270961–17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



270961–18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Table 3. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⎍	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

DEFINITION OF TERMS (EPROM PROGRAMMING)

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4–P3.5 respectively for A0–A13.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}$/V_{PP}

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 3. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

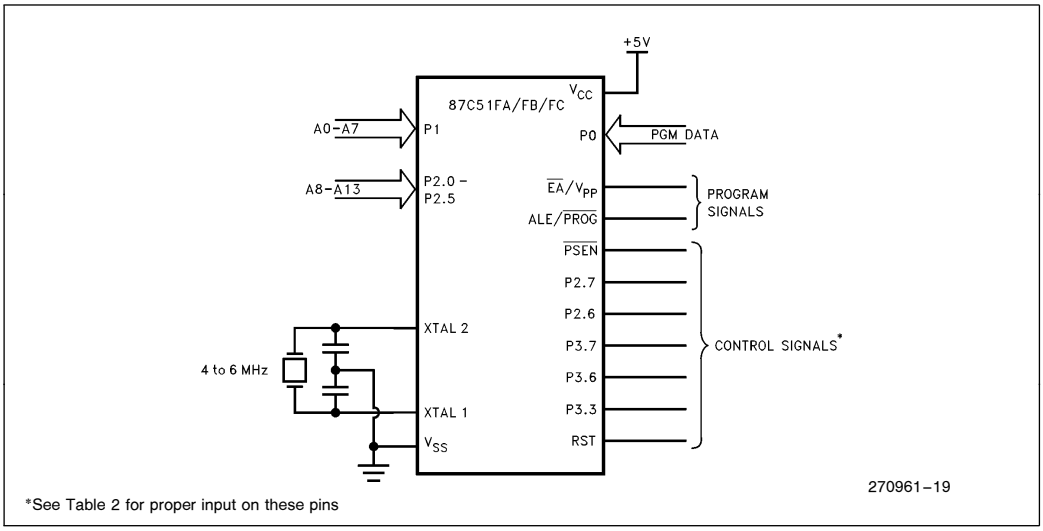


Figure 11. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 3 and Figures 11 and 12 for address, data, and control signals set up. To program the 87C51FA/FB/FC the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V $\pm$0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte or block of bytes is programmed. In either case a complete verify of the programmed array will ensure reliable programming of the 87C51FA/FB/FC.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet.

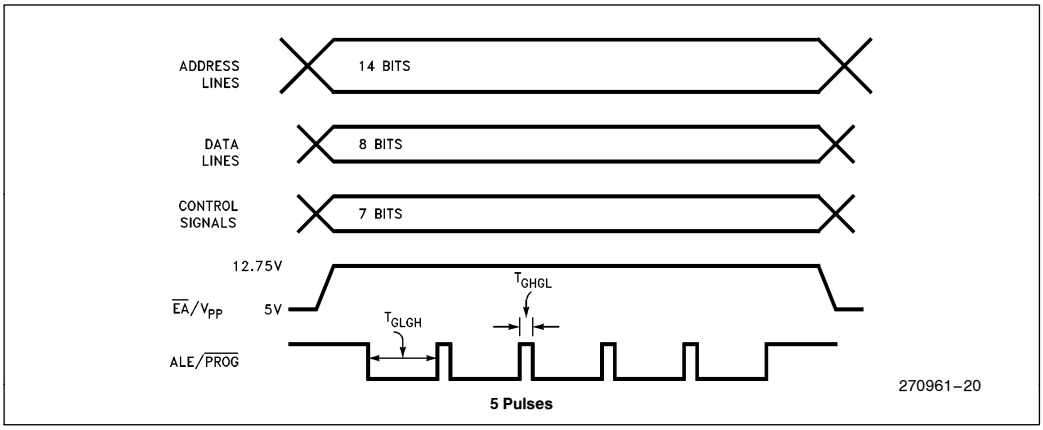


Figure 12. Programming Signal's Waveforms

EPROM Program Lock

The 87C51FA/FB/FC program lock system, when programmed, protects the onboard program against software piracy.

The 87C51FA/FB/FC has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user programmable. See Table 4.

Program Lock Bits

The 87C51FA/FB/FC has 3 programmable lock bits that when programmed according to Table 4 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form. For programming the Encryption Array, refer to Table 3 (EPROM Programming Mode).

Reading the Signature Bytes

The 87C51FA/FB/FC has 3 signature bytes in locations 30H, 31H and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 3 for Read Signature Byte.

Location: 30H = 89H
31H = 58H
60H = FBH (for an FB part)
60H = FCH (for an FC part)

Table 4. Program Lock Bits and the Features

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

Any other combination of the lock bits is not defined.

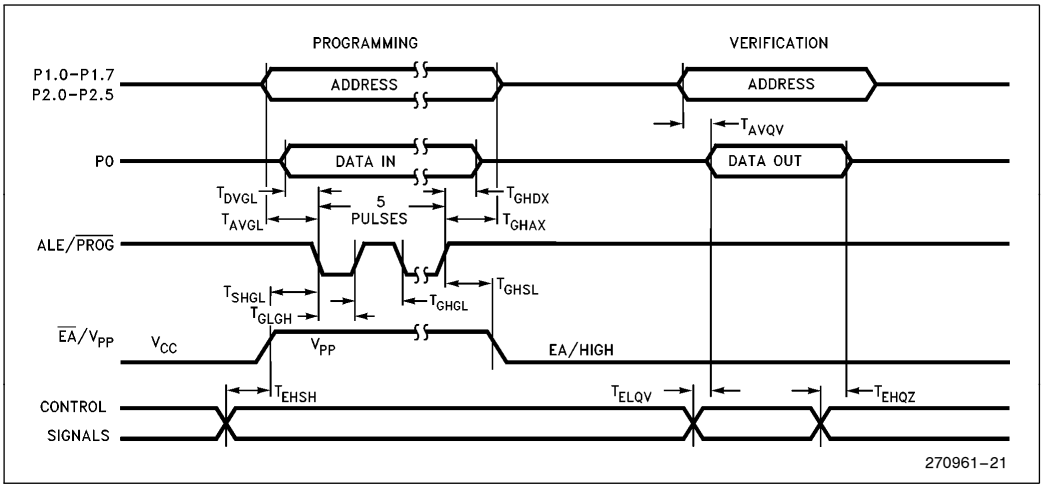
EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHAX}	Address Hold after $\overline{PROG}$	$48T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{PROG}$	$48T_{CLCL}$		
T_{EHSH}	(Enable) High to V_{PP}	$48T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{CLCL}$	
T_{GHGL}	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION HISTORY

The following are key differences between this data sheet and the -002 revision of the data sheet:

1. The data sheet has been revised from the 87C51FB/87C51FC to the 87C51FA/87C51FB/87C51FC/87C51FC-20 and includes the 20 MHz 87C51FC.
2. RST pin in Figure 3 has been changed to RESET pin.
3. Reference to Application Note AP-486 was added on page 5.
4. The I_{CC} specification has been corrected in the D.C. Characteristics section.
5. The 20 MHz I_{CC} max values have been added.
6. 20 MHz 87C51FC timings information were added to the External Program Memory Characteristics table.

DATA SHEET REVISION HISTORY

The following are key differences between this data sheet and the -001 version of the data sheet:

1. ''NC'' pin labels changed to ''Reserved'' in Figure 3.
2. Capacitor value for ceramic resonators deleted in Figure 4.
3. Replaced A0–A15 with P1.0–P1.7, P2.0–P2.5 (EPROM programming and verification waveforms).
4. Replaced D0–D7 with P0 (EPROM programming and verification waveforms).
5. Combined the 87C51FB and 87C51FC data sheets.

The following are the key differences between the previous 87C51FB data sheet versions and this new data sheet (rev-001):

1. The data sheet has been revised from a 83C51FB/87C51FB to an 87C51FB data sheet only.
2. The data sheet has been revised to specify AC and DC parameters to $V_{CC} = 5V \pm 20\%$ instead of $V_{CC} = 5V \pm 10\%$.
3. The 87C51FB is now offered in a 3.5 MHz–20 MHz version.
4. The RST description has been modified to clarify the reset operation when the oscillator is not running.
5. Figure 4 (Oscillator Connections) has been changed for Ceramic Resonators.
6. A description of RFI Reduction Mode has been added.
7. V_{OH1}, I_{IL}, I_{TL} and I_{CC} DC Characteristics have been revised.
8. Note 1 of the DC Characteristics has been clarified.
9. The External Clock Drive diagram has been modified to include 16 MHz and 20 MHz device types.
10. The Float Waveforms diagram has been revised for greater clarity.
11. Table 4, EPROM Programming Modes, has been modified, included logic levels for P3.3 and three program lock bits.
12. The Encryption Array section now states that six address lines are used to select a byte from the Encryption Array instead of five.
13. The I_{PP} specification in the EPROM Programming and Verification Characteristics has been increased to 75 mA.