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FEBRUARY 1995

ADVANCE INFORMATION

DS3715 - 2.1

PDSP16540

32K BUCKET BUFFER

(Supersedes version in December 1993 Digital Video & Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16540 Bucket Buffer is for use in systems which require a reservoir in which a block of data is accumulated, whilst previous data is being transferred to other system elements and then processed. It thus prevents the loss of incoming data whilst the previous block is being processed. Like a FIFO all address are generated internally.

It differs from a normal FIFO, however, by allowing the user to define both the length of the data block and also the amount of the old data to be re-read before the new data is added. The latter feature supports the block overlapping requirements of Digital Signal Processing Systems performing Fast Fourier Transforms. It also provides wide, 32 bit, input and output buses, unlike normal byte wide FIFO's. This wide configuration supports the16 bit real and imaginary components of the complex data found in many DSP systems.

In particular, the device can be directly connected to the PDSP16510 FFT Processor without any external logic. The FFT Processor requires the support of an input buffer when 1024 point transforms are to be continuously performed and no incoming data is to remain un-processed.

The number of words, which are read as a complete block, can be programmed in multiples of 32 up to a maximum of 1024. The amount of new data in this block can separately be programmed in multiples of 32 words. In this manner the percentage of new data in a complete block is under the control of the user, and the device is not restricted to only supporting the requirements of the PDSP16510.

A Read Me Flag is raised at a user defined point during the loading of new data. This allows the next system component to prepare itself to accept data. Data is not actually transferred, however, until all the user defined amount of new data has been loaded, and a Data Available Flag goes active. The gap between the two flags can be programmed to provide sufficient time to prepare the device which is to accept data from the buffer. This provide a much more flexible solution than the simple Full Flag offered by a standard FIFO.

ASSOCIATED PRODUCTS

PDSP16510 FFT Processor

PDSP16520 Quad Port Synchronous RAM

PDSP16116 Complex Multiplier

PDSP16318 Complex Accumulator

PDSP16330 Cartesian to Polar Converter

PDSP16340 Polar to Cartesian Converter

FEATURES

- 1K x 32 bit dual port RAM for use as a reservoir in data flow systems
- Up to 40 MHz read rates and 16 MHz write rates
- Buffer size user programmable up to 1k words
- A user programmble amount of old data can be re-read before new data is added
- Provides the input buffer requirements for the PDSP16510 FFT Processor when 1024 point continuous transforms are performed
- User programmable get ready to Read Me Flag
- Data Available Flag indicates the required amount of new data has been acquired
- 84 Pin PGA or 132 Pin QFP

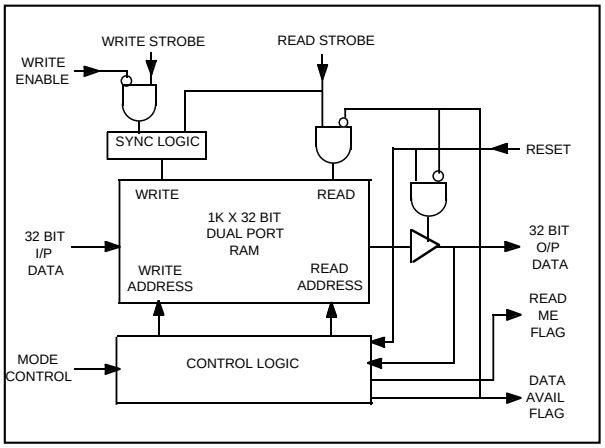
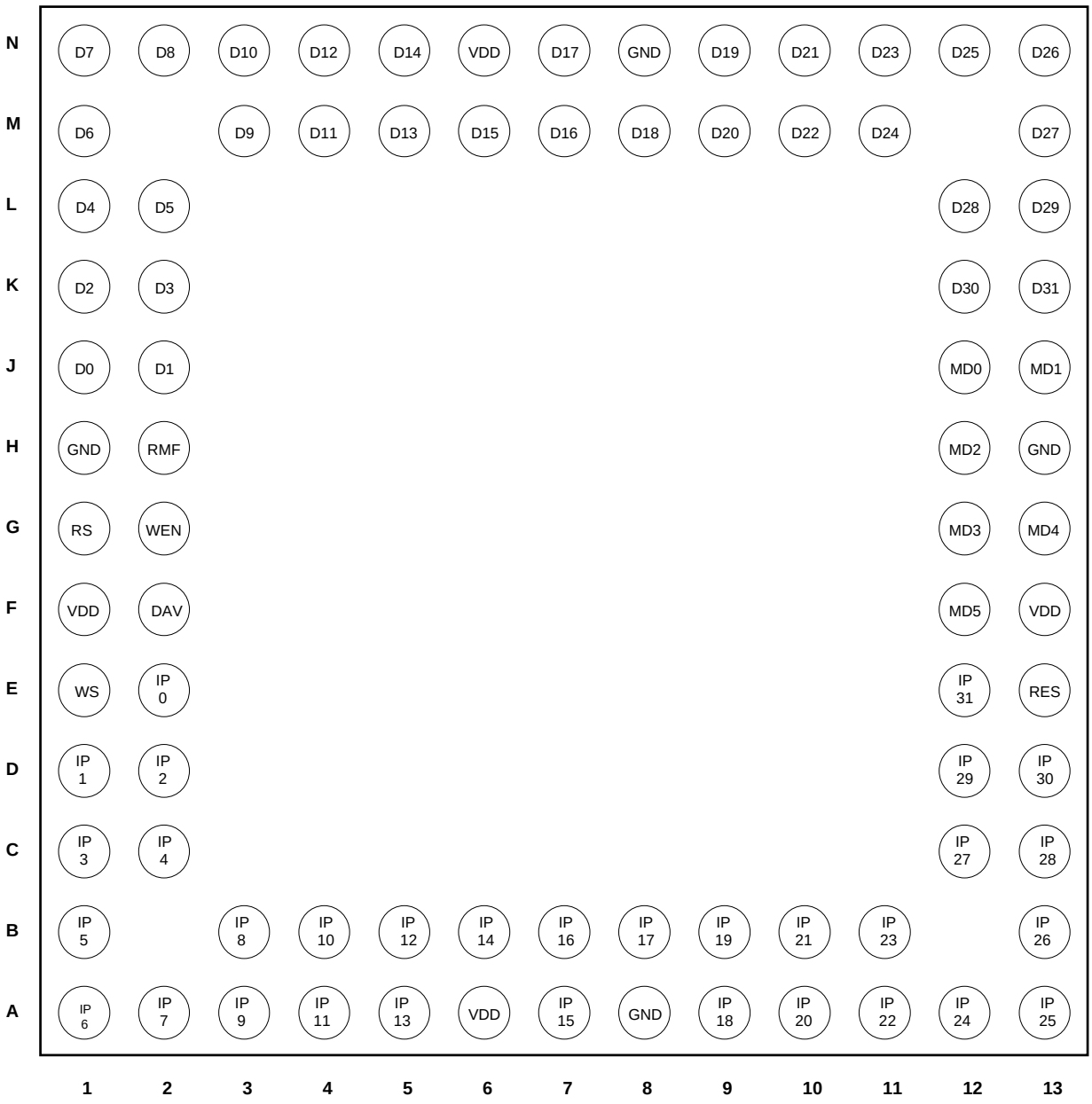


Figure 1. Simplified Block Diagram

NAME	TYPE	SIGNAL DESCRIPTION
IP31:0	I/P	32 bit input bus. If MD5 is high, pins IP16:31 are redundant
D31:0	O/P	32 bit output bus. This bus will be high impedance until the Data Available Flag is active. It then remains low impedance until the required amount of data has been read. D15:0 become inputs during reset, and may be used to define the operating conditions.
RS	I/P	The read strobe must be continuous, and the rising edge transfers data to the output pins.
WS	I/P	Write strobe used to load data into the internal RAM. This strobe may be asynchronous to the read strobe, and may be continuous or intermittent.
$\overline{WEN}$	I/P	Write enable which when low allows the write strobe to load data.
$\overline{DAV}$	O/P	Data Available Flag. This signal goes active low when the required amount of new data has been written to the RAM. The complete block of data will then be read from the RAM in sequence using the read strobe. The next system component must be ready to accept the information, which will consist of both new and old data, in amounts defined by MD2:1. The flag will go in-active for one read strobe period every time new data is written to the RAM, and stays in-active when the complete block has been transferred.
RMF	O/P	Read Me Flag. This signal goes active high when a user defined amount of new data has been written to the RAM. It can go active before DAV goes active, and thus allows the system to prepare itself for data when it becomes available. It stays active until the complete block has been read.
MD0	I/P	When MD0 is low the block length is 1024 words. When it is high the block length is defined in groups of 32 words by the data on D4:0 during reset.
MD2:1		MD2:1 define the amount of new data within the block length as defined above. The options are 1024 (00), 512 (01), 256 (10), or the number defined in groups of 32 words by D9:5 during reset (11). When the number of new words is less than the block length defined by MD0, the first words read from the RAM will be data previously stored.
MD4:3	I/P	MD4:3 define the number of new words which are written before the Read Me Flag goes active. The options are 1024, 512, 256 or the number defined in groups of 16 words by D15:10 during reset.
MD5	I/P	When this pin is high the device will support the real transform mode of the PDSP16510. Only IP15:0 input pins are then used and 2 blocks are acquired before the flags go active. Both blocks are then read in parallel using the 32 output pins.
RES	I/P	When this pin is low outputs D15:0 become inputs, which are used to define the operating mode if the internal options have not been selected. The input can be power on reset.
GND	I/P	Four ground pins. All must be connected
VCC	I/P	Four +5 volt pins.All must be connected



Pin Out Diagram - Bottom View (84pin PGA - AC84)

FUNCTIONAL DESCRIPTION

The PDSP16540 is designed for use in synchronous data flow systems in which the transfer between system elements is contolled by a continuously available system clock. This system clock is usually at the maximum rate that the system elements will allow, since it is governing the rate at which processing can be performed on the acquired data. The rate at which external data is actually inputed to the system (the sampling rate in DSP terminology) is usually much slower than the internal system, or computational, rate. The PDSP16540 then provides a reservoir for data which is acquired at the sampling rate and then processed with the higher speed system clock rate.

Data is written to the RAM using an asynchronous write strobe when a write enable input is active. The enbling signal must meet the set up and hold times given in Table 1. Data is read from the RAM using a read strobe which is expected to be continuously availble and not to just go active when read operations are actually needed. It is normally the high speed system clock discussed earlier. All RAM addresses are generated internally since the device is partitioning consecu-

tive data inputs into pre-defined blocks, which are then transferred to the rest of the system at the system clock rate.

All internal read and write operations are actually performed by the continuous read strobe. When a write strobe is received, internal syncronization occurs and the write operation is actually done with the read strobe. If data is being read from the RAM when a write operation is requested, the read sequence will be interupted for one read strobe period. The flag indicating that data is available goes in-active for this strobe period and the next system element should not accept data during this perfiod.

The correct operation of the write synchronization circuit requires that write operations occur at a slower rate than that of the read strobe. In fact the write strobe period must be at least twice the read strobe period plus some internal delays. Table 1 gives the actual maximum writing rates, and shows that the rate must be reduced when the block of data which is read from the RAM is not completely composed of new data. The maximum writing rate is limited by the need to have read a complete block before the requested amount of new data has been loaded.

A Data Available Flag is provided which goes active when the pre-defined number of words have been written to the RAM. The data read sequence then automatically starts and the flag will go in-actice when the pre-programmed amount of data has been read. An additional get ready to Read Me Flag is provided which can separately be programmed to occur at any point during the block write operation. This flag has no internal action but can be used to warn the next system element that data is to be expected.

DEFINING THE LENGTH OF THE BLOCKS

The amount of new data written to the RAM before the Data Availble Flag is raised, and the amount of data which is then read from the RAM are separately definable. In this way the user can define the amount of old data which is re-read before the new data will be accessed. These overlapping data blocks are required in systems performing frequency domain transforms, when a window operator is applied to prevent frequency discontinuities between the blocks. The resulting loss of information, caused by de-emphasizing the data near the edges, is recovered by overlapping the blocks.

The mode control input MD0 is used to define the block length during the read operation. When MD0 is tied low the read block length will be 1024 words. When MD0 is tied high the block length is defined by the state of pins D4:0, which become inputs whilst the RESET input is active. A tri-state buffer is needed on the outputs which is only enabled during RESET, and whose inputs define the block length. These five inputs allow the block length to be defined in multiples of 32 words, from a minimum of 32 up to the maximum of 1024. The decode of the five bits (0 - 31) should be considered as defining additional blocks of 32 words above the 32 word minimum.

The mode control inputs MD2:1 are used to define the number of new words in the total block defined as above. Decodes 0 through 2 define 1024, 512, and 256 new words respectively. Decode 3 is used when a finer definition is needed, and makes use of the states of pins D9:5 during reset. The decodes of the five bits (0 - 31) then define additional groups of 32 words above a 32 word minimum.

USING THE FLAGS

The data available flag (DAV) always goes active when the required number of new words have been written to the buffer, and the first word to be read is available at the output pins. The rising edges of the read strobes must then be used by the system to transfer the complete block of data to the next system component. The minimum write periods given in Table 1 ensure that the first word will have been read before it is replaced with new data.

Internal logic will increment the read address counter and DAV will go in-active when the complete block has been read. The DAV output will also go in-active for one read strobe period every time a new word is written to the buffer. Write operations to the next system component should be inhibited for that cycle, and the DAV ouput must be used as write enable for the next device. All DAV transitions are produced by the rising edge of the read strobe.

An additional flag is provided which can be used to warn the next system component that data is to be expected. This get ready to read me flag (RMF) can be programmed to occur at any point (within 16 words) during the write operation. Decodes 0 through 2, from mode control inputs MD4:3, will cause the flag to go active after 1024, 512, or 256 words respectively have been loaded. Decode 3 allows the state of pins D15:10 during RESET to be used to define the transition point. Decodes 0 through 63 define form 0 to 63 additional groups of 16 words after the minimum 16 words have been loaded. The RMF flag goes in-active at the same time DAV goes in-active.

The gap between the RMF and DAV outputs should be sufficient to ensure that the next system component can immediately accept data once DAV goes active. The RMF flag has no internal action within the PDSP16540.

SUPPORTING THE PDSP16510

The PDSP16510 FFT Processor does not contain sufficient RAM to allow it to perform continuous 1024 point transforms without ignoring some of the incoming data. When the PDSP16540 is used as an input buffer, continuous transforms can be executed without any loss of information.

When block overlapping is not needed, or if the amount is restricted to either 50% or 75%, the mode control inputs can be directly used to define the operation of the PDSP16540. The D15:0 pins need not be used to define the block lengths.It should be noted, however, that the reset input is still needed to initialise the device, even though the state of the D15:0 pins is irelevent at that time. Figure 1 shows such a system.

Tying MD0 low defines the block length to be 1024 words, and tying MD2:1 appropriately high or low will produce the required decodes to provide 0%, 50%, or 75% overlaps. With 50% overlapping 512 new words are loaded, and with 75% overlapping 256 new words are needed. MD5 should be tied low unless real only transformsd are to be done (See the next section).

The DAV output is used to drive the INEN input on the PDSP16510 and the RMF flag is not used. The PDSDP16510 must be used in the mode in which INEN is an enabling signal, rather than its edge activated mode (Control Register Bit 12 must be set). The LFLG transition produced by the PDSP16510 is not used by the PDSP16540, since internal logic computes the starting address for the read operation.

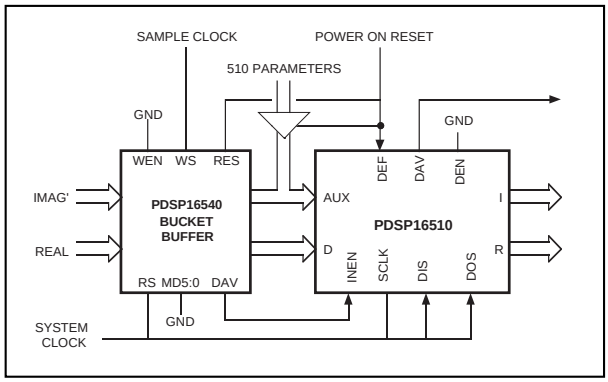


Figure 1. Typical 1024 Point FFT System

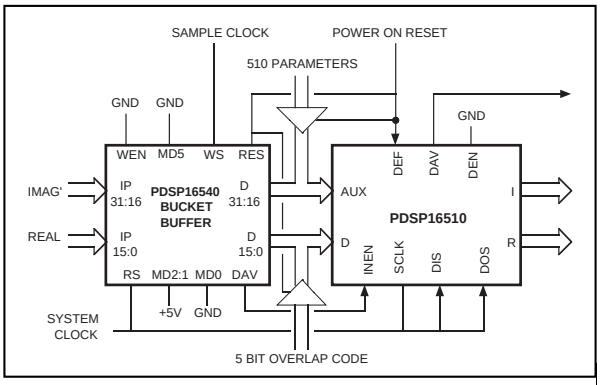


Figure 2. System with Non Standard Overlaps

Figure 2 shows a 1024 point system which allows the amount of overlap to be any value within 32 words. The 5 bit overlap code defines groups of 32 new words which are written to the buffer, in addition to the minimum number of 32 words. The smaller the number of new words written, the greater is the overlap with the previous block.

During reset the D31:0 outputs from the PDSP16540 will be high impedance and the 5 bit code is inputed on D9:5. This high impedance state also allows the PDSP16510 control parameters to be inputed on its AUX 15:0 bus without any conflicts.

The rate at which data is written to the PDSP16540 must be such that 1024 words can be transferred between the devices, transformed , and then moved to the output circuit for analysis before the DAV flag goes active again. Since the read operation is interrupted for one cycle every time a write operation occurs, the equation controlling the minimum writing period is given by;

$$NS > 1024B + \frac{1024BS}{S-B} + T + D$$

where N is the amount of new data written to the buffer, S is the period of the write strobe, B is the read strobe period, T is the transform time as given in the data sheet for the PDSP16510, and D is the time to transfer data from the PDSP16510 to the next system device.

It must be noted that the above minimum write period only applies if continuous inputs are to transformed without the loss of any incoming information. Peak writing rates can be much higher if gaps occur within the incoming data stream. The minimum periods given in Table 1 then limit the writing rate.

When the PDSP16510 uses a 40 MHz clock, dumps its transformed data with a 40MHz strobe, and the PDSP16540 uses a 40 MHz read strobe, then the minimum S period is149 ns. This equates to a 6.7 MHz writing rate when blocks are not overlapped, 3.35 MHz with 50% overlaps (512 new words), or 1.675MHz with 75% overlaps (256 new words).

Characteristic	Min	Max	Notes
RS Period,Tp	25ns		
RS Low Time	8ns		
RS High Time	8ns		
WS Period	2Tp+10ns		Both conditions must be satisfied
WS Period	$\frac{Tp \times L}{N}$		L = Block length, N = amount of new data written
WS Low Time	10ns		
WS High Time	10ns		
$\overline{WEN}$ set up wrt WS going high	2 ns		$\overline{WEN}$ going active or in-active
$\overline{WEN}$ Hold wrt WS going high	8 ns		
Data In Set Up wrt RS going high	8 ns		
Data In Hold Time wrt RS going high	0 ns		
Delay from RS going high to O/P Data		19ns	All output delays are with 30pf loads
$\overline{DAV}$,RMF transition wrt to RS going high	10ns	18ns	Going active or in-active
Time to go Low Z wrt to RS going high		19ns	Occurs when DAV also goes active
Time to go High Z wrt to RS going high		12ns	Occurs when DAV also goes in-active

Table 1. Timing Information

The amount of overlapping is dependent on the needs of a particular application, and is usually subject to some compromise. If the above maximum writing rates are marginally not adequate, the amount of overlap can possibly be reduced to achieve the required performance. Mode control inputs MD2:1 should then all be tied high, and outputs D9:5 used as inputs during reset to define the number of new words to be written.

SUPPORTING REAL ONLY TRANSFORMS

If MD5 is tied high the PDSP16540 will support the PDSP16510 when two concurrent 1024 point real transaforms are to be performed. It does not suppoprt block overlapping in this mode.

Real only data is written to the buffer using the IP15:0 inputs, and the IP31:16 inputs are redundant. Two blocks of data are acquired before DAV goes active, and both blocks are then read in parallel using all thirty two outputs.

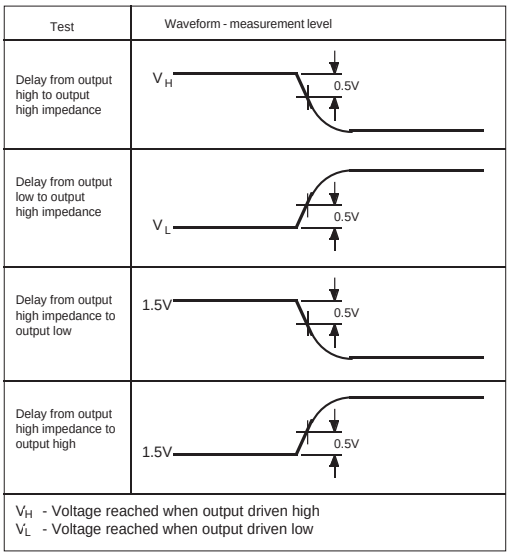
MD0,1, and 2 must be tied low in order to define blocks of 1024 words which totally consist of new data. The RMF flag is not needed by the PDSP16510, but will actually go active after the defined number of words in the second block have been loaded. Control Register Bits 8:6 in the PDSP16510 must be set to 101 in order to expect data on both its real and imaginary inputs.

ABSOLUTE MAXIMUM RATINGS [See Notes]

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	0°C to 70°C
Junction temperature	150°C
Package power dissipation	3000mW
Thermal resistances	
Junction to case $ø_{JC}$	5°C/W

NOTES ON MAXIMUM RATINGS

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as positive into the device.



STATIC ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise state)

Tamb = 0 C to +70°C.
Vcc = 5.0v ± 10%

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.8			V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	10		300	mA	V_{CC} = Max

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PDSP16540	C0	AC	Commercial	- PGA package
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