MAS9187

12 X 8-bit D to A Converter

- **3-pin Serial Data Interface**
- **Low Voltage Output Buffer**

DESCRIPTION

MAS9187 is 12-channel 8-bit DAC, designed primarily for trimmer replacement. Device is controlled by a simple 3-line input. The output buffers operate in the entire voltage range from ground to the positive power supply rail.

DAC is selected with four first bits in serial input data (SDI-pin) and the DAC output value is set according to the last 8 bits in serial input data.

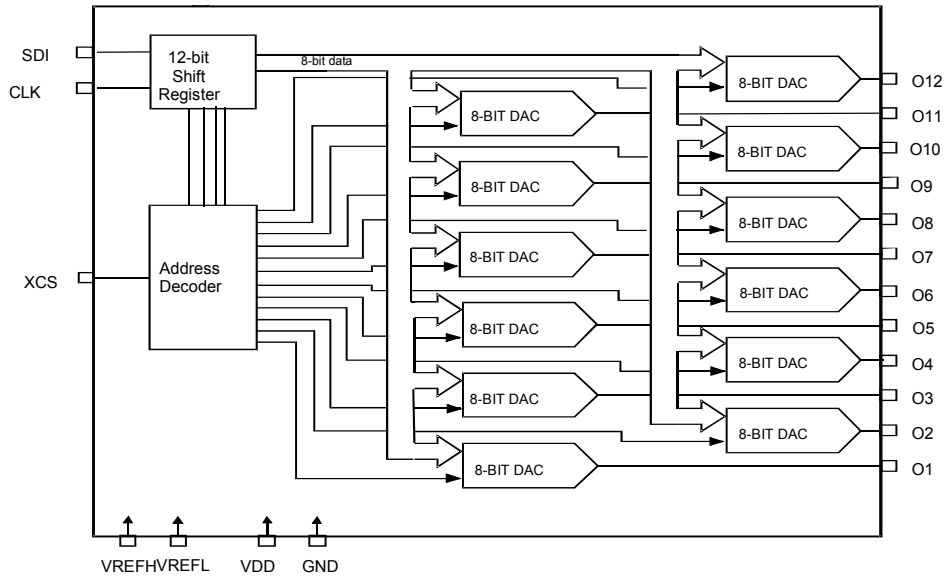
FEATURES

- Twelve 8-bit DACs on a single monolithic chip
- Voltage level output
- TSSOP 20 package
- Single, low +1.8 V supply
- Power-on reset

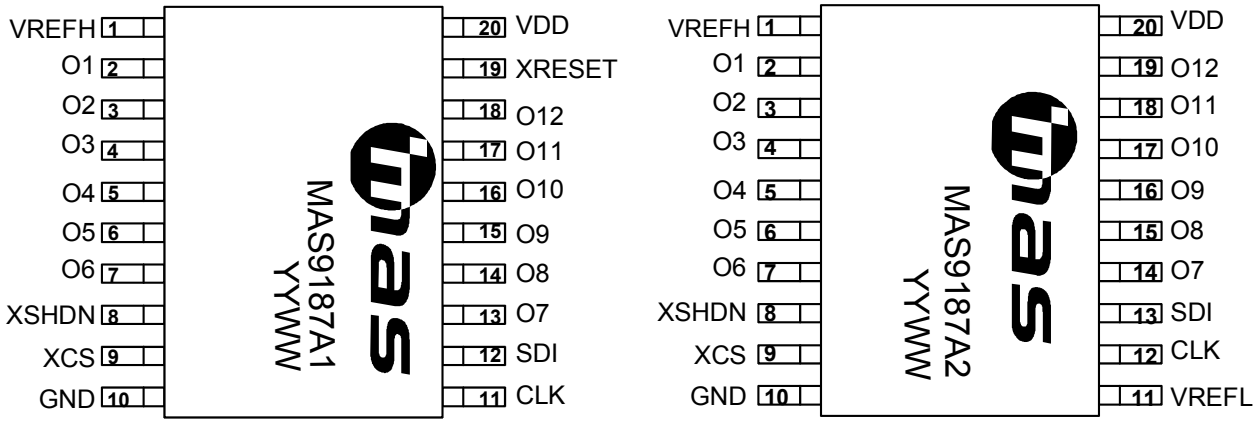
APPLICATIONS

- High resolution monitors
- Automatic gain control
- Trimmer replacement

BLOCK DIAGRAM



PIN CONFIGURATION



Top view
YYWW = year, week

PIN DESCRIPTION

Pin Number	MAS9187 A1	MAS9187 A2	Function
1	VREFH	VREFH	DAC output reference high voltage
2	O1	O1	DAC 1, address 0x0
3	O2	O2	DAC 2, address 0x1
4	O3	O3	DAC 3, address 0x2
5	O4	O4	DAC 4, address 0x3
6	O5	O5	DAC 5, address 0x4
7	O6	O6	DAC 6, address 0x5
8	XSHDN	XSHDN	Device analog part power-down signal (active low)
9	XCS	XCS	Device enable signal (rising edge loads data to DAC)
10	GND	GND	Device ground-pin
11	CLK	VREFL	Data clock / DAC output low reference voltage
12	SDI	CLK	Serial input data / Data clock
13	O7	SDI	DAC 7, address 0x6 / Serial input data
14	O8	O7	DAC 8, address 0x7 / DAC 7, address 0x6
15	O9	O8	DAC 9, address 0x8 / DAC 8, address 0x7
16	O10	O9	DAC 10, address 0x9 / DAC 9, address 0x8
17	O11	O10	DAC 11, address 0xA / DAC 10, address 0x9
18	O12	O11	DAC 12, address 0xB / DAC 11, address 0xA
19	XRESET	O12	Device Digital part reset – middle code preset pin/DAC 12, address 0xB
20	VDD	VDD	Device power supply pin

MAS9187 has two bonding options available:

- MAS9187A1, where VREFL pin is bonded to GND pin and XRESET pin can be used
- MAS9187A2, where XRESET pin is bonded to VDD pin and VREFL pin can be used

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply (VDD to GND)	VDD		-0.3	+6.0	V
Input Voltage Range (any other pin)			-0.3	VDD + 0.3	V
Continuous Power Dissipation				1000	mW
Storage Temperature Range			-65	+150	°C

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage Range	VDD		2.7	3.6	5.5	V	1)
Operating Temperature Range	Temp		-40		+85	°C	

Note 1: MAS9187Axx3 and MAS9187Axx4 minimum supply voltage 1.8 V

ELECTRICAL CHARACTERISTICS

(VDD = 3.0 V ± 10% or 5.0 V ± 10%, VREFH = VDD, VREFL = 0V, -40°C ≤ T_A ≤ +85°C unless otherwise noted)

DC Parameters

◆ **Digital Inputs**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC Resolution	N			8		Bits
DAC Differential Nonlinearity Error	DNL		-1		+1	LSB
DAC Integral Nonlinearity Error	INL		-1		+1	LSB
DAC Full-scale Error	GFSE		-1		+1	LSB
DAC Zero Code Error	BZSE		-1		+1	LSB
DAC Output Resistance	ROUT			30	60	Ω

◆ **Reference Input**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFH Voltage Range	VREFH	$V_{REFH} > V_{REFL}$	0		VDD	
REFL Voltage Range (MAS9187A2 only)	VREFL	$V_{REFH} > V_{REFL}$	0		VDD	
REFH Input Resistance	RREFH		5	10		kΩ
REFL Input Resistance	RREFL			10		kΩ

◆ **Digital Input**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Logic High	VIH		0.7*VDD			
Digital Logic Low	VIL				0.3*VDD	
Digital Input Current	IIL				± 1	uA

◆ **Power Supplies**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Power Supply Range	VDD		2.7		5.5	V	1)
Supply Current	IDD	VDD = 3.60V		3	6	mA	
Supply Current	IDD	VDD = 5.50V			20	mA	
Shutdown Current	ISHDN			0.5	5	uA	

Note 1: MAS9187Axx3 and MAS9187Axx4 minimum supply voltage 1.8 V

AC Parameters

◆ **AC Characteristics**

Dynamic Performance

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Sensitivity (100Hz)	PSRR			54		dB
Vout Settling time (±1/2 LSB error band)	TS			6		µs
Crosstalk between adjacent outputs	CT			63		dB

Switching Characteristics

(Minimum values at +25 °C, VDD = 3.60 V)

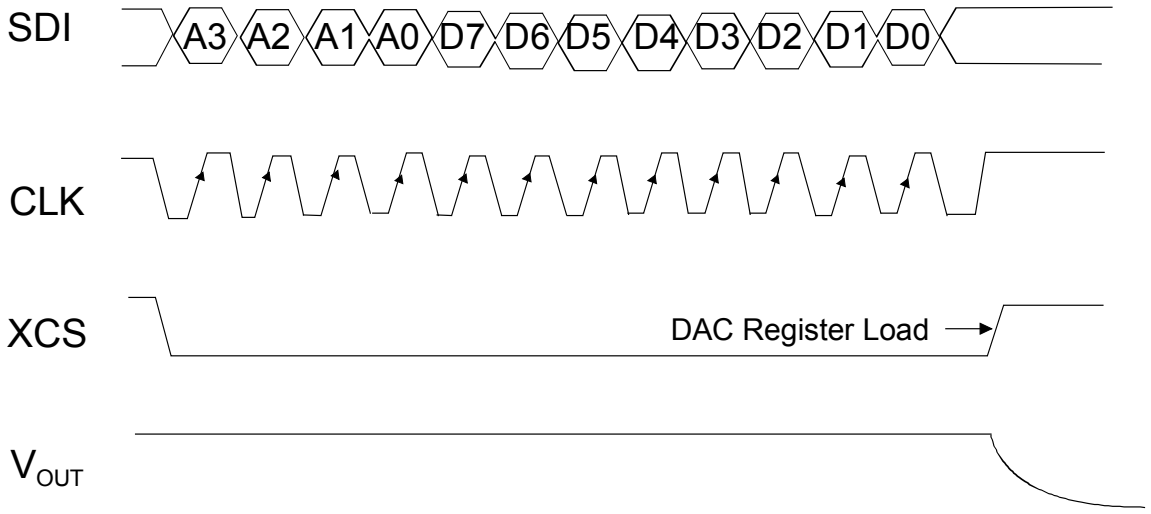
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Clock High Pulse Width	TCH			16		ns
Input Clock Low Pulse Width	TCL			7		ns
Data Setup Time	TDS			-5		ns
Data Hold Time	TDH			5		ns
XCS Fall to First Clock Pulse Fall	TCLCL			16		ns
XCS High Pulse Width	TCSW			22		ns
RESET Pulse Width	TRS			28		ns
CLK Rise to XCS Rise Hold Time	TCSH			22		ns
XCS Rise to CLOCK Rise Setup	TCS1			-5		ns

OPERATING MODES

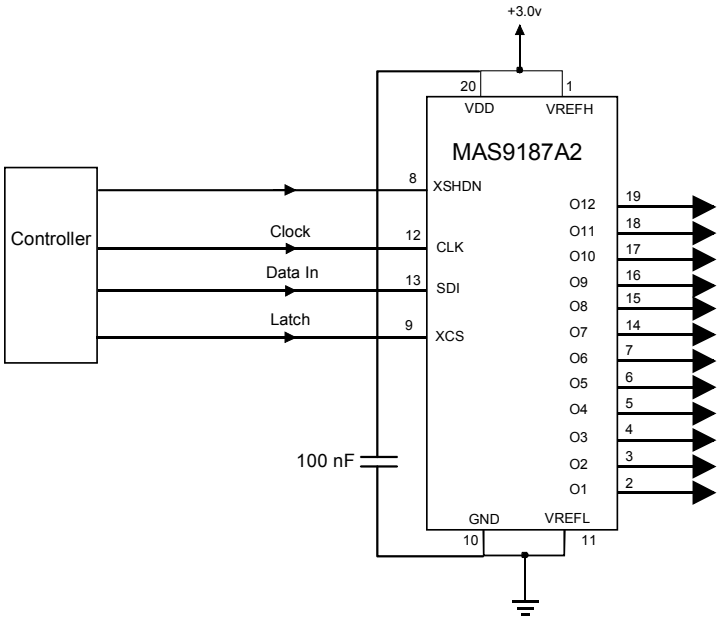
DAC maximum output voltage is set using VREFH and VREFL pins (= 255/256 * (VREFH-VREFL)+VREFL) (note: VREFL=GND in case of MAS9187A1). XRESET pin is used for middle code preset: DAC registers are reset and middle code will appear at the DAC output.

Serial input data is written to SDI while XCS is low. Data is read at CLK rising edge to on-chip shift register. Rising XCS-pin stops data reading and 12 CLK-cycles are used as the input data (4 address bits and 8 data bits). The last 12 bits before rising XCS are used as input data.

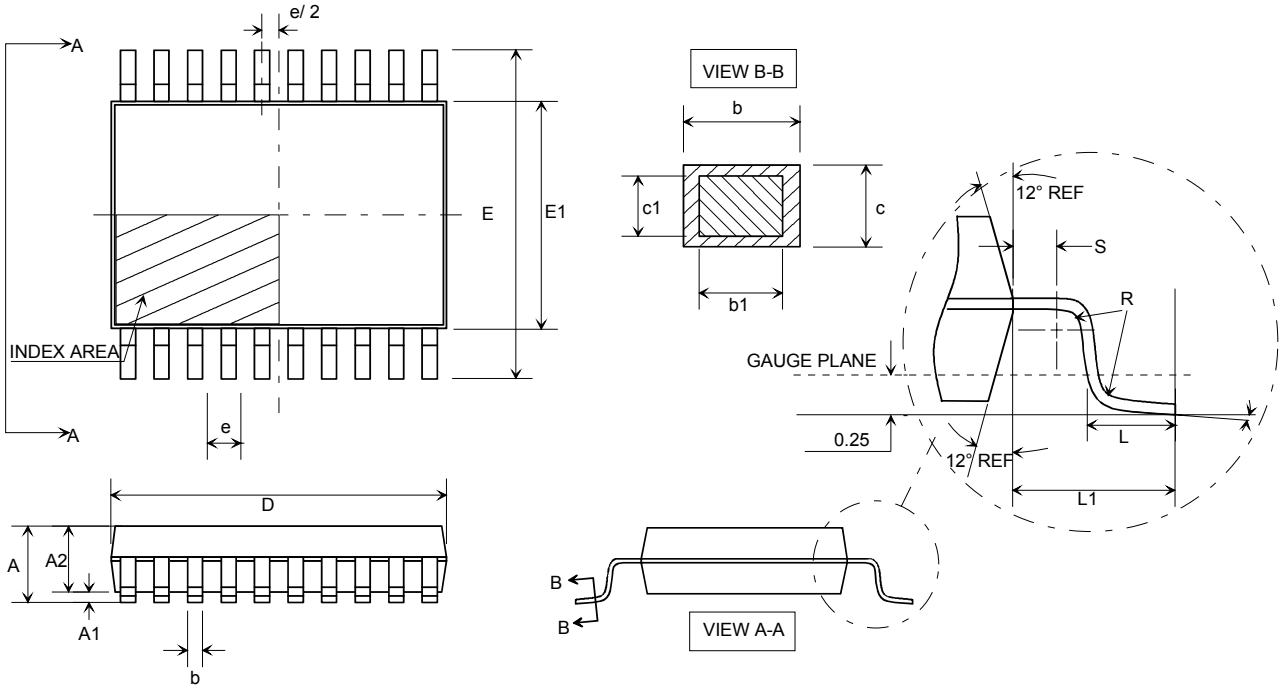
◆ **Timing diagram**



APPLICATION AND TEST CIRCUIT INFORMATION



PACKAGE (TSSOP-20) OUTLINES



Symbol	Min	Nom	Max	Unit
A	--	--	1.10	mm
A1	0.05	--	0.15	mm
A2	0.85	0.90	0.95	mm
b	0.19	--	0.30	mm
b1	0.19	0.22	0.25	mm
c	0.09	--	0.20	mm
c1	0.09	--	0.16	mm
D	6.40	6.50	6.60	mm
E		6.4 BSC		mm
E1	4.30	4.40	4.50	mm
e		0.65 BSC		mm
L	0.50	0.60	0.75	mm
L1		1.00 REF		
R	0.09	--	--	mm
S	--	0.20	--	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.
Reference Standard : JEDEC MO-153 .

SOLDERING INFORMATION

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 μm, material Sn 85% Pb 15%

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9187AUA1	12 x 8-bit D to A Converter	TSSOP-20	0 V Reference Level
MAS9187AUA2	12 x 8-bit D to A Converter	TSSOP-20	Scalable Reference Level
MAS9187AUA3	12 x 8-bit D to A Converter	TSSOP-20	0 V Reference Level, VDD min 1.8 V
MAS9187AUA4	12 x 8-bit D to A Converter	TSSOP-20	Scalable Reference Level, VDD min 1.8 V

LOCAL DISTRIBUTOR

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