MAS9178

AM Receiver IC

- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS9178 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary. Unlike MAS1016A and MAS1016B, MAS9178 does not require AGC control procedure in WWVB and JJY systems.

MAS9178A1 has differential input and internal 0.875 pF compensation capacitor for crystal shunt capacitance compensation.

MAS9178A5 requires external compensation capacitor for crystal shunt capacitance compensation. It can be used with crystals that do not match with fixed 0.875 pF compensation capacitance of MAS9178A1.

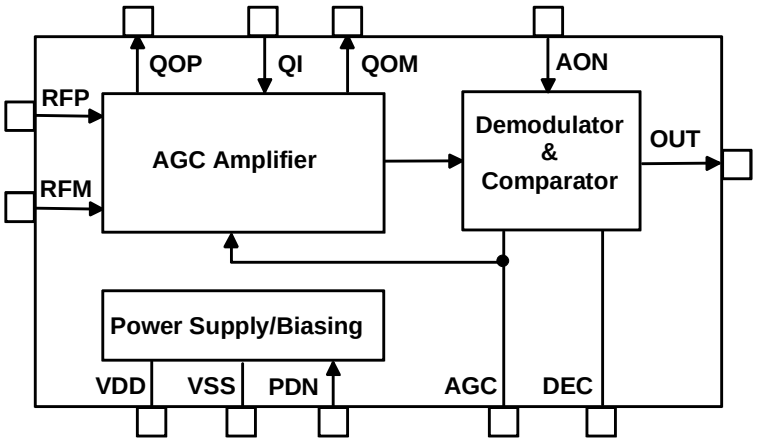
FEATURES

- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

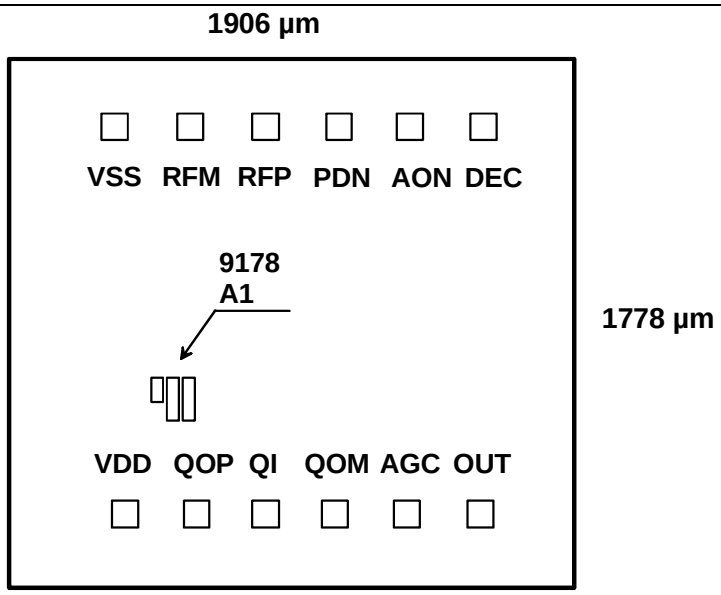
APPLICATIONS

- Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany) and MSF (UK)
- Receiver for ASK Modulated Data Signals

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 1.91 x 1.78 mm; PAD size = 100 x 100 µm except for VSS PAD size 104 x 112 µm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in the center of VDD pad

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	0 µm	0 µm	
Quartz Filter Output for Crystal	QOP	306 µm	19 µm	
Quartz Filter Input for Crystal and External Compensation Capacitor	QI	549 µm	19 µm	
Quartz Filter Output for External Compensation Capacitor	QOM	866 µm	19 µm	
AGC Capacitor	AGC	1146 µm	19 µm	
Receiver Output	OUT	1389 µm	19 µm	1
Demodulator Capacitor	DEC	1389 µm	1428 µm	
AGC On Control	AON	1146 µm	1428 µm	2
Power Down Input	PDN	829 µm	1428 µm	3
Positive Receiver Input	RFP	586 µm	1428 µm	
Negative Receiver Input	RFM	269 µm	1428 µm	
Power Supply Ground	VSS	16 µm	1407 µm	

Notes:
1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
3) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	5.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-20	70	^{o}C
Storage Temperature	T_{ST}		-40	120	^{o}C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		3.60	V
Current Consumption	I_{DD}	VDD=3.6 V, Vin=0 µV VDD=1.4 V, Vin=0 µV	56	76 66	95	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 0.8 V_{DD}		0.2 V_{DD}	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up Without Fast Start-up		12 3		s min
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION

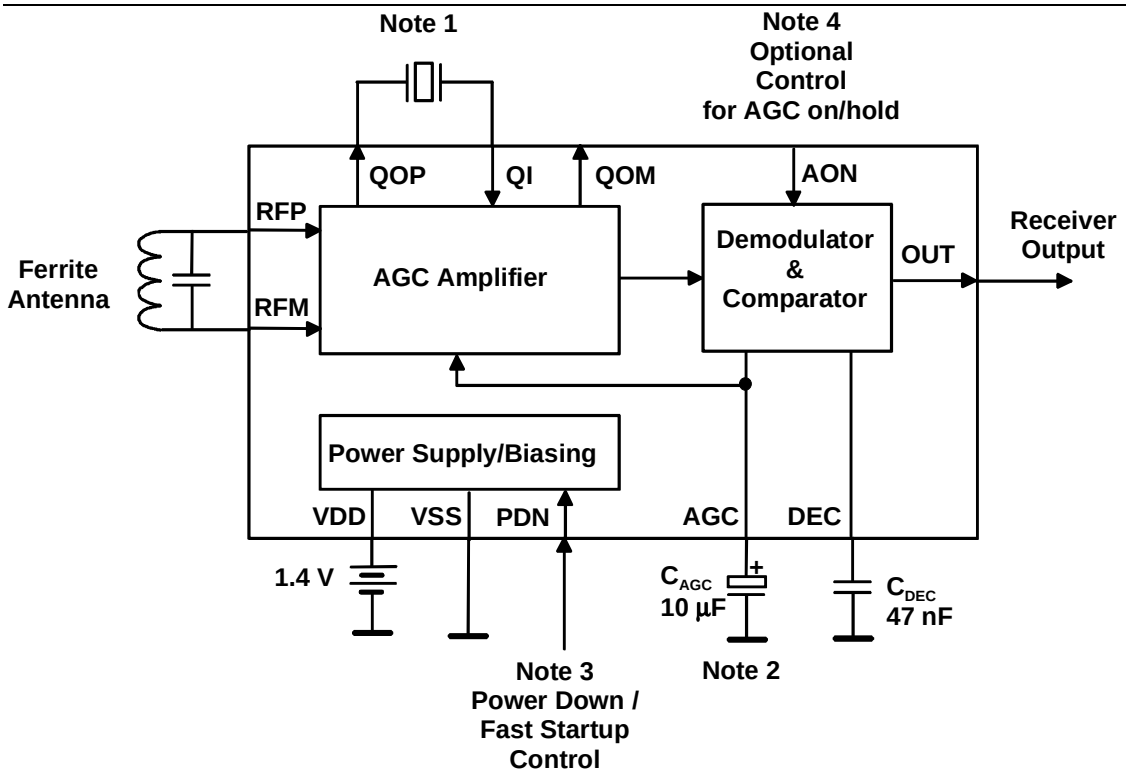


Figure 1 Application circuit of internal compensation capacitance version MAS9178A1.

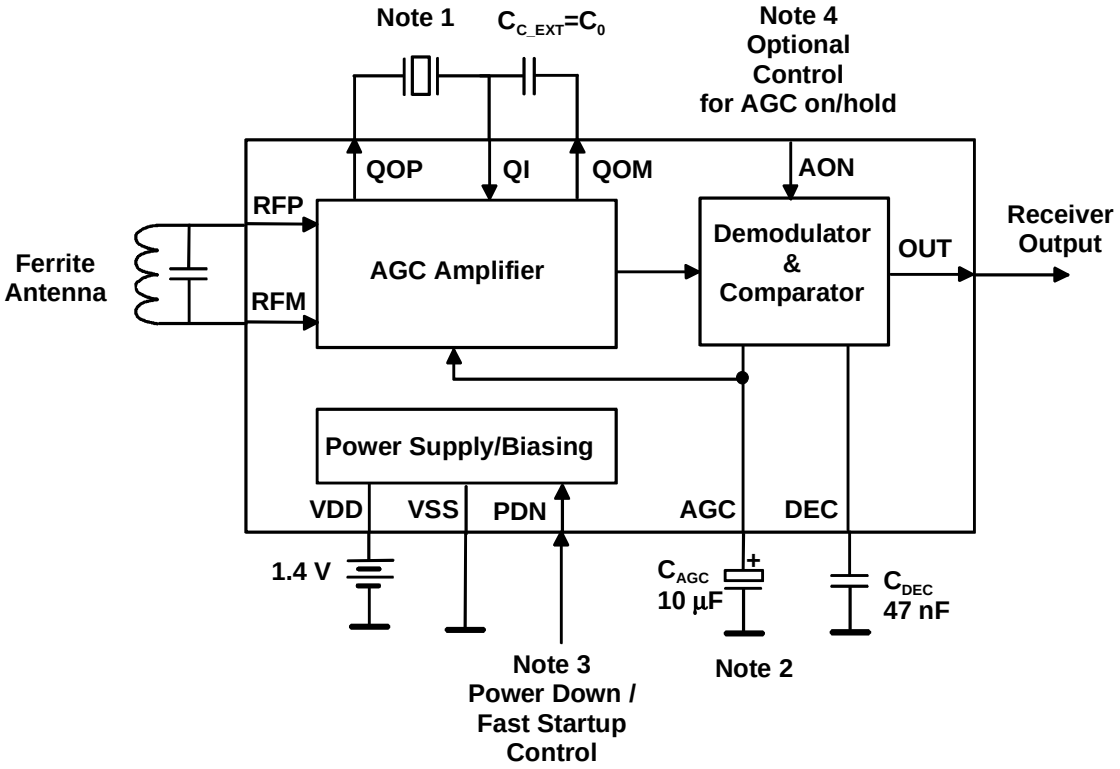


Figure 2 Application circuit of external compensation capacitance version MAS9178A5.

TYPICAL APPLICATION (Continued)

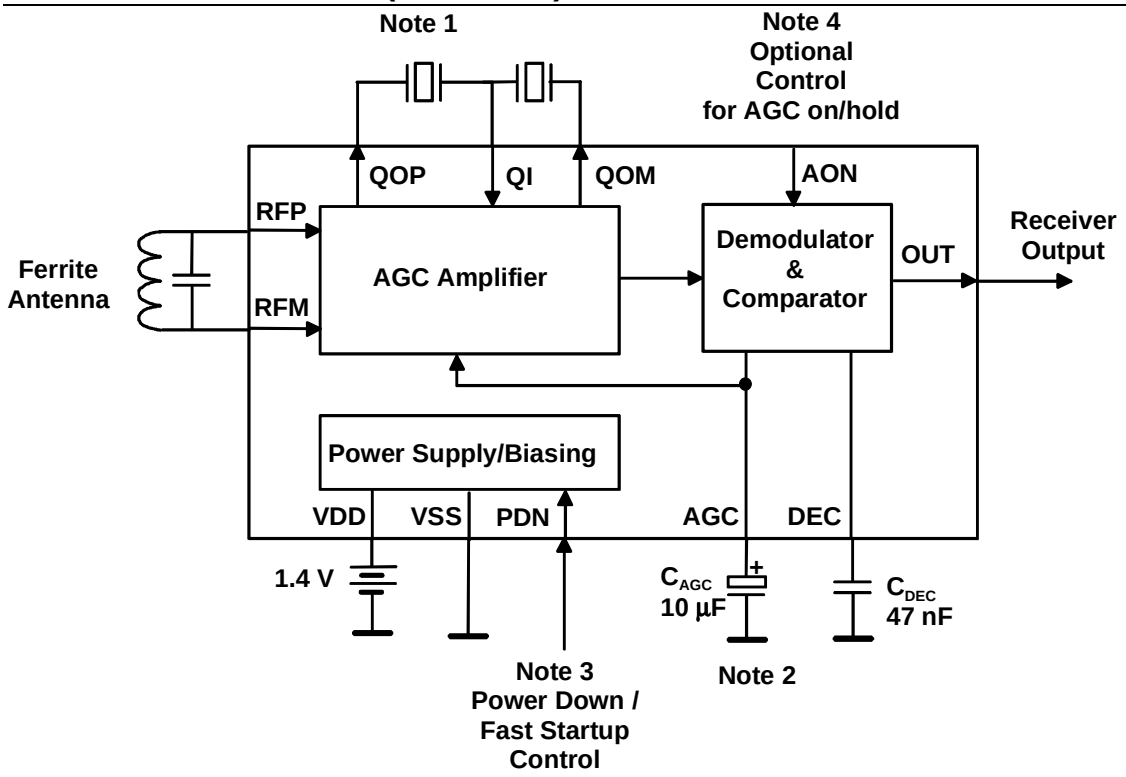


Figure 3 Dual band application circuit of external compensation capacitance version MAS9178A5.

Note 1: Crystal

The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitor C_C=0.875 pF of MAS9178A1. External compensation pad QOM is unconnected in MAS9178A1. MAS9178A5 does not have internal compensation capacitance C_C and it requires use of external compensation capacitor C_{C_EXT}. It must be connected between pins QOM and QI (see figure 2). C_{C_EXT} should have equal value with crystal's effective shunt capacitance C_0. External compensation version MAS9178A5 should be used when fixed 0.875 pF compensation capacitance of MAS9178A1 does not match well with used crystal's shunt capacitance.

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

In dual band receiver the crystals can be connected in parallel thus external compensation capacitor value C_{C_EXT} must be sum of two crystals' shunt capacitances. In dual band receiver it is also possible to connect other crystal from QOP pin and the other crystal from QOM pin to common QI pin (figure 3). In this circuit configuration no external compensation capacitor is required since the crystals compensate each other.

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz

Table 1 Time-Signal System Frequencies

Note 2: AGC Capacitor

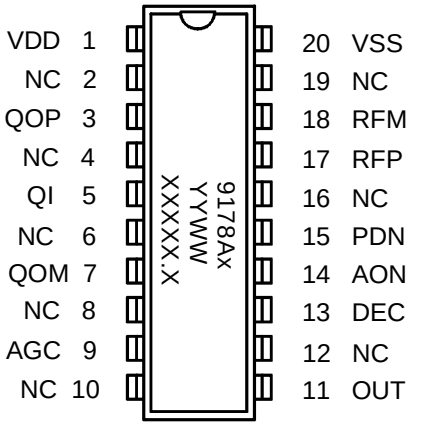
The AGC and DEC capacitors must have low leakage currents due to very small 40 nA signal currents through the capacitors. The insulation resistance of these capacitors should be higher than 70 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. Electrolyte capacitors cannot be used due to their large leakage current. Instead low leakage tantalum capacitor can be used as AGC capacitor. DEC capacitor can be low leakage chip capacitor.

TYPICAL APPLICATION (Continued)

Note 3: Power Down / Fast Startup Control
Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered by the falling edge of PDN signal, i.e., controlling device from power down to power up. The startup time without using the fast startup control can be several minutes but with fast startup it is shortened typically to 12 s.

Note 4: Optional Control for AGC On/Hold
AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive etc. can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven.

SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
x =1, 5 Sample Version Number

PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
NC	2			
QOP	3	AO	Quartz Filter Output for Crystal	
NC	4			1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
NC	6			1
QOM	7	AO	Quartz Filter Output for External Compensation Capacitor	
NC	8			
AGC	9	AO	AGC Capacitor	
NC	10			
OUT	11	DO	Receiver Output	2
NC	12			
DEC	13	AO	Demodulator Capacitor	
AON	14	DI	AGC On Control	3
PDN	15	AI	Power Down Input	4
NC	16			
RFP	17	AI	Positive Receiver Input	
RFM	18	AI	Negative Receiver Input	
NC	19			
VSS	20	G	Power Supply Ground	

Notes:

1) Pins 4 and 6 around quartz crystal filter input pins must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.

SAMPLE INFORMATION

Product Code	Product	Description	Capacitance Option
MAS9178A1TB00.01	AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 480 µm.	C_C = 0.875 pF
MAS9178A5TB00.01	AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 480 µm.	External Compensation Capacitor
MAS9178A1TC00.01	AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.875 pF
MAS9178A5TC00.01	AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	External Compensation Capacitor

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