

LM1229

I²C Compatible CMOS TV RGB and Deflection Processor

General Description

The LM1229 pre-amp is an integrated CMOS CRT RGB preamp plus horizontal and vertical deflection processing with an I²C compatible interface for controlling all the parameters necessary to directly adjust the gain, contrast and brightness and geometry of the CRT display.

In the RGB section, the CRT bias is controlled by the three DAC outputs which are matched to the LM248x integrated bias clamp ICs. The brightness control operates on the video channels rather than the bias channels and is designed to maintain the CRT color temperature through the full range of adjustment. The On Screen Display inputs accept either digital or analog input levels. Black level clamping of the video signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional clamp capacitors. Blanking inputs are provided which can accept both horizontal and vertical flyback inputs for composite blanking of the video. A vertical blanking output pulse is provided which can drive a G1 blanking amplifier such as the one in National's LM2485 clamp IC. The LM1229 RGB outputs are compatible with National's high gain drivers (<http://www.national.com>).

The Deflection section uses a 12.0 MHz resonator and with it the horizontal processor is capable of locking to seven different television signal formats, 15.734, 28.1, 31.468, 33.7, 37.9, 45.0, and 48.08 kHz by configuring two external tri-state pins. The resonator frequency can be scaled up or down by as much as 5% to accommodate custom scan frequencies, however all scan modes will be scaled up or down by the same percentage. Additional inputs are provided for H and V synchronization, X-Ray protection, V scan protection, and H and V EHT compensation. Deflection output signals are provided for horizontal drive, variable amplitude vertical ramp, vertical ramp reference voltage, variable amplitude dynamic focus, and E-W correction with DC level adjustment for size.

A status register is also provided for the system microcontroller to read and check for failure conditions.

The IC is packaged in an industry standard 64 lead LQFP molded plastic package.

Features

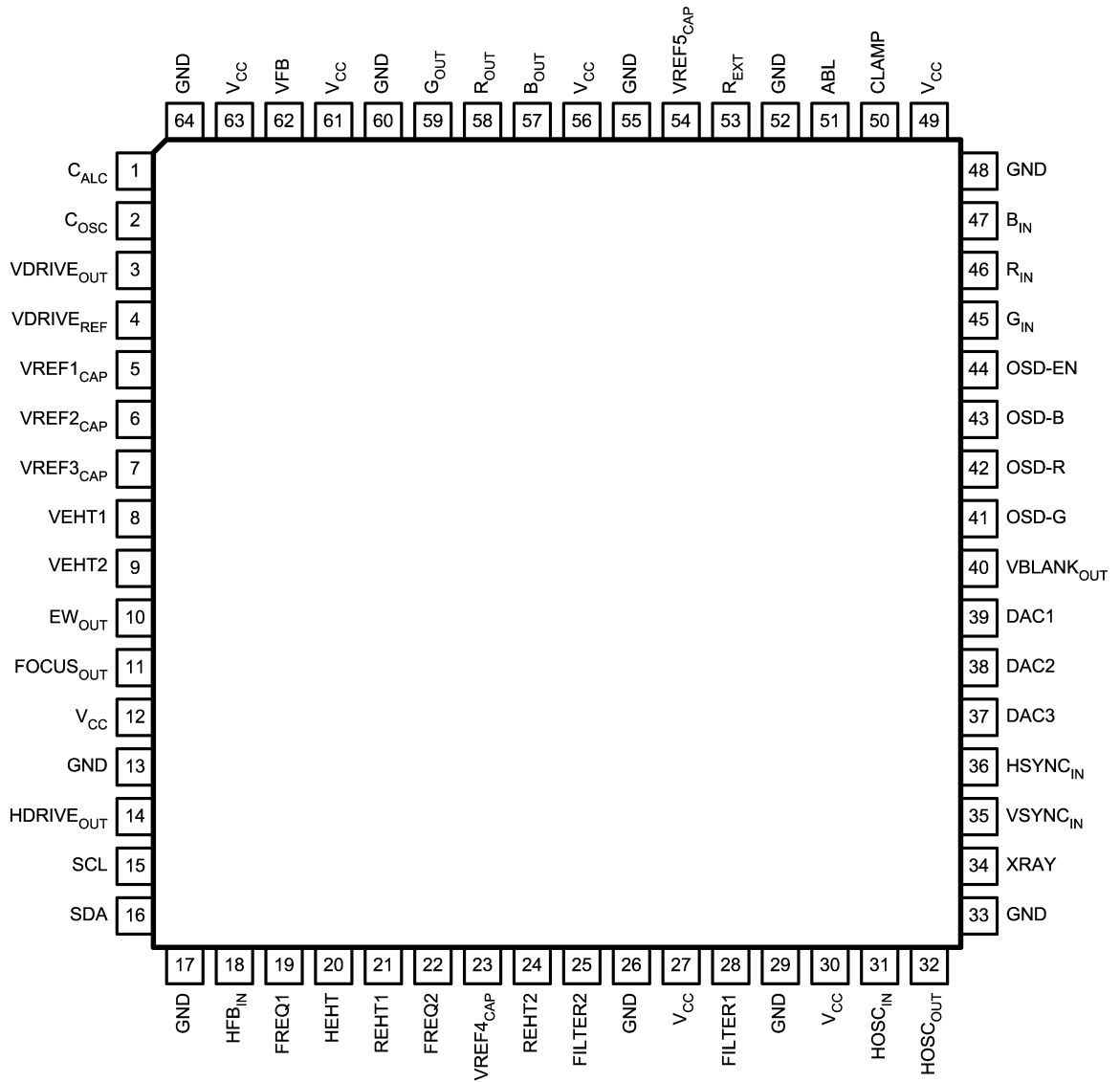
- Fully bus controllable via an I²C compatible interface.
- Contrast control for simultaneously adjusting the RGB output peak to peak levels.
- Gain controls for aligning the CRT color temperature.

- Color tracking brightness control for maintaining color temperature throughout the full range of adjustment.
- Black level clamping to ensure output level stability. The polarity of the logic pulse input is register selectable.
- Digital or analog RGB OSD inputs, with adjustable transparency available in the digital mode and clamping in the analog mode for black level stability.
- Choice of four levels of OSD amplitude.
- Window highlight using the OSD Transparency feature.
- ABL input for reducing the video contrast when the CRT beam current exceeds the predetermined threshold set by an external resistor.
- Horizontal and/or vertical blanking directly from deflection signals. The blanking can be disabled, if desired.
- Matched to National's driver and clamp IC families (<http://www.national.com>).
- Black level output adjustable from 0.5V to 1.4V for compatibility with NSC CRT driver IC's with or without PNP transistor buffers.
- Three DAC outputs for setting CRT cathode bias, which can be set to full or half scale like the LM1267 series of preamplifiers.
- Spot killer which blanks the video outputs when V_{CC} falls below the specified threshold.
- RGB Power Saving Mode with 35% power reduction.
- Support for seven different TV signal formats.
- RGB blanking for scan loss protection.
- I²C control over horizontal and vertical position and size, pincushion, pin balance, trapezoidal, parallelogram, top and bottom corner corrections, vertical S and C correction, and dynamic focus amplitude.
- Programmable duration 5V vertical blanking output pulse.
- Uses a low cost resonator.
- Status register indicating vertical scan loss, X-Ray, horizontal flyback and horizontal lock status.
- Blanks the RGB outputs whenever the loss of vertical scan is detected.
- Independent control over horizontal and vertical sync input polarities.

Applications

- Television deflection and RGB video processing with National's CRT drivers.

LM1229 Package and Pinout



20118701

Non-Exposed DAP — Order Number LM1229VEC
 Non-Exposed DAP — NS Package Number VEC64A
 Exposed DAP — Order Number LM1229YA
 Exposed DAP — NS Package Number VXE64A

FIGURE 1.

Absolute Maximum Ratings (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC} , Pins 12, 27, 30, 49, 56, 61, 63	6.0V
Peak Video DC Output Source Current (Any One Amp) Pins 57, 58 or 59	1.0 mA
Voltage at Any Input Pin (V_{IN}) $V_{CC} - 0.5V \leq V_{IN} \leq V_{CC} + 0.5V$	
Video Inputs (pk-pk) $0V \leq V_{IN} \leq 1.2V$	
Power Dissipation (P_D) (Above 25°C Derate Based on θ_{JA} and T_J)	1.8W
Thermal Resistance LM1229VEC (θ_{JA})	35 °C/W

Thermal Resistance LM1229YA (θ_{JA}) DAP not soldered	41 °C/W
Thermal Resistance LM1229YA (θ_{JA}) DAP soldered	27 °C/W
Junction Temperature (T_J)	150°C
ESD Susceptibility (Note 4)	3.5 kV
ESD Machine Model (Note 13)	350V
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C

Operating Ratings (Note 3)

Temperature Range	0°C to +70°C
Supply Voltage V_{CC}	4.75V $\leq V_{CC} \leq$ 5.25V
Video Inputs (peak-peak)	0V $\leq V_{IN} \leq$ 1.0V

Video Signal Electrical Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{IN} = 0.70 V_{P-P}$, $V_{ABL} = V_{CC}$, $C_L = 10 \text{ pF}$, Video Outputs = 2.4 V_{P-P} . See (Note 7) for Min and Max parameters and (Note 6) for Typical.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply current	No output loading. See (Note 8).		260	330	mA
I_{S-PS}	Supply current, power save mode.	No output loading. See (Note 8).		100	125	mA
$V_{OB \text{ TYP}}$	Active video black level output.	No input signal, DC offset = 0x3.		1.25		V
$V_{OB \text{ MIN}}$	Active video minimum black level output.	No input signal, DC offset = 0xF(min).		0.5		V
$V_{OB \text{ MAX}}$	Active video maximum black level output.	No input signal, DC offset = 0x0(max).		1.45		V
$V_{OB \text{ STEP}}$	Active video black level step size.	No input signal. Varying DC offset.		65		mV
$V_{OB \text{ MIN BRITE}}$	Active video minimum black level output.	No input signal, DC offset = 0x3, gain = 0x7F, brightness = 0xFF(min).		0.8		V
$V_{OB \text{ MAX BRITE}}$	Active video maximum black level output.	No input signal, DC offset = 0x3, gain = 0x7F, brightness = 0x00(max).		1.65		V
$V_{OBB \text{ STEP}}$	Active video brightness step size.	No input signal, DC offset = 0x3, varying brightness.		6.3		mV
$V_{O \text{ MAX}}$	Maximum video output.	Video in = 0.70 V_{P-P} , contrast = 0x7F, brightness = 0x0, DC offset = 0x3		4.75		V
LE	Linearity error.	Staircase input signal. See (Note 9).		5		%
t_R	Video rise time.	(Note 5), 10% to 90%, AC input signal.		8		ns
OS_R	Rising edge overshoot.	(Note 5), AC input signal.		2		%
t_F	Video fall time.	(Note 5), 90% to 10%, AC input signal.		8		ns
OS_F	Falling edge overshoot.	(Note 5), AC input signal.		2		%
BW	Channel bandwidth (-3 dB)	(Note 5), AC input signal.		70		MHz
$SEP_{10 \text{ kHz}}$	Video amplifier 10 kHz isolation.	(Note 14).		70		dB
$SEP_{10 \text{ MHz}}$	Video amplifier 10 MHz isolation.	(Note 14).		50		dB
$A_V \text{ MAX}$	Maximum voltage gain.	Video in = 0.70 V_{P-P} , Maximum contrast and gain, $V_{ABL} = 5.0\text{V}$.		4.35		V/V
$A_V 50\% \text{ CONT}$	Contrast attenuation @ 50%.	Maximum gain, $V_{ABL} = 5.0\text{V}$.		-5.15		dB
$A_V \text{ MIN}/$ $A_V \text{ MAX}$	Maximum contrast attenuation.	Maximum gain, $V_{ABL} = 5.0\text{V}$.		-20.5		dB
$A_V 50\% \text{ GAIN}$	Gain attenuation @ 50%.	Maximum contrast, $V_{ABL} = 5.0\text{V}$.		-4.15		dB

Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{IN} = 0.70 V_{P-P}$, $V_{ABL} = V_{CC}$, $C_L = 10 \text{ pF}$, Video Outputs = $2.4 V_{P-P}$. See (Note 7) for Min and Max parameters and (Note 6) for Typical.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$A_{V \text{ MIN GAIN}} / A_{V \text{ MAX GAIN}}$	Maximum gain attenuation.	Maximum contrast, $V_{ABL} = 5.0\text{V}$.		-12		dB
$A_{V \text{ MATCH}}$	Maximum gain match between channels.	Maximum contrast, $V_{ABL} = 5.0\text{V}$.		± 0.6		dB
$A_{V \text{ TRACK}}$	Gain tracking channel to channel.	AC input signal. See (Note 11).		± 0.6		dB
$V_{ABL \text{ HIGH}}$	ABL control range upper limit.	(Note 12), AC input signal.		4.5		V
$V_{ABL \text{ LOW}}$	ABL control range lower limit.	(Note 12), AC input signal.		2.5		V
$A_{V \text{ 2.5}} / A_{V \text{ MAX}}$	ABL Gain Reduction at $V_{ABL} = 2.5\text{V}$.	(Note 12), AC input signal.		-5.8		dB
$I_{ABL \text{ ACTIVE}}$	ABL input bias current during ABL.	(Note 12), AC input signal. $V_{ABL} = 2.5\text{V}$			10	μA
$I_{ABL \text{ MAX}}$	ABL input current sink capability.	(Note 12), AC input signal.		1.0		mA
$A_{V \text{ ABL TRACK}}$	ABL channel to channel gain tracking error.	Input signal = $0.7 V_{P-P}$, ABL voltage set to 4.5V and 3.0V.		0	7.5	%
R_{IP}	Minimum input resistance (pins 45, 46, 47)			20		M Ω

OSD Electrical Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$. See (Note 7) for Min and Max parameters and (Note 6) for Typical.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL MODE						
V_{LOW}	Maximum low input voltage, (OSD and Enable).	Enable: video inputs selected OSD: OSD black displayed			1.0	V
V_{HIGH}	Minimum high input voltage, (OSD and Enable).	Enable: OSD inputs selected OSD: OSD colors displayed	3.0			V
V_{OSD-11}	OSD output amplitude.	OSD Enable = 1, OSD Contrast = 11.		2.65		V
V_{OSD-10}	OSD output amplitude.	OSD Enable = 1, OSD Contrast = 10.		2.35		V
V_{OSD-01}	OSD output amplitude.	OSD Enable = 1, OSD Contrast = 01.		2.15		V
V_{OSD-00}	OSD output amplitude.	OSD Enable = 1, OSD Contrast = 00.		1.75		V
$V_{OSD-AUX}$	OSD output amplitude (AUX).	OSD Enable = 1, OSD[5] = 1		3.0		V
$\Delta V_{OSD \text{ BLACK}}$	Difference between OSD and video black levels.	Same channel, contrast and gain = 0x60	-85		100	mV
$\Delta V_{OSD \text{ WHITE}}$	Output Match between channels.	OSD Contrast = 11, maximum difference between R, G and B		3		%
$V_{OSD \text{ TRACK}}$	Output Variation between channels.	OSD contrast varied from max to min		3		%
HT_{MAX}	OSD background video maximum level.	OSD[3] = 1, OSD TRANS = 0x7F. See (Note 18).		100		%
HT_{MIN}	OSD background video minimum level.	OSD[3] = 1, OSD TRANS = 0x00. See (Note 18).		10		%
ANALOG MODE						
$A_{V \text{ ANALOG OSD}}$	Analog gain from pins 41, 42, 43 to the video outputs, with input level $0.7 V_{PP}$.	OSD Enable = 1, Gains at maximum.		3.75		V/V

OSD Electrical Characteristics (Continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$. See (Note 7) for Min and Max parameters and (Note 6) for Typical.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BOTH MODES						
I_{LOW}	Low input current (OSD and Enable).	$V_{\text{IN}} = 0\text{V}$		-3.0		μA
I_{HIGH}	High input current (OSD and Enable).	$V_{\text{IN}} = 5\text{V}$.001		μA
SEP _{10 kHz}	Crosstalk from video @ 10 kHz.	See (Note 17).		-70		dB
SEP _{10 MHz}	Crosstalk from video @ 10 MHz.	See (Note 17).		-50		dB

DAC Output Electrical Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{\text{IN}} = 0.7\text{V}$, $V_{\text{ABL}} = V_{CC}$, $C_L = 10\text{ pF}$, Video Outputs = $2.4 V_{\text{P-P}}$. See (Note 7) for Min and Max parameters and (Note 6) for Typical. DAC parameters apply to all 3 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{\text{DAC MIN}}$	Minimum DAC output voltage	Register Value = 0x00		0.5		V
$V_{\text{DAC MAX MODE 0}}$	Maximum DAC output voltage (full scale)	Register Value = 0xFF, GLOBAL[5] = 0.		4.2		V
$V_{\text{DAC MAX MODE 1}}$	Maximum DAC output voltage (half scale)	Register Value = 0xFF, GLOBAL[5] = 1.		2.1		V
$\Delta V_{\text{DAC TEMP}}$	DAC output voltage variation with temperature	$0^\circ\text{C} < T < 70^\circ\text{C}$ ambient		0.5		mV/ $^\circ\text{C}$
$\Delta V_{\text{DAC VCC}}$	DAC output voltage variation with V_{CC}	$4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$, DAC register set to mid-range (0x7F)		50		mV
Linearity	Linearity of DAC over its range			5		%
Monotonicity	Monotonicity of the DAC excluding dead zones		-0.5		+0.5	LSB
I_{MAX}	Maximum DAC output load current				1.0	mA

Deflection Signal Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{\text{IN}} = 0.7\text{V}$, $V_{\text{ABL}} = V_{CC}$, $C_L = 10\text{ pF}$, See (Note 7) for Min and Max parameters and (Note 6) for Typical.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{XTL}	Ceramic resonator input frequency			12		MHz
V_{HFB}	Switching threshold for detecting horizontal flyback on pin 18.			2.4		V
t_{FW}	Flyback Width		1			μs
$V_{\text{VFB-DC}}$	DC bias point of VFB input			1.25		V
$V_{\text{VFB-SW}}$	Switching threshold for detection			1.75		V
$V_{\text{X-RAY}}$	X-Ray Threshold Voltage	Above $V_{\text{X-RAY}}$ the HDRIVE output is disabled (high)		2.5	3.2	V
$V_{\text{CCforXRAYRESET}}$	X-Ray Reset	V_{CC} required to reset X-Ray		4		V
Δf_{FR}	Free-run frequency tolerance	(ceramic resonator tolerance)			± 1	%
f_{CR}	PLL capture range			± 6		%
t_{HDPHASE}	Horizontal phase control range	All scan frequencies		± 25		% T_H
t_{PARCOR}	Maximum parallelogram correction	Measured at 31 kHz		± 1		μs
t_{BOWCOR}	Maximum pin balance (bow) correction	Measured at 31 kHz		± 0.5		μs
$H_{\text{EHT-}}$	HEHT phase shift left ($R_{\text{EHT}} = 20\text{k}$)	HEHT[3:0] = 0011b and $V_{20} = 1.5\text{V}$		-2.7		% T_H
$H_{\text{EHT+}}$	HEHT phase shift right ($R_{\text{EHT}} = 20\text{k}$)	HEHT[3:0] = 0111b and $V_{20} = 3.5\text{V}$		2.8		% T_H
V_{HDOL}	HDRIVE Max low level output	$I_{\text{OL}} = 10\text{ mA}$		0.7		V

Deflection Signal Characteristics (Continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{IN} = 0.7\text{V}$, $V_{ABL} = V_{CC}$, $C_L = 10\text{ pF}$, See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{HDO}	HDRIVE Max sink current				10	mA
V_{HDOH}	HDRIVE Max high level output voltage			5		V
δ	HDRIVE Duty cycle	During normal use		50		%
t_{ON}	Delay to 50% duty cycle			60		lines
t_{JITTER}	Jitter (Note 19)	Measured at 31 kHz scan frequency		1.8		ns
$f_{V_{MIN}}$	Minimum vertical lock frequency				50	Hz
$f_{V_{MAX}}$	Maximum vertical lock frequency		120			Hz
f_{VFR}	Vertical free run frequency			30		Hz
$V_{MAXRAMPOUT}$	Maximum ramp amplitude	$VSIZE[7:0] = 0xFF$	1.7	2.2		V
$V_{MINRAMPOUT}$	Minimum ramp amplitude	$VSIZE[7:0] = 0x00$		1.4	1.9	V
$V_{RAMPDCOUT}$	Vertical ramp DC reference voltage			2.5		V
$\Delta V_{RAMP}/\Delta V_{EHT1}$	Ramp amplitude reduction with V_{EHT1}	$VEHT[3:0]$ varied from 0x0 to 0xF	0		-4.4	%/V
$R_{IN-VEHT1}$	Pin 8 input resistance		1			M Ω
$\Delta V_{EW}/\Delta V_{EHT2}$	Change in EW output level with V_{EHT2}	$VEHT[7:4]$ varied from 0x0 to 0xF	0		348	mV/V
$R_{IN-VEHT2}$	Pin 9 input resistance			50		k Ω
k_S	S correction range		0		10	%
k_C	C correction range		-11		11	%
V_{DF}	Dynamic Focus Amplitude	$DYN_FOCUS[6:0] = 0x7F$		1.1		V
V_{EW}	Maximum E-W amplitude peak-peak	$PIN[6:0] = 0x7F$		1.2		V
I_{EW}	E-W output current		-3		3	mA
$V_{EWDCMIN}$	EW output DC at middle of parabola	$HSIZE[6:0] = 0x00$		1.4		V
$V_{EWDCMAX}$	EW output DC at middle of parabola	$HSIZE[6:0] = 0x7F$		2.5		V
V_{EWTRAP}	Trapezoid correction parabola tilt	Beginning and end of parabola shift oppositely and equally. $PIN[6:0] = 0x00$, $T_CORNER[6:0]$, $B_CORNER[6:0] = 0x3F$.		± 0.375		V
$V_{EWCORNER}$	Corner correction shift at end points	Top & bottom adjusted independently. $PIN [6:0] = 0x00$, $TRAP[6:0] = 0x3F$.		± 0.375		V
V_{EWPIN}	Pin correction amplitude	$TRAP[6:0]$, $T_CORNER[6:0]$, $B_CORNER[6:0] = 0x3F$.	0		1.8	V

System Interface Signal Characteristics

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{IN} = 0.7\text{V}$, $V_{ABL} = V_{CC}$, $C_L = 10\text{ pF}$, Video Outputs = 2.4 V_{P-P} . See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SPOT}	Spot Killer Voltage	(Note 16), V_{CC} Adjusted to Activate		4.0		V
V_{REF}	V_{REF} output voltage (pin 2)			1.2		V
V_{IL}	Logic low input voltage (SCL, SDA, HSYNC, VSYNC)		-0.5		1.5	V
V_{IH}	Logic high input voltage (SCL, SDA, HSYNC, VSYNC)		3.0		$V_{CC} + 0.5$	V

System Interface Signal Characteristics (Continued)

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $V_{IN} = 0.7\text{V}$, $V_{ABL} = V_{CC}$, $C_L = 10\text{ pF}$, Video Outputs = $2.4 V_{P-P}$. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_L	Logic low input current (SCL, SDA, HSYNC, VSYNC)	SDA or SCL, Input Voltage = 0V		±10		µA
I_H	Logic high input current (SCL, SDA, HSYNC, VSYNC)	SDA or SCL, Input Voltage = 5.0V		±10		µA
V_{OL}	Logic low output voltage (SCL, SDA)	$I_O = 3\text{ mA}$		0.5		V
$I_{FB\ THRESHOLD}$	I_{IN} blank detection threshold (pin 24)			-20		µA
$I_{FB\ IN\ MAX}$	Flyback input	Absolute maximum current during flyback			5	mA
$I_{FB\ IN\ MAX}$	Peak flyback input current	Design value - AC coupled		1.0		mA
$I_{FB\ OUT\ MAX}$	Flyback input current	Absolute maximum during scan	-500			µA
$t_{H-BLANK\ ON}$	Blanking time delay - on	+ Zero crossing of I_{FB} to 50% of output blanking start. $I_{FB} = +1.5\text{ mA}$		50		ns
$t_{H-BLANK\ OFF}$	Blanking time delay - off	- Zero crossing of I_{FB} to 50% of output blanking end. $I_{FB} = -100\ \mu\text{A}$		50		ns
$V_{BLANK\ MAX}$	Maximum video blanking level	CONTRAST[6:0], RGAIN[6:0], GGAIN[6:0], BGAIN[6:0] = 0x7F, BRIGHTNESS[7:0] = 0x00, OFFSET[3:0] = 0xC, AC input signal.	0		0.25	V
$t_{PW\ CLAMP}$	Minimum clamp pulse width	See (Note 15)	200			ns
$V_{CLAMP\ MAX}$	Maximum low level clamp voltage	To guarantee low state			1.0	V
$V_{CLAMP\ MIN}$	Minimum high level clamp voltage	To guarantee high state	3.0			V
$I_{CLAMP\ LOW}$	Clamp gate low input current	$V_{23} = 0\text{V}$		-0.4		µA
$I_{CLAMP\ HIGH}$	Clamp gate high input current	$V_{23} = 5.0\text{V}$		0.4		µA
$t_{CLAMP-VIDEO}$	Minimum wait from end of clamp pulse to start of video.	Referenced to RGB video inputs.	50			ns
$V_{HEHT-LOW}$	Low limit of pin 20 HEHT input			1.4		V
$V_{HEHT-HIGH}$	High limit of pin 20 HEHT input			3.4		V
$V_{VEHT1-LOW}$, $V_{VEHT2-LOW}$	Low limit of pins 8 and 9 VEHT inputs			1		V
$V_{VEHT1-HIGH}$, $V_{VEHT2-HIGH}$	High limit of pins 8 and 9 VEHT inputs			4		V

Note 1: Limits of Absolute Maximum Ratings indicate below which damage to the device will not occur.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Input from signal generator: $t_r, t_f < 1\text{ ns}$.

Note 6: Typical specifications are specified at $+25^\circ\text{C}$ and represent the most likely parametric norm.

Note 7: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 8: The supply current specified is the quiescent current for $V_{CC} = 5\text{V}$ and with $R_L = \infty$. Load resistors are not required and are not used in the test circuit, therefore all the supply current is used by the pre-amp.

Note 9: Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a $0.7 V_{P-P}$ level at the input. All 16 steps equal, with each at least 100 ns in duration.

Note 10: $dt/dV_{CC} = 200 \cdot (t_{5.5V} - t_{4.5V}) / ((t_{5.5V} + t_{4.5V})) \% / \text{V}$, where: $t_{5.5V}$ is the rise or fall time at $V_{CC} = 5.5\text{V}$, and $t_{4.5V}$ is the rise or fall time at $V_{CC} = 4.5\text{V}$.

Note 11: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to $A_V 50\%$ and measured relative to the $A_V MAX$ condition. For example, at $A_V MAX$ the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to $A_V 50\%$. This yields a typical gain change of 10.0 dB with a tracking change of $\pm 0.2\text{ dB}$.

Note 12: The ABL input provides smooth decrease in gain over the operational range of 0 dB to -5 dB: $\Delta A_{ABL} = A_V MAX - A_V (V_{ABL} = V_{ABL\ MIN\ GAIN})$. Beyond -5 dB the gain characteristics, linearity and pulse response may depart from normal values.

Note 13: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Note 14: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at $f_{IN} = 10$ MHz for V_{SEP} 10 MHz.

Note 15: A minimum pulse width of 200 ns is the guaranteed minimum for a horizontal line of 15 kHz. This limit is guaranteed by design. If a lower line rate is used then a longer clamp pulse may be required.

Note 16: Once the spot killer has been activated, the LM1229 remains in the off state until V_{CC} is cycled (reduced below 0.5V and then restored to 5V).

Note 17: Video input = $0.7 V_{p-p}$ and the OSD Enable is active with the OSD inputs at black. For each video input, in turn, set the specified video input at the designated frequency and measure the video feedthrough at the video outputs.

Note 18: In the transparency mode, the OSD background consists of video with contrast level determined by the Transparency Register. The OSD foreground is unaffected.

Note 19: Jitter is measured at the 31 kHz scan rate by measuring the time difference between the leading edge of HSYNC and the leading edge of the HDRIVE output pulse.

LM1229 Test Circuit

The LM1229 RGB test circuit is shown in *Figure 2*. The video generator should be a clean 75Ω source to prevent unwanted reflections from the terminations. The output waveforms should be measured with a 10X, low capacitance probe on an oscilloscope with at least 400 MHz bandwidth. The jumpers JP1 and JP2 determine the free running frequency according to *Table 1*. The OSD inputs are shown as

analog 0.7V peak to peak. If higher level signals are available, suitable attenuation and termination should be used to achieve the proper input level. To prevent overdriving the input pins, the 1000 pF capacitors should be removed (shorted) to test the digital OSD mode. Caution—Do not apply TTL OSD input signals to the LM1229 while it is in the analog OSD mode.

LM1229 Test Circuit (Continued)

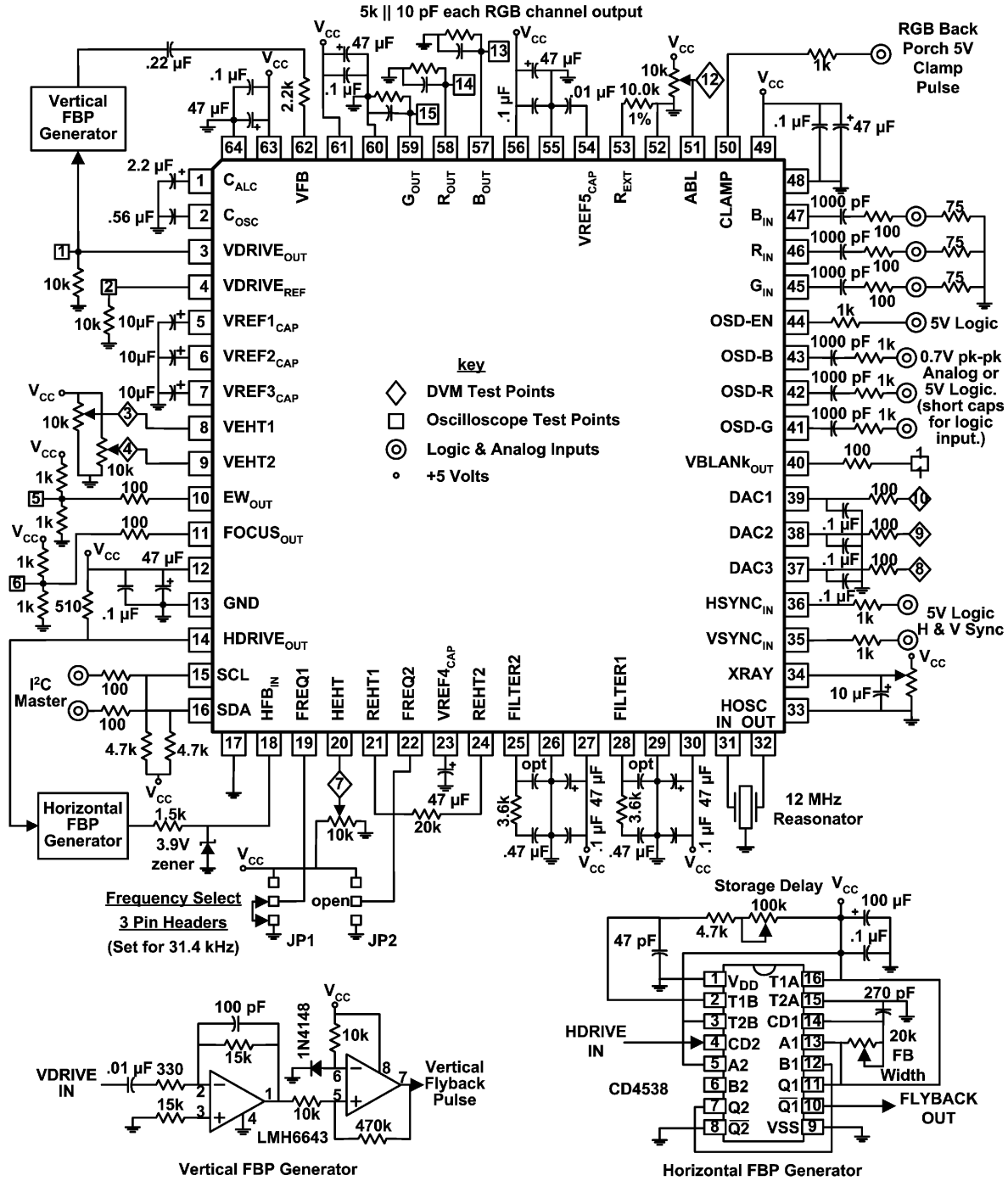


FIGURE 2. LM1229 Test Circuit

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Application Information

PIN CONNECTIONS

Pin No.	Pin Name	Schematic	Description
1 2	C_{ALC} C_{OSC}		<p>C_{ALC} is the feedback loop filter which maintains constant vertical ramp amplitude according to the value set in the vertical height register.</p> <p>C_{OSC} is the capacitor which determines the slope of the vertical ramp.</p>
3 4	$VDRIVE_{OUT}$ $VDRIVE_{REF}$		<p>These two outputs provide the inputs to a vertical output amplifier which drives the vertical yoke winding. Since the $VDRIVE_{OUT}$ amplitude is from 1.5V to 2.5V peak to peak, the gain of the output amplifier must be set with external resistors to match the vertical yoke being used. The $VDRIVE_{OUT}$ slope is positive (increasing voltage with time).</p>
5 6 7 23 54	V_{REF} Caps	<p>Pin Value 5,6,7: 10 μF 23: 47 μF 54: .01 μF</p> <p>* ESD Protection</p>	<p>Provides filtering for the internal voltages which set the internal bias currents in conjunction with R_{EXT}. For proper filtering, pins 5, 6 and 7 should be 10 μF, pin 23 should be 54 μF and pin 54 should be .01 μF. These capacitors should be placed as close to their pins as possible.</p>
8	VEHT1		<p>This input pin is used to control the height of the vertical ramp based on changes in the high voltage. A 1V negative change at pin 8 causes a maximum of 5% reduction in the ramp amplitude when the $VEHT[3:0]$ is set to 0xF. If this pin is not used, bit 3 of the SYNCPOL register should be set to 1. The values shown give a 350 mV change at pin 8 from a 2.5V change at the ABL pin.</p>
9	VEHT2		<p>This input pin is used to control the level of the E-W parabola based on changes in the high voltage. A 1V negative change at pin 9 causes a maximum of 300 mV increase in the ramp DC level when the $VEHT[7:4]$ is set to 0xF. If this pin is unused, bit 4 of the SYNCPOL register should be set to 1. The values shown give a 350 mV change at pin 9 from a 2.5V change at the ABL pin.</p>

Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
10	EW _{OUT}		EW _{OUT} is the output used for control of width, pincushion, trapezoid and top and bottom corners. Its lowest voltage is in the middle of vertical scan. The amplitudes of these functions are register controlled.
11	FOCUS _{OUT}		FOCUS _{OUT} is used for dynamic focus adjustment. The peak to peak amplitude is register controlled and if it is used for both horizontal and vertical dynamic focus, their amplitudes will be controlled proportionately.
	V _{CC} & GND		Power supply and ground pin for all the LM1229. Note the recommended charge storage and high frequency capacitors which should be as close to pins wherever possible.
14	HDRIVE _{OUT}		This is the horizontal drive output. When this output is low, the horizontal output transistor is on and a positive edge at pin 14 starts the flyback pulse. The duty cycle slowly increases to 50% when power is applied. The output sink current should not exceed 10 mA.
15	SCL		The I ² C compatible clock line. A pull-up resistor of about 4.7 kΩ should be connected between this pin and V _{CC} . A resistor of at least 100Ω should be connected in series with the clock line for additional ESD protection.
16	SDA		The I ² C compatible data line. A pull-up resistor of about 4.7 kΩ should be connected between this pin and V _{CC} . A resistor of at least 100Ω should be connected in series with the data line for additional ESD protection.

Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
18	Horizontal Flyback	<p>* ESD Protection</p>	<p>The input is a threshold detector at approximately 2.4V. R_H should be large enough to limit the combined peak current during flyback to a few milliamperes in the zener diode in accordance with the zener power rating. It may be desirable to add a resistor from V_{CC} or GND to pin 18 to offset the switching point up or down by a small amount. Be sure to start with small offsets and work up from there.</p>
19 22	FREQ1 FREQ2	<p>* ESD Protection</p>	<p>These two pins select the frequency of the horizontal PLL. They are tri-state and may be hard wired for a single frequency design or driven by a microcontroller for a multiple frequency design. The 100Ω resistor is used for ESD and arcing protection when the connections comes from a long distance away and are recommended even if the pins are hard wired. The input logic states and their corresponding scan frequencies are given in <i>Table 1</i>.</p>
20	HEHT		<p>This pin provides horizontal phase compensation, if needed, for beam current loading. The polarity and magnitude are selectable from the I²C bus. See <i>Table 4</i>, which shows the compensation for $R_{EHT} = 20k$. If this correction is not needed then it can be disabled by setting HEHT[3] to 1 and pin 20 can be left open.</p>
21 24	REHT1 REHT2	<p>* ESD Protection</p>	<p>The R_{EHT} resistor determines the gain of the horizontal phase compensation, HEHT. A smaller resistor increases the compensation and a larger resistor decreases it. If this feature is not used, pins 21 and 24 may be left open.</p>
25	FILTER2		<p>These are the currently recommended filter values for PLL 2. These components should be kept as close to pins 25 and 26 as possible, and high frequency signals should be routed away from this filter to avoid affecting the loop.</p>
28	FILTER1		<p>These are the currently recommended filter values for PLL 1. These components should be kept as close to pins 28 and 29 as possible, and high frequency signals should be routed away from this filter to avoid affecting the loop.</p>

Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
31 32	HOSC2 HOSC1		The oscillator can be a standard 12 MHz ceramic or crystal oscillator. Two suitable manufacturer's part numbers are Murata CST12.0MT and Panasonic PX1200MC-ND.
34	XRAY		This pin provides X-ray sense and shutdown. The input is a rectified horizontal flyback pulse. R_B is adjusted to cause shutdown at the desired amplitude of the flyback pulse. This provides X-ray protection by turning off the horizontal drive. After the shutdown, the LM1229 will be reset when V_{CC} drops below 4V or when the HDRIVE output is disabled and reenabled with bit 5 of the HEHT register. This shutdown function can be disabled by setting bit 6 of the HEHT register to a 1.
35 36	HSYNC VSYNC		These are the horizontal and vertical sync inputs to the LM1229. The horizontal sync is required by the horizontal PLL and the horizontal blanking function. The vertical sync is required by the vertical blanking function which includes the programmable vertical blanking output pulse and the RGB vertical blanking. These are both 5V logic levels with thresholds as given in the specifications section. Care must be taken to prevent sync overshoots from reaching the LM1229.
37 38 39	DAC 3 Output DAC 2 Output DAC 1 Output		These are the DAC outputs for the RGB cathode cut-off adjustments. The DAC output levels are set through the I ² C compatible bus. These can be set for 4.2V or 2.1V full scale to match the various NSC bias ICs. NSC's CRT arcing tests and experience shows that the best output termination for the DAC outputs is a 0.1 µF capacitor to ground at the IC terminals and a series 1k resistor close to the load.
40	VBLANK _{OUT}		This is a positive going logic pulse which can be used for vertical blanking on G1. It can be an input to the LM2485 where it is amplified to either 20V or 40V negative going peak to peak, depending on an option pin. The pulse starts when an input is received on the Vertical Flyback Input on pin 62 and lasts for the number of scan lines loaded in the VBLANK register, 0x51[7:0].

Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
41 42 43	Green OSD Red OSD Blue OSD (Digital Mode)	<p style="text-align: center;">* ESD Protection</p>	These inputs can be used for either analog or digital inputs. In the digital mode these inputs accept either TTL or CMOS input levels. Each color is either fully on (logic high) or fully off (logic low). Unused pins should be connected to ground with a 47k resistor. National Semiconductor does not recommend mixing analog and digital inputs in the same application.
41 42 43	Green OSD Red OSD Blue OSD (Analog Mode)	<p style="text-align: center;">* ESD Protection</p>	In the analog OSD mode, the inputs should be AC coupled through a 1000 pF capacitor, and the gain is about 3.5, so that a peak to peak input of 0.7V results in a 2.45V peak to peak signal at the RGB outputs when the OSD contrast is maximum. Signal input amplitudes larger than 0.7V are not recommended. The external ESD diodes are recommended if the input OSD video is generated some distance away from the LM1229. The 75Ω termination may not be needed if the signal amplitude is already 0.7V.
44	OSD Enable	<p style="text-align: center;">* ESD Protection</p>	This input accepts either TTL or CMOS input levels. When this input is a "0", only video is displayed. When it is a "1", the OSD from pins 1, 2 and 3 is displayed. If bit 3 of the OSD register (0x0B) is a "1" then the background of the OSD (when the Enable is a "1" and the OSD inputs are "0") will be video attenuated by the OSD_TRANS register (0x0A). If this input is unused, connect it to ground through a 47k resistor.
45 46 47	Green Video In Red Video In Blue Video In	<p style="text-align: center;">* ESD Protection</p>	These video inputs must be AC coupled with a 1000 pF cap. Internal DC restoration is done at these inputs. A series resistor of at least 33Ω and external ESD protection diodes should also be used for protection from ESD damage.
50	Clamp	<p style="text-align: center;">* ESD Protection</p>	This pin accepts either TTL or CMOS logic levels. The internal switching threshold is about one-half of V_{CC} . An external series resistor R_S between 1k and 3.9k is recommended to attenuate the peak to peak signal at pin 50. The resistor must be large enough to prevent the voltage at pin 50 from going higher than V_{CC} or below GND. The capacitor C_F should be used to eliminate noise on the clamp pulse which could cause false triggering during video.

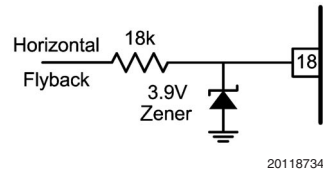
Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
51	ABL	<p>* ESD Protection</p>	<p>The Automatic Beam Limiter input is biased to the desired beam current limit by R_{ABL} and V_{BB} and normally keeps D_{INT} and the 1N4148 forward biased. When the current resupplying the CRT capacitance (averaged by C_{ABL}) exceeds this limit, then D_{INT} and the 1N4148 begin to turn off and the voltage at pin 51 begins to drop. The LM1229 then lowers the gain of the three video channels until the beam current reaches an equilibrium value. The 1N4148 is needed to prevent overcurrent in D_{INT} in cases where the ABL limit is greater than 1 mA.</p>
53	V_{REF} R_{EXT}	<p>* ESD Protection</p>	<p>External current set resistor, 10k 1%, sets the internal bias current level for optimum performance of the LM1229. This resistor should be placed as close to pin 53 and the pin 52 ground return as possible.</p>
57 58 59	Blue Output Red Output Green Output	<p>* ESD Protection</p>	<p>These are the three video output pins. They are intended to drive the National family of cathode drivers. Nominally, about 2.8V peak to peak will produce 140V peak to peak of cathode drive with the LM2426.</p>
62	Vertical Flyback	<p>* ESD Protection</p>	<p>This input is used to start the VBLANK output pulse which is used internally for vertical blanking of the RGB outputs. It is also used for the V Protect function which blanks the RGB video outputs if the vertical deflection fails. The values of C_V and R_V should be chosen to eliminate the long vertical rate slope at pin 62 and also ensure that this pin is not forced above V_{CC} or below GND. The bias level at this pin is about 25% of V_{CC} and the actual switching threshold is about 35% of V_{CC}.</p>

Application Information (Continued)

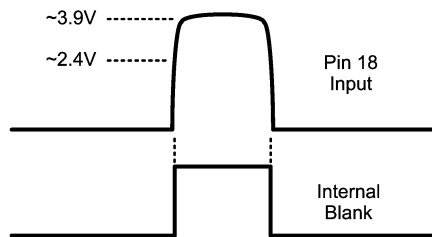
BLANKING

The pin 18 horizontal flyback input switches at about 2.4V based on an internal reference. A large amplitude input pulse is more desirable since it reduces the rise time at pin 18. The component values shown in *Figure 3* have been selected for a horizontal flyback amplitude of 40V peak to peak. This gives about 2 milliamps peak in the 3.9V zener diode. The internal blanking pulse is shown in *Figure 4* with its relationship to the external input.



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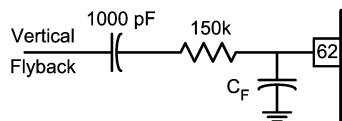
FIGURE 3. Horizontal Flyback



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FIGURE 4. Internal Blank Timing

The pin 62 vertical flyback input requires an AC coupled waveform. The time constant should be chosen to make a highpass filter to eliminate the slope of the vertical flyback waveform during vertical scan. The values in *Figure 5* are for a vertical flyback amplitude of 45V peak to peak. C_F may be needed to prevent horizontal rate noise from causing multiple triggering of the vertical blanking pulse. It can be as large as 1000 pF. Care must also be taken to ensure the voltage at pin 62 does not go below ground or above V_{CC} .



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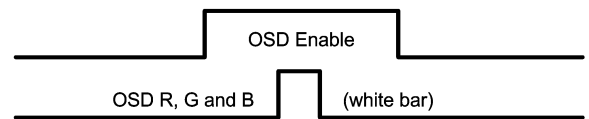
FIGURE 5. Vertical Flyback

CLAMP PULSE

In order for the video processing to operate correctly, there must be a clamping pulse present on pin 50. The polarity of this pulse can be selected with bit 3 of the GLOBAL register. Only about 1V peak to peak is needed to operate the clamp and it is often desirable to have a 3.3k to 3.9k series resistor to attenuate the signal to prevent it from coupling into other signal lines.

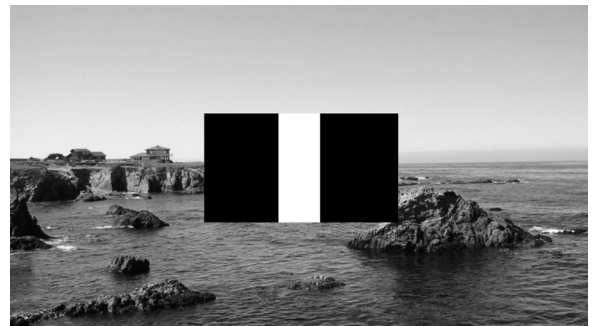
DIGITAL OSD OPERATION

The LM1229 is configured for digital OSD operation by setting the DA bit, 0x0B[4], to 0. This is also the power on default. The On Screen Display must be provided from an external source. The contrast of the OSD can be controlled with the OSD_Cont bits, OSD[1:0]. The OSD Enable input causes the LM1229 output to switch from video to OSD. Depending on the TRANS bit, 0x0B[3], the OSD background will be either black or video with contrast setting determined by the OSD TRANS register, 0x0A[6:0]. *Figure 6* shows one possible OSD timing where the Enable is longer than the OSD white block itself. In *Figure 7* the transparency bit is 0, resulting in a black background while the OSD Enable is active. In *Figure 8* the transparency bit is 1, resulting in a background of video whose contrast is determined by the OSD TRANS register. Care should be taken in setting the OSD TRANS register since it is independent of the CONTRAST register and therefore it is possible to make the OSD background contrast higher than that of the surrounding video. In normal use as seen in *Figure 8*, the OSD TRANS register is set to a lower value than the CONTRAST register. See *Table 2* for the OSD as a function of the TRANS bit of the OSD register and the OSD Enable input.



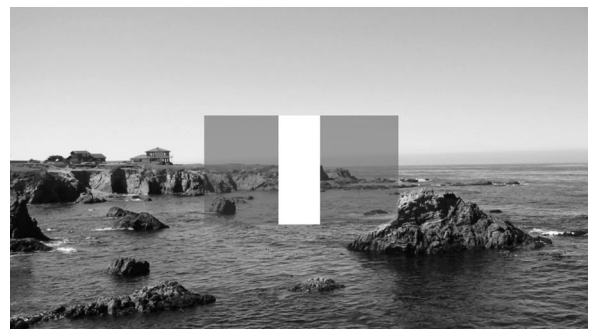
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FIGURE 6. OSD Timing Example



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FIGURE 7. Opaque OSD Background



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FIGURE 8. Transparent OSD Background

Application Information (Continued)

HIGHLIGHT WINDOW

The OSD Enable input to the LM1229 can also be used to highlight an area of the video by setting the DA bit to 0 (for digital OSD) and the TRANS bit to a 1. The OSD TRANS register must be set to some value higher than the CONTRAST register. Then whenever the OSD Enable input is high, the video will have the higher contrast setting. During this time the RGB OSD inputs must be kept at logic 0 to prevent them from overriding the video. Note also that since there is only one OSD TRANS register, the highlight window and the transparent OSD background cannot be used at the same time.

ANALOG OSD OPERATION

The LM1229 is configured for analog OSD operation by setting the DA bit, 0x0B[4], to 1. In this mode, the TRANS bit and OSD TRANS register have no effect. The inputs are AC coupled and clamped at the same time as the RGB video inputs for OSD black level stability. These inputs are selected when the OSD Enable input is high.

As in the digital mode, the contrast of the OSD can be controlled with the OSD_Cont bits, OSD[2:1]. The AUX bit, OSD[5], can be set to 1 to bypass the OSD contrast control and provide full amplitude analog OSD at the video outputs. This is still gated by the OSD Enable input level. See *Tables 2, 3* for details.

National Semiconductor does not recommend using the OSD inputs with both analog and digital sources in the same design. When configured for analog, the OSD inputs are vulnerable to digital logic levels and damage could occur to the LM1229 unless 100Ω resistors are used in series with these three inputs. These resistors should also be used in the digital OSD mode. It very important to make the OSD inputs AC coupled with 1000 pF capacitors in the analog mode for black level clamping of the OSD inputs and to prevent serious disruption of the video processing.

OSD CONTRAST

The OSD contrast amplitude is adjustable to four levels and is set with the OSD register, OSD[1:0]. *Table 3* gives the OSD amplitudes at the RGB outputs when the RGB outputs have each been set to 2.9V peak to peak. An "X" in the table indicates bits which have no effect under the given conditions.

DAC OUTPUTS

The three DAC outputs can be used to bias the CRT cathodes using one of the NSC bias IC family. The outputs are full scale (0.5V to 4.2V) or half scale (0.5V to 2.1V). Since the controlling registers are eight bits, the approximate step size is either 16 mV or 8 mV. Used in combination with a

clamp IC having a gain of -30, the half scale mode gives a bias range of 60V and a step size of 240 mV at the cathode.

HEHT COMPENSATION

The HEHT input can be used to change the horizontal phase in response to CRT beam current loading and high voltage droop. The compensation is register controlled and as the input voltage drops from 3.5V to 1.5V, the resulting phase change is a maximum of ±4.4%. The percentages shown in *Table 4*, are for an external 20k resistor connected between pins 21 and 24 (REHT1 and REHT2). Scaling this resistor will change these percentages proportionately.

FREQ1 AND FREQ2

The frequency selection for these pins is shown in *Table 1*. A series 100Ω resistor is recommended regardless of whether these pins are fixed biased to V_{CC} or GND, or connected to a microcontroller. If either pin is floated for the frequency selection, it may be desirable to use a 0.1 μF bypass capacitor to ground in series with the 100Ω resistor to prevent noise from changing the frequency selection.

ALIGNMENT

During factory alignment of the display, there are registers which are interactive. Two of these are the vertical size, VSIZE[7:0], and the S correction, S[6:0]. When the S correction is increased the vertical size will naturally decrease due to the changing shape of the V_{DRIVE} output. During alignment this can be compensated by writing both registers at the same time. An approximate rule of thumb is to increase the VSIZE register by the same amount as the S register. Experimentation will give the best algorithm to use to keep the overall vertical size constant.

The C correction adjustment is interactive with the vertical position register VPOS[7:0]. As the C register is lowered from the mid-range value of 0x3F (decimal 63), the position of the raster will move up due to the changing shape of the V_{DRIVE} output. To compensate for this the vertical position must be lowered by increasing the VPOS register value. An approximate rule of thumb is to change the VPOS register in the opposite direction from the C register by about half as much. In other words, if the C register is lowered from 63 to 53, the VPOS register should be increased by about 5.

ESD PROTECTION

The LM1229 uses internal circuitry to protect itself against damage from ESD transients. This self-protection activates when any input pin is driven above the V_{CC} supply or below ground, and results in unpredictable behaviour during this time. In order to avoid any unpredictable behaviour in normal use, external protection diodes should be used on any pin where the input can go beyond the supply voltage or below ground. See the recommendation for the HSYNC and VSYNC input pins.

Tables

These are the tables which are referenced in the text.

TABLE 1. Scan Frequencies

FREQ1 (JP1)	FREQ2 (JP2)	FREE RUN (kHz)	TV MODE (kHz)
float	x	15.7	15.734
0	0	28.1	28.1
0	float	31.4	31.468
0	1	33.8	33.750, 33.716
1	0	37.9	37.9
1	float	45.1	45.000
1	1	48.0	48.077 (SVGA)

TABLE 2. OSD Modes

TRANS	ENABLE	ANALOG OSD (DA = 1)	DIGITAL OSD (DA = 0)
0	0	Normal video display.	Normal video display.
0	1	Foreground and background determined by OSD inputs.	Foreground and background determined by OSD inputs.
1	0	Normal video display.	Normal video display.
1	1	Foreground and background determined by OSD inputs. OSD TRANS register is ignored.	OSD window background is video, with contrast from OSD TRANS register, 0x0A[6:0].

TABLE 3. OSD Peak to Peak Amplitudes

RGB IN	OSD ENABLE	OSD INPUT	OSD[1:0]	AUX	DA	OSD/AUX PERCENT	OSD OUTPUT	VIDEO OUTPUT	
0.70V	logic 1	0.7V analog (DA = 1) or digital @ logic 1 (DA = 0)	0 0	X	1,0	55	1.60V	2.90V	
			0 1	X	1,0	65	1.89V	2.90V	
			1 0	X	1,0	75	2.18V	2.90V	
			1 1	X	1,0	85	2.47V	2.90V	
	logic 0	any	digital @ logic 0	X X	X	0	0	0V	2.90V
			0.7V analog	X X	1	1	100	2.90V	2.90V

TABLE 4. HEHT Compensation

Input	$\Delta\Phi$	Conditions
Changing from 3.5V to 1.5V ($R_{EHT} = 20k$)	$\Delta\Phi = 4.43\%$ left	HEHT register = 0011b
	3.81% left	0010b
	3.17% left	0001b
	2.56% left	0000b
	$\Delta\Phi = 0$	HEHT register = 1xxx b
	$\Delta\Phi = 4.45\%$ right	HEHT register = 0111b
	3.81% right	0110b
	3.17% right	0101b
	2.56% right	0100b

Microcontroller Interface

I²C COMMUNICATION

The microcontroller interfaces to the LM1229 preamp using the I²C compatible interface. The protocol begins with a Start Pulse followed by a byte comprising of a seven bit Slave Device Address and a Read/Write bit. Since the first byte is composed of both the address and the read/write bit, the address of the LM1229 for writing is 0xBA (10111010b) and the address for reading is 0xBB (10111011b). The development software provided by National Semiconductor will automatically take care of the difference between the read and write addresses if the target address under the communications tab is set to 0xBA. *Figures 9, 10* show a write and read sequence on the I²C compatible interface.

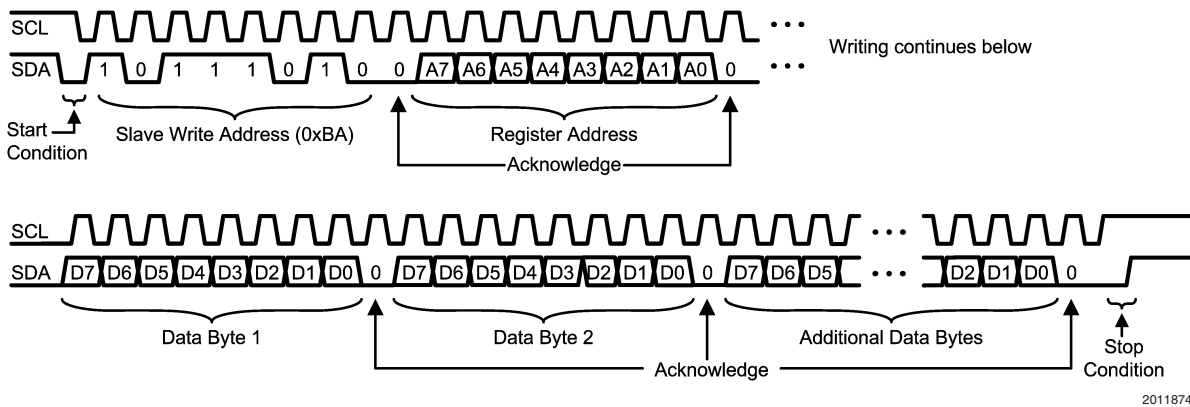
WRITE SEQUENCE

The write sequence begins with a start condition which consists of the master pulling SDA low while SCL is held high. The Slave Device Write Address, 0xBA, is sent next. Each byte that is sent is followed by an acknowledge. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The register to be written to is the next byte sent. The master can then send the data,

which consists of one or more bytes. Each data byte is followed by an acknowledge bit. If more than one data byte is sent the data will increment to the next address location. See *Figure 9*.

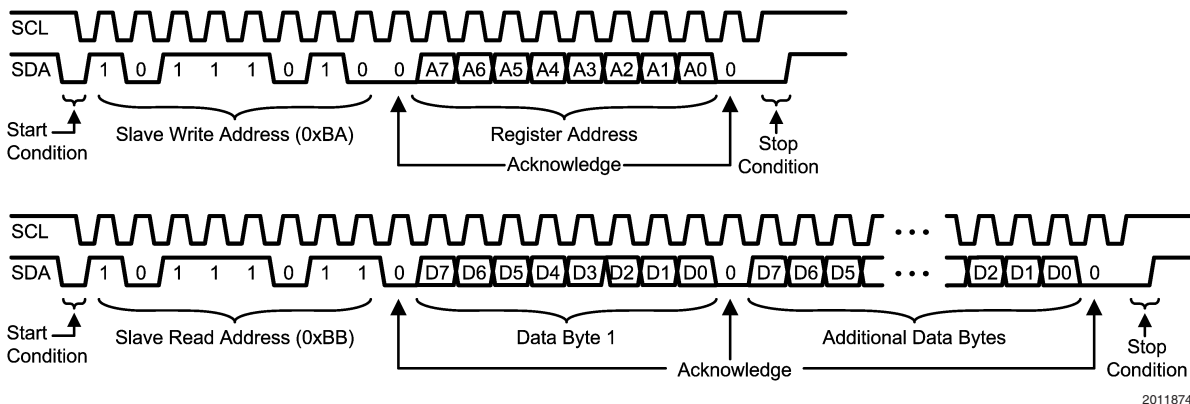
READ SEQUENCE

Read sequences are comprised of two I²C compatible transfer sequences: The first is a write sequence that only transfers the two byte address to be accessed. The second is a read sequence that starts at the address transferred in the previous address only write access and increments to the next address upon every data byte read. This is shown in *Figure 10*. The write sequence consists of the Start Pulse, the Slave Device Write Address (0xBA), and the Acknowledge bit; the next byte is the address to be accessed, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access. Next the read data access will be performed beginning with the Start Pulse, the Slave Device Read Address (0xBB), and the Acknowledge bit. The next 8 bits will be the actual data sent by the LM1229 preamp as clocked out by the Master. Subsequent bytes that are read will correspond to the next incremented address locations.



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FIGURE 9. I²C Compatible Write Sequence



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FIGURE 10. I²C Compatible Read Sequence

APPLICATION CONTROL REGISTERS

Tables 5, 6 show the LM1229 RGB and deflection application control registers. Care should be taken to avoid writing

or reading any register outside this range as National Semi-

Microcontroller Interface (Continued)

Register bits indicated by an "X" are not used and should be written to with 0's when the register is updated.

conductor may use some additional addresses for production testing. Writing to an address outside the ranges shown here could have unpredictable or even destructive results.

Note the address gap between the RGB and deflection control registers. This allows for future expansion of each without changing existing registers.

TABLE 5. RGB Application Registers

Register	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RED GAIN	0x00	0x60	X	RGAIN[6:0]						
GREEN GAIN	0x01	0x60	X	GGAIN[6:0]						
BLUE GAIN	0x02	0x60	X	BGAIN[6:0]						
CONTRAST	0x03	0x60	X	CONTRAST[6:0]						
DAC 1	0x04	0x00	DAC1[7:0]							
DAC 2	0x05	0x00	DAC2[7:0]							
DAC 3	0x06	0x00	DAC3[7:0]							
BRIGHTNESS	0x07	0x80	BRIGHTNESS[7:0]							
OFFSET	0x08	0x0C	X	X	X	X	DC_Offset[3:0]			
GLOBAL	0x09	0x00	INCR	X	DCF	VB	CLAMP	HB	PSAVE	BLANK
OSD TRANS	0x0A	0x00	X	TRANS[6:0]						
OSD	0x0B	0x02	OOD	X	AUX	DA	TRANS	X	OSD_Cont[1:0]	
RESET	0x0C	0x00	X	X	X	X	X	X	X	SRST

TABLE 6. Deflection Application Registers

Register	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	0x40	N/A	X	X	X	X	VPROT	XRay	FBP	HLOCK
HPOS	0x41	0x40	H_POS[7:0]							
HEHT	0x42	0xA8	EQPRM	XRayOff	HOFF	HPCOff	EHTEN	POL	HEHT[1:0]	
PAR	0x43	0x80	PAR[7:0]							
PIN_BAL	0x44	0x80	PIN_BAL[7:0]							
VSIZE	0x45	0x80	VSIZE[7:0]							
VEHT	0x46	0x88	VEHT2[7:4]				VEHT1[3:0]			
C	0x47	0x40	X	C[6:0]						
S	0x48	0x00	X	S[6:0]						
VPOS	0x49	0x80	VPOS[7:0]							
HSIZE	0x4A	0x40	X	HSIZE[6:0]						
PIN	0x4B	0x40	X	PIN[6:0]						
T_CORNER	0x4C	0x40	X	T_CORNER[6:0]						
B_CORNER	0x4D	0x40	X	B_CORNER[6:0]						
TRAP	0x4E	0x40	X	TRAP[6:0]						
DYN_FOCUS	0x4F	0x40	X	DYN_FOCUS[6:0]						
SYNCPOL	0x50	0x3B	X	X	VPD	V2D	V1D	SERV	VPOL	HPOL
VBLANK	0x51	0x00	X	VBLANK[7:0]						

Application Register Detail

RED Gain Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RED GAIN	0x00	X	RGAIN[6:0]						

Bits 6–0 Sets the gain level of the red video channel. A value of 0x7F generates the maximum red gain. A value of 0x00 generates the minimum red gain.

Application Register Detail (Continued)

GREEN Gain Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GREEN GAIN	0x01	X	GGAIN[6:0]						

Bits 6–0: Sets the gain level of the green video channel. A value of 0x7F generates the maximum green gain. A value of 0x00 generates the minimum green gain.

BLUE Gain Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLUE GAIN	0x02	X	BGAIN[6:0]						

Bits 6–0: Sets the gain level of the blue video channel. A value of 0x7F generates the maximum blue gain. A value of 0x00 generates the minimum blue gain.

CONTRAST Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONTRAST	0x03	X	CONTRAST[6:0]						

Bits 6–0: Sets the contrast level three video channels. A value of 0x7F generates the maximum contrast. A value of 0x00 generates the minimum contrast.

DAC 1 Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC 1	0x04	DAC1[7:0]							

Bits 7–0: Sets the DAC 1 DC output level at pin 39. A full scale value of 0xFF generates the maximum DC output level. A value of 0x00 generates the minimum DC level.

DAC 2 Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC 2	0x05	DAC2[7:0]							

Bits 7–0: Sets the DAC 2 DC output level at pin 38. A full scale value of 0xFF generates the maximum DC output level. A value of 0x00 generates the minimum level.

DAC 3 Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAC 3	0x06	DAC3[7:0]							

Bits 7–0: Sets the DAC 3 DC output level at pin 37. A full scale value of 0xFF generates the maximum DC output level. A value of 0x00 generates the minimum level.

BRIGHTNESS Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRIGHTNESS	0x07	BRIGHTNESS[7:0]							

Bits 7–0: Sets the brightness level of the RGB outputs. A full scale value of 0xFF generates the minimum DC video black level (darkest). A value of 0x00 generates the maximum DC black level (brightest).

OFFSET Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OFFSET	0x08	X	X	X	X	DC_Offset[3:0]			

Bits 3–0: Determines the video reference level at the RGB video outputs on pins 57, 58 and 59. A setting of 0xF gives a DC Offset of about 0.5V and 0x0 gives a DC Offset of about 1.4V.

GLOBAL

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GLOBAL	0x09	INCR	X	DCF	VB	CLAMP	HB	PSAVE	BLANK

Bit 7: When set to 0, the I²C auto increment function is active. When set to a 1, the I²C auto increment function is disabled. In the auto increment mode, a given register can be updated continuously using an ADDR - DATA - DATA - ... - DATA transmission sequence.

Bit 5: When set to 0, the outputs of DACs 1–3 are full scale (0V–4.2V). When this bit is a 1, the output DC range is halved

Application Register Detail (Continued)

(0V–2.1V).

- Bit 4: When set to 0, vertical blanking of the RGB outputs is disabled. When set to 1, vertical blanking is enabled.
- Bit 3: When set to 0, the LM1229 clamps the input video when the input clamp pulse is high. When set to 1 the LM1229 expects a negative going pulse.
- Bit 2: When set to 0, horizontal blanking at the RGB outputs is disabled. When set to 1, horizontal blanking is enabled.
- Bit 1: When set to 0, the LM1229 is in normal operation. When set to 1, it is put into the power save mode for reduced power consumption.
- Bit 0: When set to 0, normal video appears at the RGB outputs. When set to 1, the RGB outputs are set to the blanking level as given in the specification section.

OSD TRANSPARENCY

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSD TRANS	0x0A	X	OSD TRANS[6:0]						

Bits 6–0: These bits determine the amount of video in the OSD background at the times when the OSD Enable input is active and when there is no OSD foreground. When set to 0x00, the video background is at minimum contrast and when set to 0x7F, the video background is at maximum contrast.

OSD Control

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSD	0x0B	OOR	X	AUX	DA	TRANS	X	OSD_Cont[1:0]	

- Bit 7: This is the OSD override bit. This will be read as a 0 for normal operation. When set to a 1, the video outputs are disconnected and OSD only is displayed. This is useful for the OSD display of special conditions such as “No Signal”, or other information to the user.
- Bit 5: This bit controls whether the analog OSD gain is set to maximum. When this bit is a 0 and bit 4 is a 1, the analog OSD output levels are determined by the input level and OSD_Cont[1:0]. When this bit is a 1 and DA is a 1, the output levels are determined by the input level only, with a gain of 4.14. When DA is a 0 for digital OSD inputs, this bit has no effect. See *Table 3*.
- Bit 4: When set to a 0, the LM1229 is configured for digital OSD inputs. When set to a 1, the OSD inputs are configured for 0V–0.7V analog.
- Bit 3: When set to a 0, the OSD background is determined by the OSD Enable input, such that when the enable is active the video is set to black. When this bit is set to a 1 the OSD background is video attenuated by the OSD Transparency register, 0x0A, but only while the OSD Enable input is a 1. See *Table 2*.

Bits 1–0: These bits determine the contrast level of the OSD. Refer to *Table 3* for amplitudes.

RESET

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESET	0x0C	X	X	X	X	X	X	X	SRST

Bit 0: Setting this bit to a 1 causes a software reset. All registers (except this one) are loaded with their default values. All operations currently in progress are aborted (except for I²C transactions). This bit automatically clears itself when the reset has been completed.

STATUS

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	0x40	X	X	X	X	VPROT	XRay	FBP	HLOCK

- Bit 3: This is the Vertical Protection status. This bit is a 0 for normal operation, and is a 1 if Vertical Protection is triggered and the R, G, B, video outputs are blanked. This will reset to 0 when a good vertical drive signal is present.
- Bit 2: This bit is 0 if X-Ray is not triggered, 1 if X-Ray triggered. It will reset to 0 when $V_{CC} \leq 4V$.
- Bit 1: Flyback pulse, 0 if good flyback pulse present, 1 if bad flyback pulse or no flyback pulse.
- Bit 0: This is the horizontal deflection lock bit. It is 1 if HSYNC is present and the PLL is locked to it. It is a 0 if no HSYNC is present or if the PLL is not locked to HSYNC.

HORIZONTAL POSITION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HPOS	0x41	HPOS[7:0]							

Bits 7–0: Sets the horizontal position of the picture on the CRT. When set to minimum the picture is to the left, and when set to maximum the picture is to the right.

Application Register Detail (Continued)

HORIZONTAL EHT CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HEHT	0x42	EQPRM	XRayOff	HOFF	HPCOFF	EHTEN	POL	HEHT[3:0]	

- Bit 7: When this bit is a 0, no attempt is made to remove HSYNC equalizing pulses. When set to a 1, HSYNC equalizing pulses are removed.
- Bit 6: When this bit is a 0, the XRay protection is functional. When set to a 1, the XRay protection is disabled.
- Bit 5: When set to a 1, HDRIVE output is off and the output will be pulled high by the external pullup resistor (this is the power up default). When this bit is a 0, the HDRIVE output is functional.
- Bit 4: When this bit is a 0, the horizontal phase corrections (parallelogram and bow) are functional. When set to a 1, these corrections are disabled.
- Bit 3: When this bit is 0 the HEHT compensation is enabled. When a 1, compensation is disabled.
- Bit 2: This is the compensation polarity bit. When it is a 0, a reduction in the voltage at pin 20 causes the picture to shift to the left. When it is a 1, the shift is to the right.
- Bits 1–0: These two bits determine the amplitude of the phase correction. When both are both 0, the compensation is a minimum (not zero) and is determined by the external resistor R_{EHT} connected between pins 21 and 24. When these bits are 01 through 11, the compensation is increased according to *Table 4*.

PARALLELOGRAM CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAR	0x43	PAR[7:0]							

- Bits 7–0: Sets the parallelogram correction which can be either polarity. A value of 0x7F gives no correction. A value of 0x00 tilts the picture to the right and 0xFF tilts the picture to the left.

PINCUSHION BALANCE (BOW)

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIN_BAL	0x44	PIN_BAL[7:0]							

- Bits 7–0: Sets the amount of pin balance (bow) correction which can be either polarity. A value of 0x7F gives no correction. A value of 0x00 bows the top and bottom to the left. A value of 0xFF bows the top and bottom to the right.

VERTICAL SIZE

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSIZE	0x45	VSIZE[7:0]							

- Bits 7–0: Sets the amplitude of the vertical ramp. 0x00 gives minimum size and 0xFF gives maximum size.

VERTICAL EHT CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
VEHT	0x46	VEHT2[7:4]				VEHT1[3:0]				

- Bits 7–4: Sets the amount of EW EHT correction. This can be disabled with bit 4 of the SYNCPOL register.

- Bits 4–0: Sets the amount of vertical drive EHT correction. This can be disabled with bit 3 of the SYNCPOL register.

'C' CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C	0x47	X	C[6:0]						

- Bits 6–0: Sets the amount of C correction which can be either polarity. A value of 0x3F gives no correction. Smaller values will stretch the lower part of the screen. Larger values will stretch the upper part of the screen.

'S' CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S	0x48	X	S[6:0]						

- Bits 6–0: Sets the amount of S correction. 0x00 gives no correction and 0x7F gives maximum correction.

VERTICAL POSITION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VPOS	0x49	VPOS[7:0]							

Application Register Detail (Continued)

Bits 7–0: Sets the DC level of the vertical ramp that is used to move the picture up and down. In a typical application, a setting of 0xFF will move the raster image to the lowest position and 0x00 moves it to the highest position.

HORIZONTAL SIZE

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HSIZE	0x4A	X	HSIZE[6:0]						

Bits 6–0: Sets the DC level of the 2nd order waveform (parabola) sent to EW to control horizontal size. In a typical application a setting of 0x7F produces minimum width and 0x00 produces maximum width.

PINCUSHION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIN	0x4B	X	PIN[6:0]						

Bits 6–0: Sets the amplitude of the 2nd order waveform sent to EW for pincushion. A value of 0x00 gives no parabola and a value of 0x7F gives the maximum amount of correction.

TOP CORNER CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T_CORNER	0x4C	X	T_CORNER[6:0]						

Bits 5–0: Sets the amplitude of the 4th order waveform sent to EW for top corner correction. A value of 0x3F gives no correction. A value of 0x00 gives maximum top width and 0x7F gives minimum top width.

BOTTOM CORNER CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B_CORNER	0x4D	X	B_CORNER[6:0]						

Bits 5–0: Sets the amplitude of the 4th order waveform sent to EW for bottom corner correction. A value of 0x3F gives no correction. A value of 0x00 gives maximum bottom width and 0x7F gives minimum bottom width.

TRAPEZOIDAL CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRAP	0x4E	X	TRAP[6:0]						

Bits 5–0: Sets the amount of trapezoid correction. A value of 0x3F gives no correction. A value of 0x00 gives a picture with a narrow top and 0x7F gives a picture with a wide top.

DYNAMIC FOCUS CORRECTION

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DYN_FOCUS	0x4F	X	DYN_FOCUS[6:0]						

Bits 5–0: Sets the amplitude of the dynamic focus. A value of 0x00 gives no correction and a value of 0x7F gives the maximum correction.

SYNC POLARITY

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNCPOL	0x50	X	X	VPD	V2D	V1D	SERV	VPOL	HPOL

Bits 5: When set to a 1, this bit disables the vertical protect function (the power up default). This allows the LM1229 vertical section to operate without a vertical flyback input and still keep the RGB outputs operating normally, without blanking them. This bit must be set to a 0 to enable the vertical protect function.

Bit 4: When this bit is a 0, the VEHT2 compensation is functional. When this bit is a 1, the VEHT2 compensation is disabled.

Bit 3: When this bit is a 0, the VEHT1 compensation is functional. When this bit is a 1, the VEHT1 compensation is disabled.

Bit 2: When this bit is set to a 0, the vertical output ramp is active. When set to a 1, the ramp is turned off (set to the vertical DC reference) to produce the service line used for color temperature setup.

Bit 1: When this bit is set to a 0, the LM1229 expects negative going vertical sync input. When this bit is a 1, it expects positive going sync.

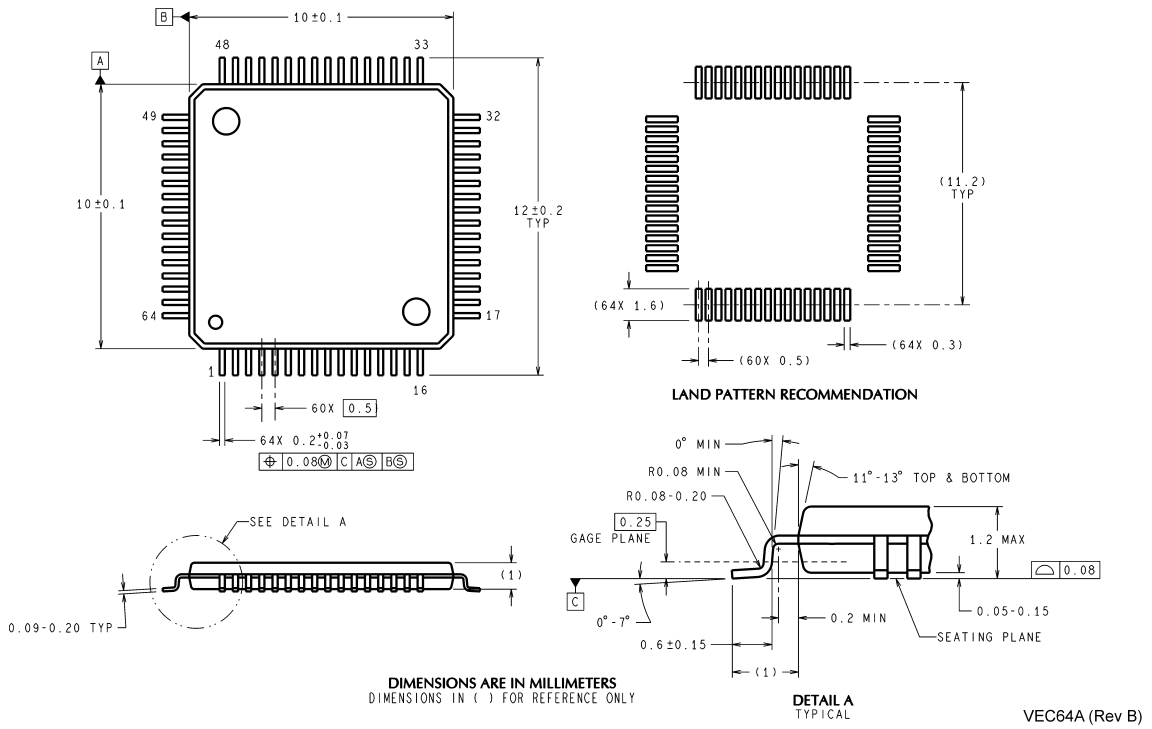
Bit 0: When this bit is set to a 0, the LM1229 expects negative going horizontal sync input. When this bit is a 1, it expects positive going sync.

Application Register Detail (Continued)**VERTICAL BLANKING OUTPUT**

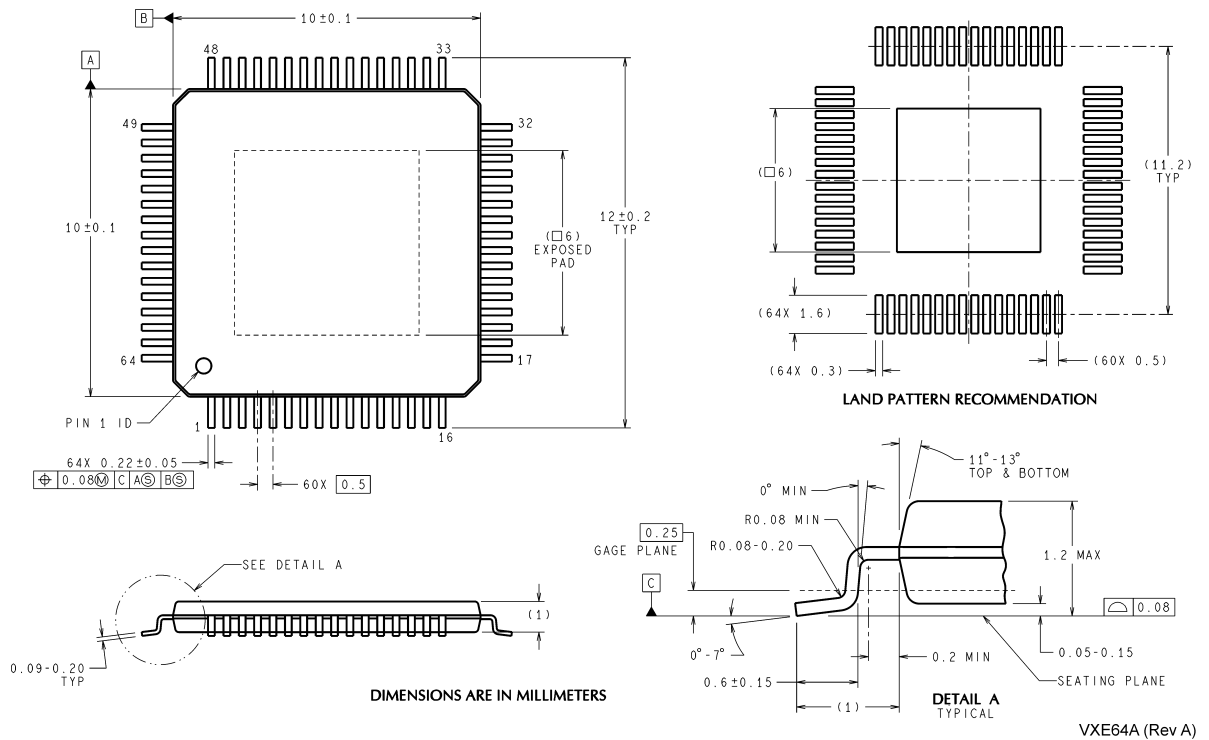
Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VBANK	0x51	X	VBANK[7:0]						

Bits 6–0: These bits determine the duration of the vertical blanking output in horizontal lines, as counted by the horizontal sync input.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM1229VEC
NS Package Number VEC64A



Order Number LM1229YA
NS Package Number VXE64A

Notes

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