78C 05899 D

THOMSON SEMICONDUCTORS

LM11M
LM11C
LM11LC

T-79-06-10

PRECISION SINGLE OP-AMPs / BUFFERS

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been improved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (– 55°C to + 125°C) are :

- Offset voltage : 100 µV (200 µV)
- Bias current : 25 pA (65 pA)
- Offset current : 0.5 pA (3 pA)
- Temperature drift : 1 µV/°C
- Long-term stability : 10 µV/year.

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low resistance potentiometer.

Otherwise, the device is the electrical equivalent of the LM108A, except that the negative common-mode limit is 0.6 V less, performance is specified down to ±2.5 V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obvious applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations.

The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

ORDERING INFORMATION

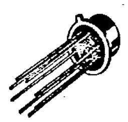
Hi-Rel versions available - See chapter 14

PART NUMBER	TEMPERATURE RANGE	PACKAGE		
		DP	H	GC
LM11M	– 55°C to + 125°C		•	•
LM11C	0°C to + 70°C	•	•	
LM11LC	0°C to + 70°C	•	•	
Examples : LM11MH, LM11CDP				

PRECISION SINGLE OPERATIONAL AMPLIFIERS / BUFFERS

CASES

CB-11 (TO-99)



H SUFFIX
METAL CAN

CB-98

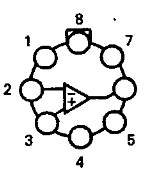
DP SUFFIX
PLASTIC PACKAGE

CB-705

GC SUFFIX
TRICECOP (LCC)

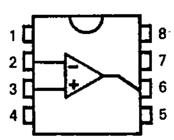
PIN CONFIGURATIONS
(Top views)

CB-11

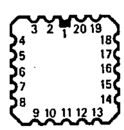


1 - Balance
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Compensation
6 - Output
7 - V_{CC}^+
8 - Balance

CB-98



CB-705



1 - NC
2 - Balance
3 - NC
4 - NC
5 - Inverting input
6 - NC
7 - Non-inverting input
8 - NC
9 - NC
10 - V_{CC}^-
11 - NC
12 - Compensation
13 - NC
14 - NC
15 - Output
16 - NC
17 - V_{CC}^+
18 - NC
19 - NC
20 - Balance

Réf. 00130

THOMSON SEMICONDUCTORS
Sales headquarters
45, av. de l'Europe - 78140 VELIZY - FRANCE
Tel. : (3) 946 97 19 / Telex : 204780 F

THOMSON COMPONENTS

MAXIMUM RATINGS

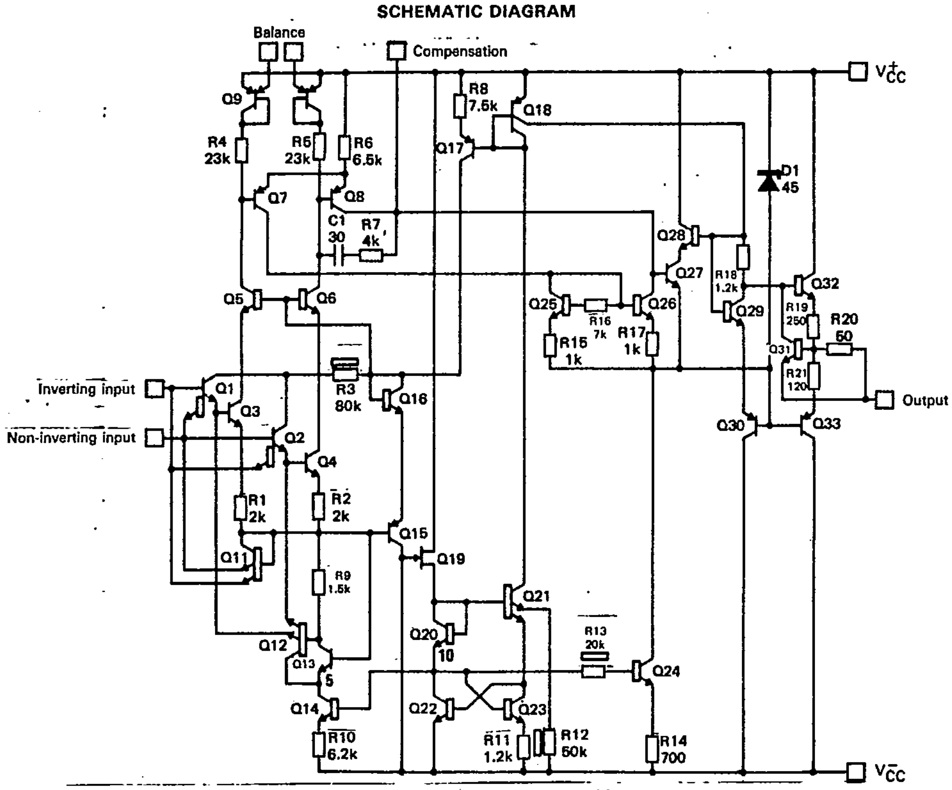
Rating	Symbol	Value	Unit
Total supply voltage	V_{CC}	40	V
Input current (Note 1)	I_I	±10	mA
Power dissipation (Note 2)	P_{tot}	500	mW
Output short-circuit duration (Note 3)	–	Indefinite	–
Lead temperature (soldering, 10 seconds)	T_{lead}	300	°C
Operating free-air, temperature range LM11M, LM11C, LM11LC	T_j	–55 to +125 0 to + 70	°C
Storage temperature range	T_{stg}	–65 to +150	°C

Note 1 : The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

Note 2 : The maximum operating-junction temperature is +150°C for the LM11M and 85°C for the LM11C, LC. Devices must be derated based on package thermal resistance (see physical dimensions).

Note 3 : Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

SCHEMATIC DIAGRAM



CASE	Inverting input	Non-inverting input	Output	V_{CC}^-	V_{CC}^+	Balance	Compensation	N.C.
CB-98 CB-11	2	3	6	4	7	1,8	5	–
CB-705	5	7	15	10	17	2,20	12	•

• CB-705 : Other pins are not connected

ELECTRICAL CHARACTERISTICS

$T_j = +25°C$, $(V_{CC}^- + 2\ V) \leq V_{CM} \leq (V_{CC}^+ - 1\ V)$ and $\pm 2.5\ V \leq V_{CC} \leq \pm 20\ V$
$T_{min} \leq T_j \leq T_{max}$: $(V_{CC}^- + 2.5\ V) \leq V_{CM} \leq (V_{CC}^+ - 1\ V)$ and $\pm 2.5\ V \leq V_{CC} \leq \pm 20\ V$
(Unless otherwise specified)

Characteristic	Symbol	LM11M			LM11C			LM11LC			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input offset voltage	V_{IO}										mV
$T_j = +25°C$		–	0.1	0.3	–	0.2	0.6	–	0.5	5	
$T_{min} \leq T_j \leq T_{max}$		–	–	0.6	–	–	0.8	–	–	6	
Input offset current	I_{IO}										pA
$T_j = +25°C$		–	0.5	10	–	1	10	–	4	25	
$T_{min} \leq T_j \leq T_{max}$		–	–	30	–	–	20	–	–	50	
Input bias current	I_{IB}										pA
$T_j = +25°C$		–	25	50	–	40	100	–	70	200	
$T_{min} \leq T_j \leq T_{max}$		–	–	150	–	–	150	–	–	300	
Input resistance	R_I	–	10^{11}	–	–	10^{11}	–	–	10^{11}	–	Ω
Offset voltage drift ($T_{min} \leq T_j \leq T_{max}$)	αV_{IO}	–	1	3	–	2	5	–	3	–	µV/°C
Offset current drift ($T_{min} \leq T_j \leq T_{max}$)	αI_{IO}	–	20	–	–	10	–	–	50	–	pA/°C
Bias current drift ($T_{min} \leq T_j \leq T_{max}$)	αI_{IB}	–	0.5	1.5	–	0.8	3	–	1.4	–	pA/°C
Large signal voltage gain ($V_{CC} = \pm 15$ V)	A_V										V/mV
$T_j = +25°C$, $V_O = \pm 12$ V, $I_O = \pm 2$ mA		100	300	–	100	300	–	25	300	–	
$I_O = \pm 0.5$ mA		250	1200	–	250	1200	–	50	800	–	
$T_{min} \leq T_j \leq T_{max}$, $V_O = \pm 12$ V, $I_O = \pm 0.5$ mA		100	–	–	100	–	–	30	–	–	
$V_O = \pm 11.5$ V, $I_O = \pm 2$ mA		50	–	–	50	–	–	15	–	–	
Common-mode rejection ratio ($V_{CC} = \pm 15$ V)	CMR										dB
$T_j = +25°C$, $-13\ V \leq V_{CM} \leq +14$ V		110	130	–	110	130	–	96	110	–	
$T_{min} \leq T_j \leq T_{max}$, $-12.5\ V \leq V_{CM} \leq +14$ V		100	–	–	100	–	–	90	–	–	
Supply voltage rejection ($\pm 2.5 \leq V_{CC} \leq \pm 20$ V)	SVR										dB
$T_j = +25°C$		100	118	–	100	118	–	84	100	–	
$T_{min} \leq T_j \leq T_{max}$		96	–	–	96	–	–	80	–	–	
Supply current	I_{CC}										mA
$T_j = +25°C$		–	0.3	0.6	–	0.3	0.8	–	0.3	0.8	
$T_{min} \leq T_j \leq T_{max}$		–	–	0.8	–	–	1	–	–	1	
Output short-circuit current ($T_j = +150°C$)	I_{OS}	–	–	±15	–	–	–	–	–	–	mA

APPLICATION HINTS

When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins. With the ceramic package, the floating metal lid is best connected to the guard. This might be accomplished with a dab of conductive paint.

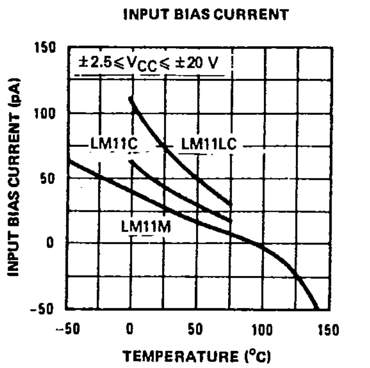
Electrostatic shielding of high impedance circuitry is advisable.

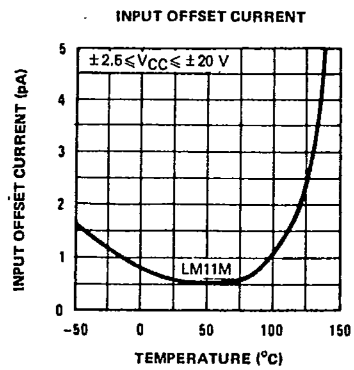
Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoiled by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together also help.

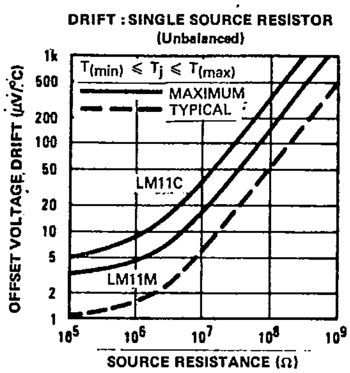
With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3 V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could results if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 µF bypass on the supply buss.

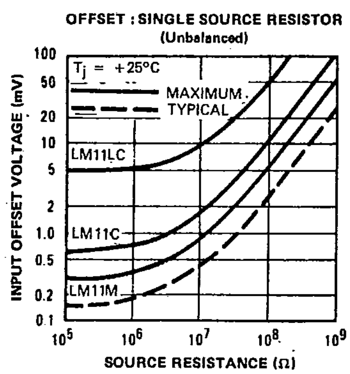
Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

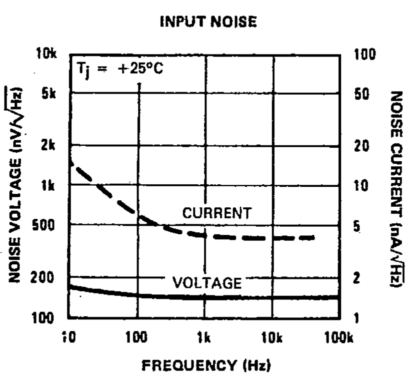
TYPICAL CHARACTERISTICS

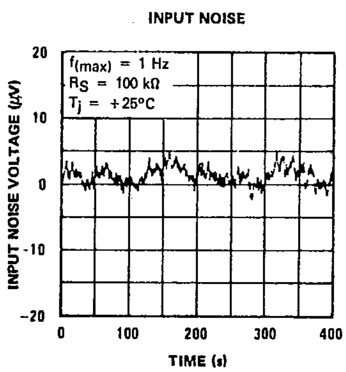




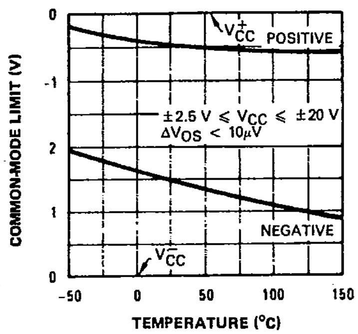




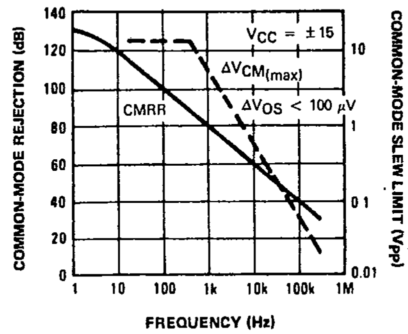




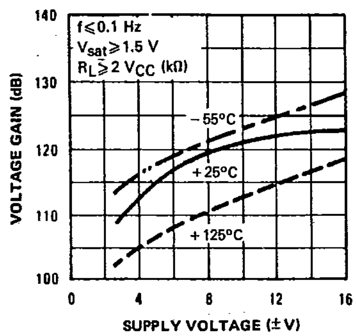
COMMON-MODE LIMITS



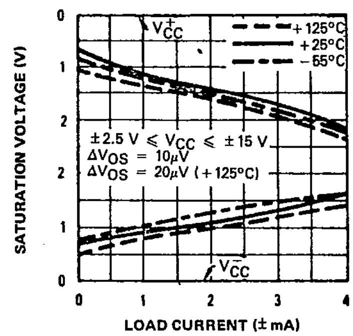
COMMON-MODE REJECTION



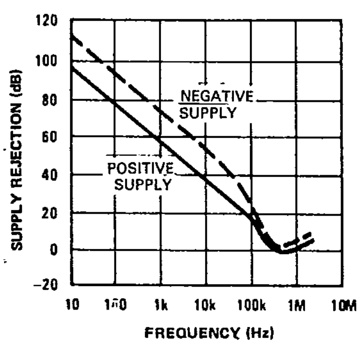
LARGE SIGNAL VOLTAGE GAIN



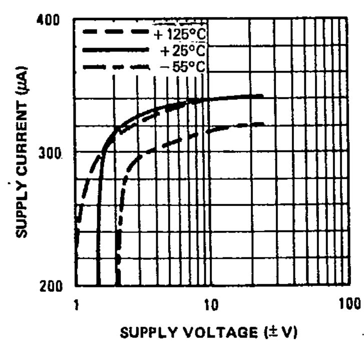
OUTPUT SATURATION THRESHOLD



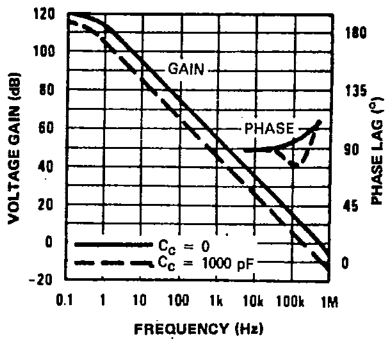
SUPPLY REJECTION



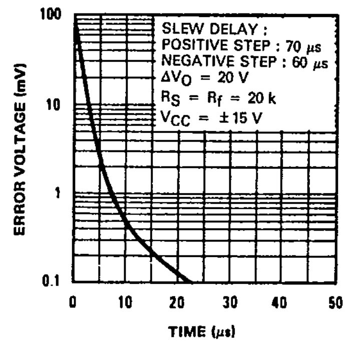
SUPPLY CURRENT



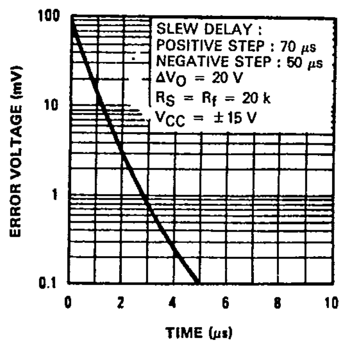
OPEN LOOP RESPONSE



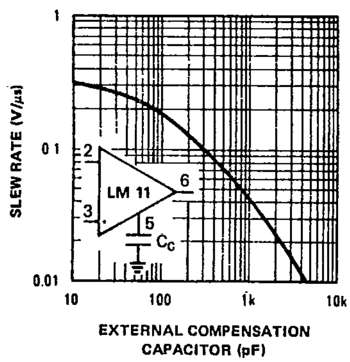
FOLLOWER FINAL SETTLING TIME



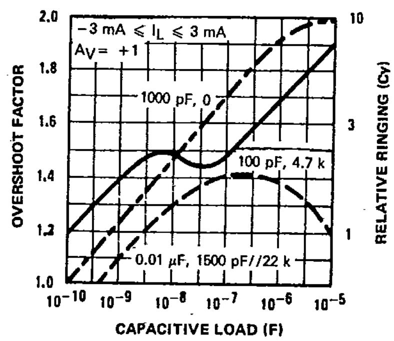
INVERTER FINAL SETTLING TIME



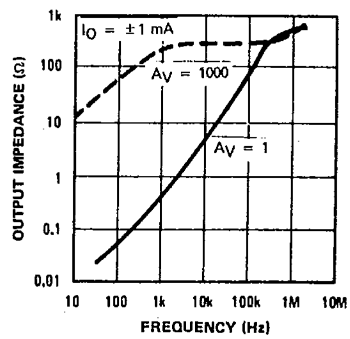
SLEW RATE



STABILITY WITH OVER-COMPENSATION

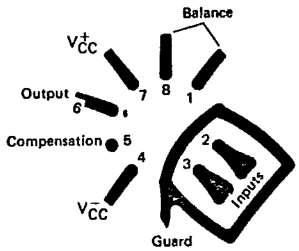


CLOSED LOOP OUTPUT IMPEDANCE



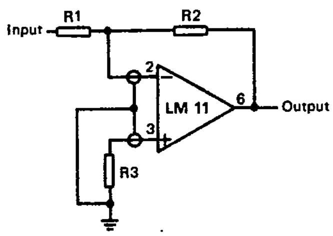
Input guarding

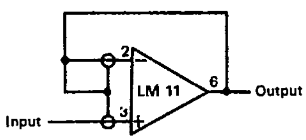
Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.

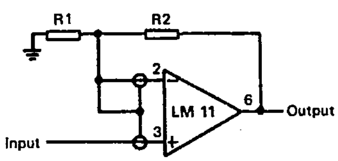


Bottom view

Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are shown here.

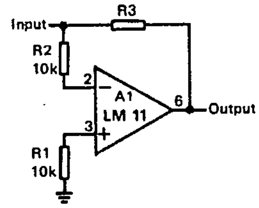




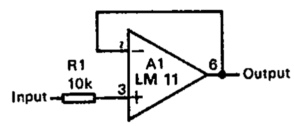


Input protection

Current is limited by R2 even when input is connected to voltage source outside common-mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.

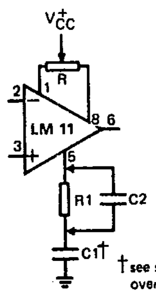


Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



Balancing and over-compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.

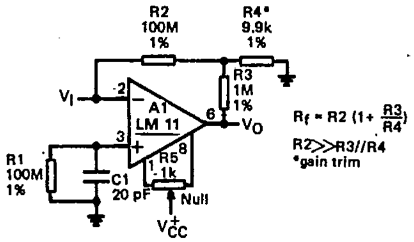


† see stability with over-compensation curve

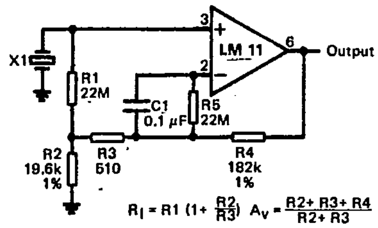
min. adj range	R
±5 mV	100 kΩ
±2	10k
±1	3k
±0.8	3k
±0.4	1k

Resistance multiplication

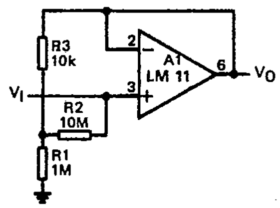
Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.



A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.

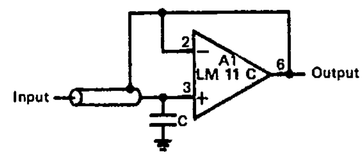


Follower input resistance is 1GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.

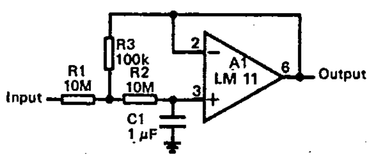


Cable bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



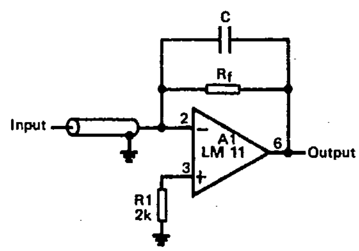
This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.



$$\tau = \frac{R1\,C}{R3}(R2 + R3)$$

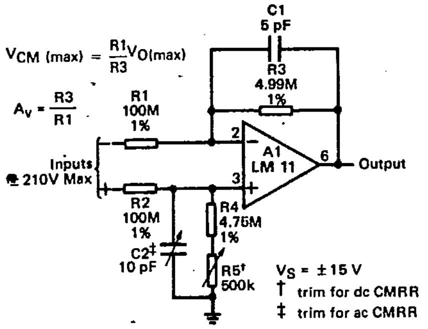
$$\Delta V_O = \frac{R1 + R3}{R3}(I_B R2 + V_{OS})$$

With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.

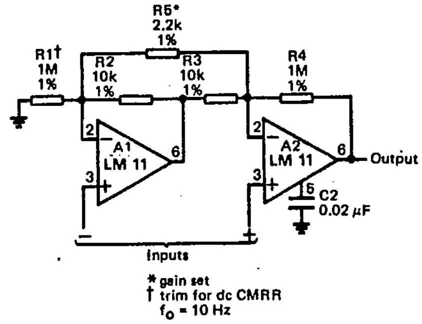


Differential amplifiers

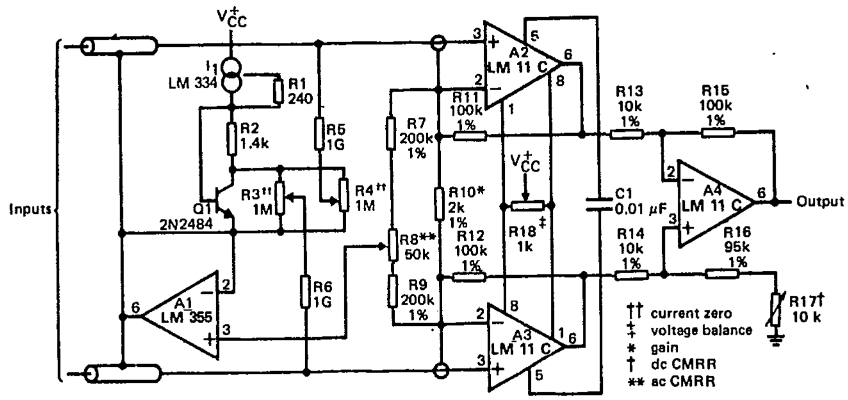
This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.



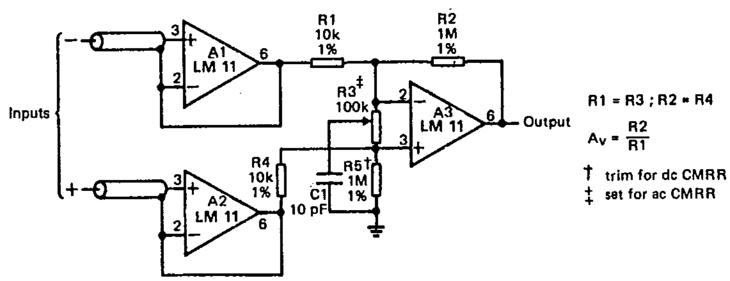
Two op-amp instrumentation amplifier has poor ac common-mode rejection. This can be improved at the expense of differential bandwidth with C2.



High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.

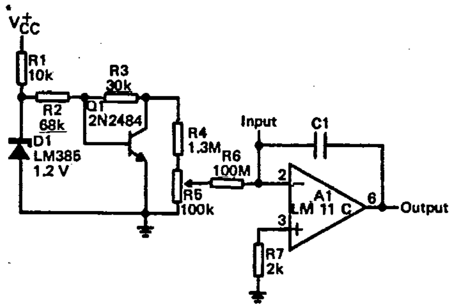


For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.

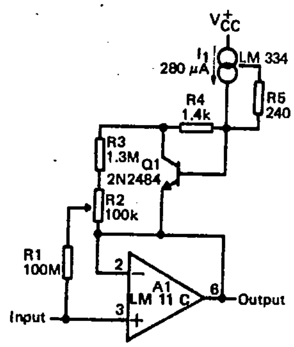


Bias current compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

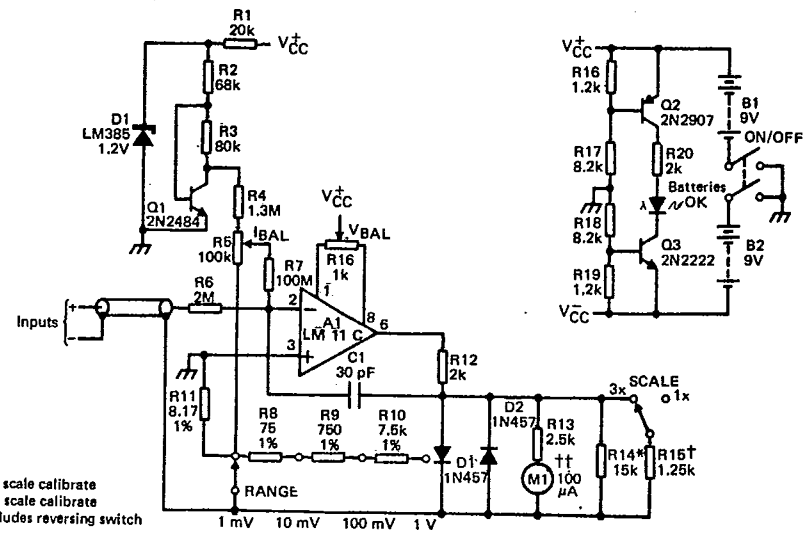


This circuit shows how bias current compensation can be used on a voltage follower.



Voltmeter

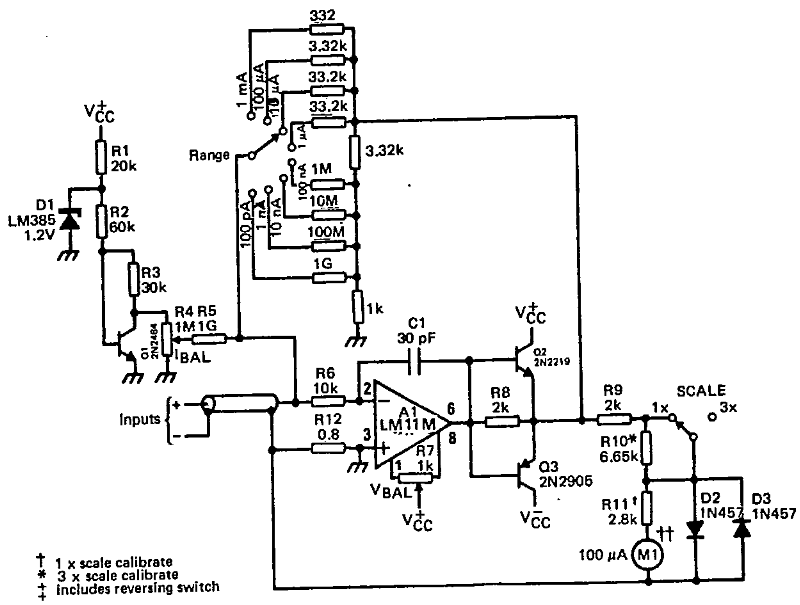
High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.



* 1 x scale calibrate
† 3 x scale calibrate
‡ includes reversing switch

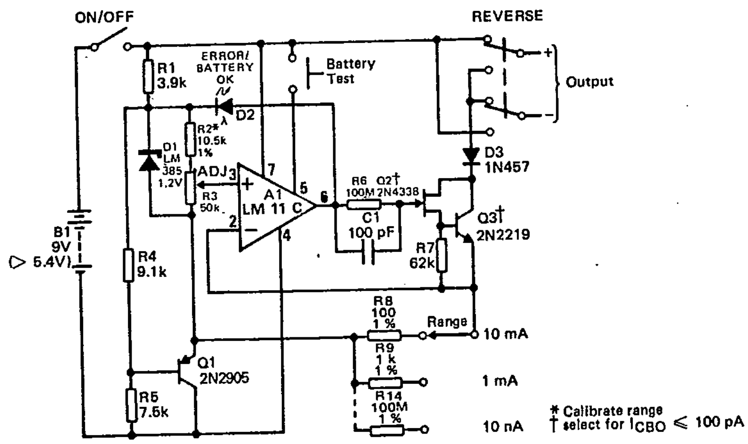
Ammeter

Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



Current source

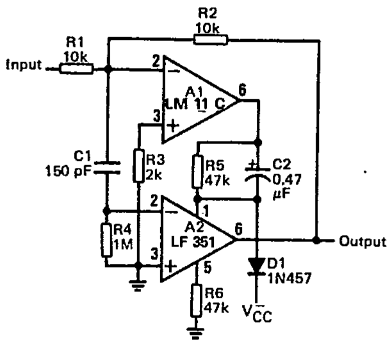
Precision current source has 10 μA to 10 mA ranges with output compliance of 30 V to −5 V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.

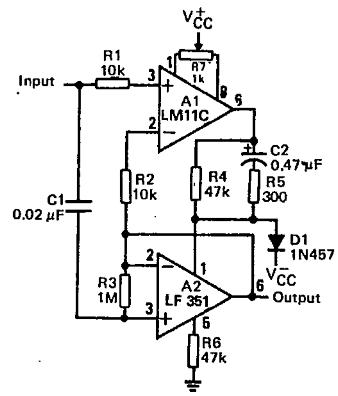


Fast amplifiers

These inverters have bias current and offset voltage of LM 11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 µs. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.

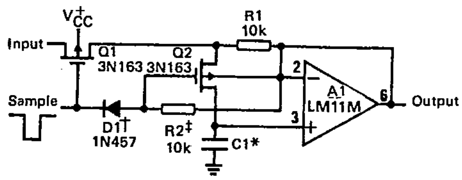
Follower has 10 µs setting to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.





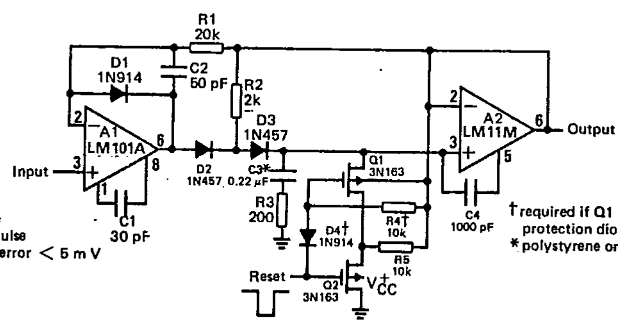
Leakage isolation

Switch leakage in this sample and hold does not reach storage capacitor.



*polystyrene or Teflon
†required if protected-gate switch is used

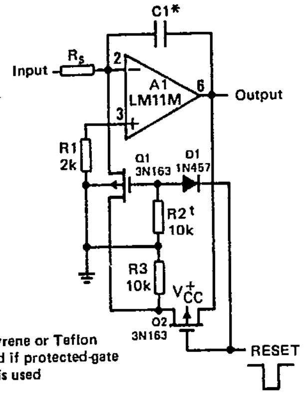
A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.



300 µs min single pulse
200 µs min repetitive pulse
300 Hz max sine wave error < 5 mV

† required if Q1 has gate-protection diode
* polystyrene or Teflon

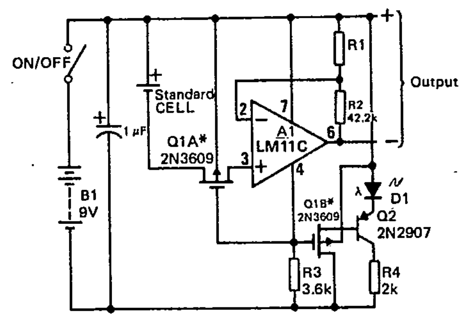
Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



* polystyrene or Teflon
† required if protected-gate switch is used

Standard-cell buffer

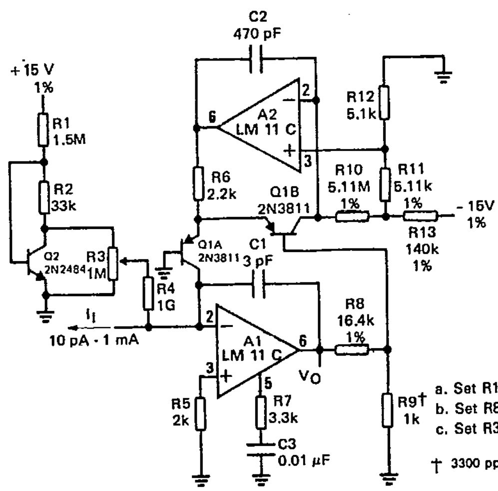
Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



*cannot have gate protection diode ; $V_{TH} > V_O$

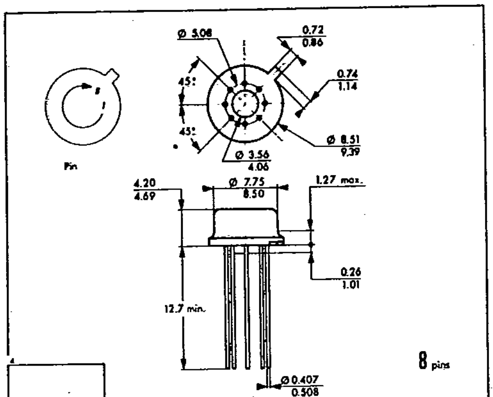
Logarithmic amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 µs time constant from 1 mA down to 100 µA, increasing from 200 µs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.

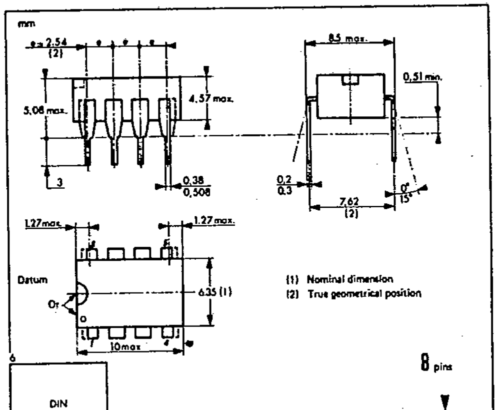


a. Set R11 for $V_O = 0$ at $I_I = 100$ nA
b. Set R8 for $V_O = +3$ V at $I_I = 100$ µA
c. Set R3 for $V_O = -4$ V at $I_I = 10$ pA

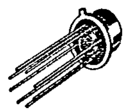
† 3300 ppM/°C.



DIN				
Case: Base: C-23 CEI	TO-99 D.A.T.A.	TO-99 JEDEC	F 101 SITELESC	CB-11 THOMSON SEMICONDUCTORS

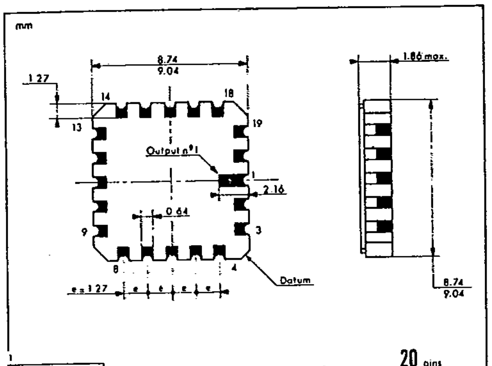


DIN				
A50D CEI	D.A.T.A.	JEDEC	F 116 A SITELESC	CB-98 THOMSON SEMICONDUCTORS

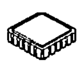


CB-11
(TO-99)
H SUFFIX
METAL CAN

CB-98
DP SUFFIX
PLASTIC PACKAGE



DIN				
MS004 CB CEI	D.A.T.A.	TMS004 CB JEDEC	SITELESC	CB-705 THOMSON SEMICONDUCTORS



CB-705
GC SUFFIX
TRICECOP (LCC)

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.