Nonvolatile DACPOT™ Electronic Potentiometer With Up/Down Counter Interface

FEATURES

- **Digitally Controlled Electronic Potentiometer**
- **7-Bit Digital-to-Analog Converter (DAC)**
  - **Independent Reference Inputs**
  - **Differential Non-Linearity - ±0.5LSB**
  - **Integral Non-Linearity - ±1LSB**
- **V_{OUT} Value in EEPROM for Power-On Recall**
  - **Equivalent to 128-Step Potentiometer**
- **Unity Gain Op Amp Drives ±100µA**
- **Simple Trimming Adjustment**
  - **Up/Down Counter Style Operation**
- **Low Noise Operation**
- **"Clickless" Transitions between DAC Steps**
- **No Mechanical Wearout Problem**
  - **1,000,000 Stores (typical)**
  - **100 Year Data Retention**
- **Operation from +2.7V to +5.5V Supply**
- **Ultra-Low Power, 0.5mW max at +5V**

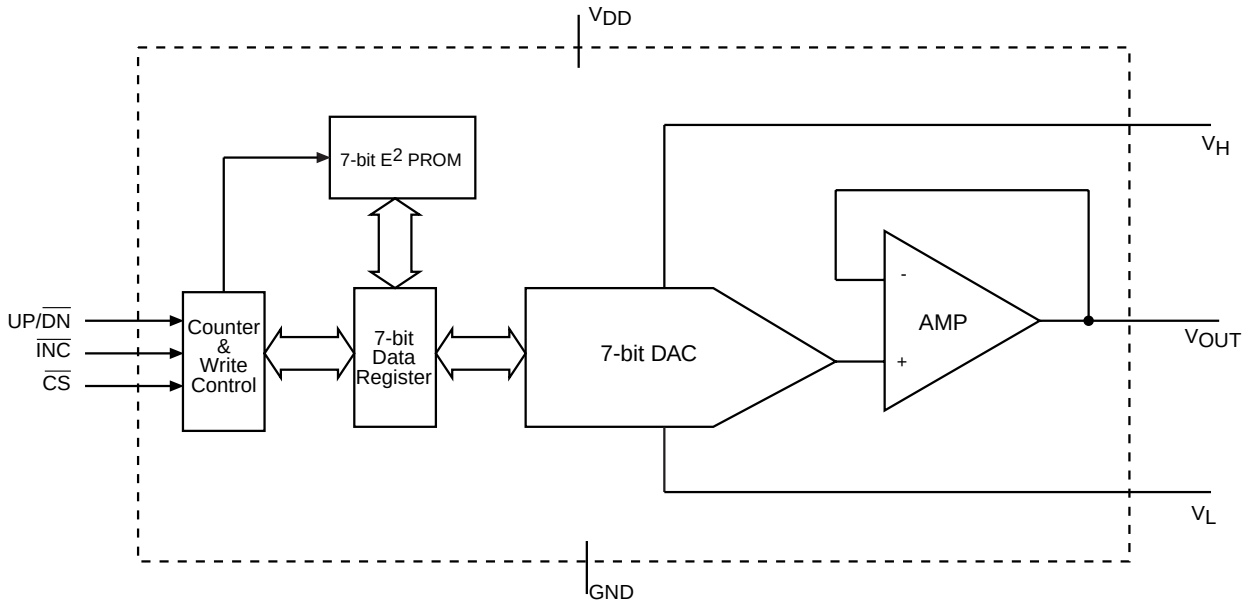
OVERVIEW

The SMP9317 DACPOT™ trimmer is a 7-bit nonvolatile DAC designed to replace mechanical potentiometers. The SMP9317 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The SMP9317's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the V_{OUT} voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The SMP9317 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The SMP9317 offers higher resolution than these devices and provides 'clickless' transitions of V_{OUT}.

FUNCTIONAL BLOCK DIAGRAM



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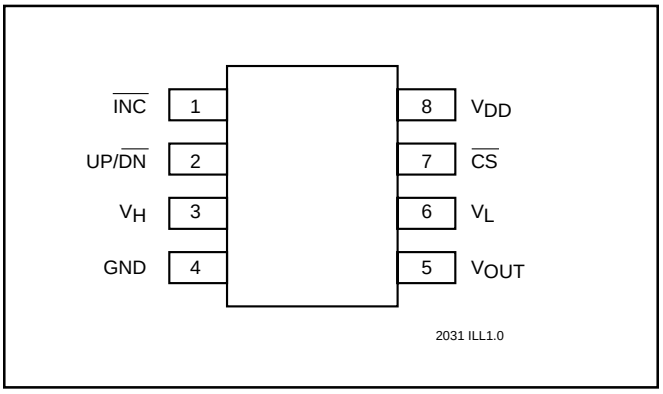
PIN NAMES

Symbol	Description
$\overline{INC}$	Increment Input, High to Low Edge Trigger
UP/$\overline{DN}$	Up/Down Input controlling relative V_{OUT} movement
V_H	V+ reference input
GND	Analog and Digital Ground
V_{OUT}	Trimmed Voltage Output
V_L	V- reference input
$\overline{CS}$	Active low chip select input
V_{DD}	Supply Voltage (2.7V to 5.5V)

PINOUT



Analog Section

The SMP9317 is a 7-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts a 7-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_L and V_H inputs sets the full-scale output voltage range. V_L must be equal to or greater than ground (i.e. a positive voltage). V_H must be greater than V_L and less than or equal to V_{DD}. See table on page 3 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is from a precision unity-gain follower that can slew up to 1V/µs.

Digital Interface

The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

Chip Select ($\overline{CS}$) is an active low input. Whenever $\overline{CS}$ is high the SMP9317 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When $\overline{CS}$ is low the SMP9317 will recognize transitions on the $\overline{INC}$ input and will move the V_{OUT} either toward the V_H reference or toward the V_L reference depending upon the state of the UP/$\overline{DN}$ input.

The host may exit an adjustment routine in two ways: deselecting the SMP9317 while $\overline{INC}$ is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the SMP9317 while $\overline{INC}$ is high will store the current V_{OUT} setting into non-volatile memory.

Increment ($\overline{INC}$) is an edge triggered input. Whenever $\overline{CS}$ is low and a high to low transition occurs on the $\overline{INC}$ input, the V_{OUT} voltage will either move toward V_H or V_L depending upon the state of the UP/$\overline{DN}$ input.

UP/Down (UP/$\overline{DN}$) is an input that will determine the V_{OUT} movement relative to V_H and V_L. When $\overline{CS}$ is low, UP/$\overline{DN}$ is high and there is a high to low transition on $\overline{INC}$, the V_{OUT} voltage will move ($1/128^{th}$ x V_H-V_L) toward V_H. When $\overline{CS}$ and UP/$\overline{DN}$ are low, and there is a high to low transition on $\overline{INC}$, the V_{OUT} will move ($1/128^{th}$ x V_H-V_L) toward V_L.

Power–Up/Power–Down Conditions

On power–up the SMP9317 loads the value of EEPROM memory into the wiper position register. The value in the register is changed using the $\overline{CS}$, $\overline{INC}$, and UP/DN pins. The new data in the register will be lost at power-down unless $\overline{CS}$ was brought high, with $\overline{INC}$ high, to initiate a store operation after the last increment or decrement. On the next device power–up, the value of EEPROM memory will be loaded into the wiper position register. During power-up the SMP9317 is write-protected in two ways:

1) A power-on reset, that trips at approximately 2.5V, holds $\overline{CS}$ and $\overline{INC}$ high internally.
2) Resistor pull-ups on all logic inputs prevent data change if the inputs are floating.

Data Retention

The SMP9317 is guaranteed to perform at least 1,000,000 writes to EEPROM before a wear–out condition can occur. After EEPROM wearout, the SMP9317 continues to function as a volatile digital-potentiometer. The wiper position can be changed during powered conditions using the digital interface. However, on power–up the wiper–position will be indeterminate.

On shipment from the factory, Summit Microelectronics does not specify any EEPROM memory value. The value must be set by the customer as needed.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to V_{DD}+.5V
Digital Inputs	-0.5V to V_{DD}+.5V
Analog Outputs	-0.5V to V_{DD}+.5V
Digital Outputs	-0.5V to V_{DD}+.5V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V_{DD}	+2.7V	+5.5V

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DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	I_{LOAD} = 50µA, T_R = C	-	0.6	±1	LSB
			T_R = I	-	0.6	±1	LSB
			I_{LOAD} = 100µA, T_R =C	-	1.2	-	LSB
			T_R = I	-	1.2	-	LSB
	DNL	Differential Non-Linearity	I_{LOAD} = 50µA, T_R = C	-	0.25	±0.5	LSB
			T_R = I	-	0.25	±0.5	LSB
			I_{LOAD} = 100µA, T_R = C	-	0.5	-	LSB
			T_R = I	-	0.5	-	LSB
References	V_H	V_{refH} Input Voltage		2.5	-	V_{DD}	V
	V_L	V_{refL} Input Voltage	$V_H \geq V_L$	Gnd	-	V_{DD}-2.5	V
	R_{IN}	V_{refH} to V_{refL} Resistance		-	38K	-	Ω
	TCR_{IN}	Temperature Coefficient of R_{IN}	V_{refH} to V_{refL}	-	700	-	ppm/°C
Analog	G_{EFS}	Full-Scale Gain Error	DATA = 7F	-	-	±1	LSB
Output	$V_{OUT}ZS$	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TCV_{OUT}	V_{OUT} Temperature Coefficient, note 3	V_{DD} = +5, I_{LOAD} = 50µA, V_{refH} = +5V, V_{refL} = 0V	-	-	200	µV/°C
	I_L	Amplifier Output Load Current				100	µA
	R_{OUT}	Amplifier Output Resistance	I_L = 100µA +5V	-	10		Ω
			+3V	-	20		Ω
	PSRR	Power Supply Rejection	I_{LOAD} = 10µA	-	-	1	LSB/V
	e_N	Amplifier Output Noise	f = 1KHz, V_{DD} = +5V	-	90	-	nV/ $\sqrt{Hz}$
	THD	Total Harmonic Distortion	V_{IN} = 1V rms, f = 1KHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V_{IN} = 100mV rms	-	1,000	-	kHz

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RELIABILITY CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2031 PGM T2.0

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_H = V_{DD}$, V_L = 0V, T_A = -40°C to +85°C, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply Current during store, note 1	CS = V_{IL} to V_{IH} W/$\overline{INC}$ HI		1.0		mA
I_{SB}	Supply Standby Current	CS = V_{IH}			100	µA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$			10	µA
I_{IL}	Input Leakage Current, note 2	V_{IN} = 0V			-25	µA
V_{IH}	High Level Input Voltage		2		V_{DD}	V
V_{IL}	Low Level Input Voltage	$V_{DD} \geq 4.5V$	0		0.8	V

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Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. $\overline{CS}$, UP/$\overline{DN}$ and $\overline{INC}$ have internal pull-up resistors of approximately 200kΩ. When the input is pulled to ground the resulting output current will be V_{DD}/200kΩ.
3. TCV_{OUT} is guaranteed but not tested.

OPERATIONAL TRUTH TABLE

$\overline{INC}$	$\overline{CS}$	UP/$\overline{DN}$	Operation
HI$_{TO}$LO	L	H	V_{OUT} toward V_H
HI$_{TO}$LO	L	L	V_{OUT} toward V_L
H	LO$_{TO}$HI	X	Store Setting
L	LO$_{TO}$HI	X	Maintain Setting, NO Store
X	H	X	Standby, note 1

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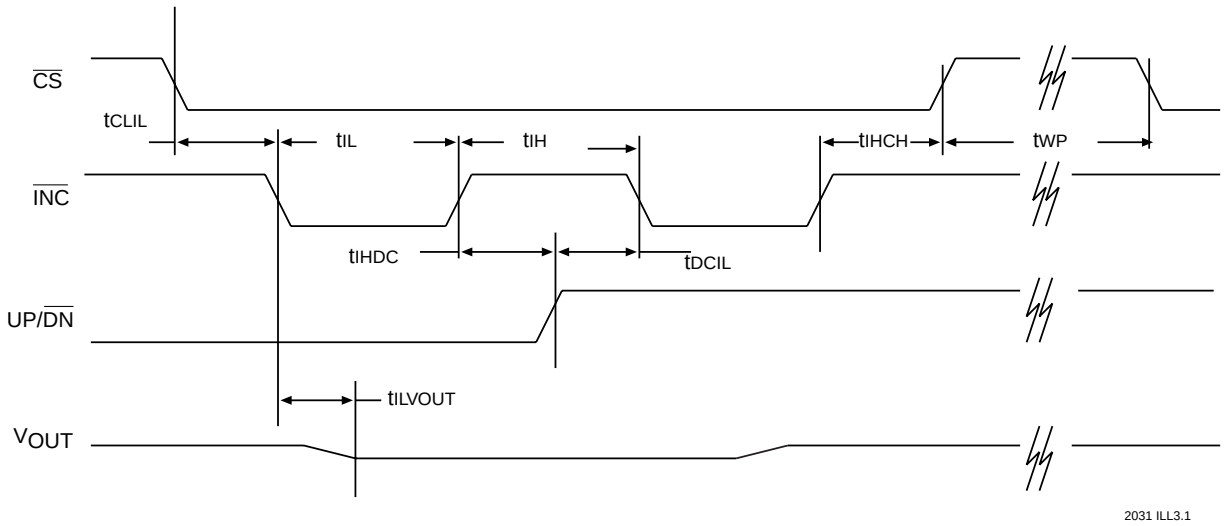
Notes: 1. The Standby or operating current will be lowest with $\overline{INC}$ and UP/$\overline{DN}$ pins at H as there are weak internal pull-ups that draw current when connected LO.

AC TIMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t_{CLIL}	$\overline{CS}$ to $\overline{INC}$ Setup	100		ns
t_{IHDC}	$\overline{INC}$ High to UP/$\overline{DN}$ Change	100		ns
t_{DCIL}	UP/$\overline{DN}$ to $\overline{INC}$ Setup	100		ns
t_{IL}	$\overline{INC}$ Low Period	200		ns
t_{IH}	$\overline{INC}$ High Period	200		ns
t_{IHCH}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	100		ns
t_{WP}	$\overline{Write}$ Cycle Time		5	ms
t_{ILVOUT}	$\overline{INC}$ to V_{OUT} Delay		5	µs

2031 PGM T6.0



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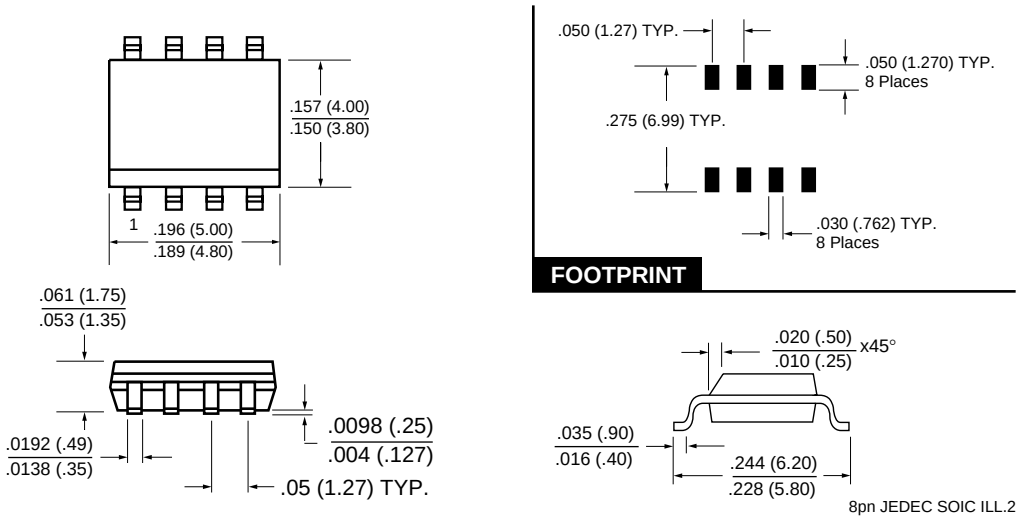
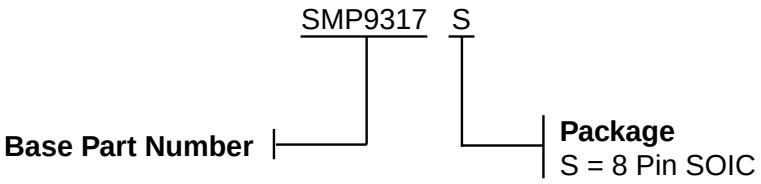
AC TIMING DIAGRAM

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8pn JEDEC SOIC ILL.2

ORDERING INFORMATION



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