SUCCESS BY DESIGN

USB2601/USB2602

4th Generation USB2.0 Flash Media Controller with Integrated Card Power FETs and HS Hub

PRODUCT FEATURES

Datasheet

Hub Controller

- Provides Three USB2.0 Downstream Ports via internal USB2.0 Hub
  - Multi Transaction Translator for FS/LS devices attached

Flash Media Controller

- Complete System Solution for interfacing SmartMedia™ (SM) or xD Picture Card™ (xD)[1], Memory Stick™ (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo™, Secure Digital (SD), Mini-Secure Digital (Mini-SD), TransFlash (SD), MultiMediaCard™ (MMC), Reduced Size MultiMediaCard (RS-MMC), NAND Flash, Compact Flash™ (CF) and CF Ultra™ I & II, and CF form-factor ATA hard drives to USB2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- Hardware support for SD Security Command Extensions
- 3.3 Volt I/O with 5V input tolerance on VBUS, Port Power and Over-Current Sense pins
- On-chip power FETs for supplying flash media card power with minimum board components
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
  - Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal Program Memory Interface
  - 64K Byte Internal Code Space
- On Board 24Mhz Crystal Driver Circuit
- Can be clocked by an external 24MHz source
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz USB2.0 Sampling, Configurable MCU clock
- 11 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
- Configuration of Hub and Flash Media features controlled either by internal defaults or via single external EEPROM. User configurable features:
  - Full or Partial Card compliance checking
  - LUN configuration and assignment
  - Write Protect Polarity
  - Cover Switch operation for xD compliance
  - Inquiry Command operation
  - SD Write Protect operation
  - Older CF card support
  - Force USB 1.1 reporting
  - Internal or External Power FET operation
- Compatible with Microsoft WinXP, WinME, Win2K SP3&4, Apple OS10 and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers are available from SMSC
- 128 Pin TQFP Package (1.0mm height, 14mm x14mm footprint); green, lead-free package also available

1.xD Picture Card not applicable to USB2601

ORDER NUMBER(S):

USB2601/USB2602-NE-XX FOR 128 PIN, TQFP PACKAGE

USB2601/USB2602-NU-XX FOR 128 PIN, TQFP PACKAGE (GREEN, LEAD-FREE)

80 Arkay Drive
Hauppauge, NY 11788
(631) 435-6000
FAX (631) 273-3123

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Chapter 1 General Description

The USB2601/USB2602 is an Integrated “combo” High-Speed USB hub and Flash Media Controller. The Flash media controller permanently resides on Port 1 of the Integrated USB hub.

1.1 High-Speed Hub

The integrated SMSC Hub is fully compliant with the USB2.0 Specification and will attach to a USB host as a Full-Speed Hub or as a Full-/High-Speed Hub. The Hub supports Low-Speed, Full-Speed, and High-Speed (if operating as a High-Speed Hub) downstream devices on all of the enabled downstream ports.

A dedicated Transaction Translator (TT) is available for each downstream facing port. This architecture ensures maximum USB throughput for each connected device when operating with mixed-speed peripherals.

The Hub works with an external USB power distribution switch device to control V_{BUS} switching to downstream ports, and to limit current and sense over-current conditions.

All required resistors on the USB ports are integrated into the Hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Throughout this document the upstream facing port of the hub will be referred to as the upstream port, and the downstream facing ports will be called the downstream ports.

Three externally available ports are available for general USB device connectivity.

1.2 Flash Media Controller

The Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and XD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. SM controller supports both SM and xD cards.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Eleven GPIO pins are provided for indicators, external serial EEPROM for OEM ID and system configuration information, and other special functions.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPro cards.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. SMSC also provides licenses** for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

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Chapter 2 Acronyms

SM: SmartMedia

SMC: SmartMedia Controller

FM: Flash Media

FMC: Flash Media Controller

CF: Compact Flash

CFC: CompactFlash Controller

SD: Secure Digital

SDC: Secure Digital Controller

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

TPC: Transport Protocol Code.

ECC: Error Checking and Correcting

CRC: Cyclic Redundancy Checking

Chapter 3 Pin Table

3.1 128-Pin Package

Table 3.1 USB2601/USB2602 128-Pin Package

UPSTREAM USB2.0 INTERFACE (3 PINS)			
USBUP_DP	USBUP_DM	VBUS_DET	
3-PORT USB2.0 INTERFACE (16 PINS)			
USBDN_DP2	USBDN_DM2	USBDN_DP3	USBDN_DM3
USBDN_DP4	USBDN_DM4	PRTPWR2	PRTPWR3
PRTPWR4	OCS2_N	OCS3_N	OCS4_N
GR2_N	GR3_N	GR4_N	PRTPWR_POL
CompactFlashINTERFACE (28 Pins)			
CF_D0	CF_D1	CF_D2	CF_D3
CF_D4	CF_D5	CF_D6	CF_D7
CF_D8	CF_D9	CF_D10	CF_D11
CF_D12	CF_D13	CF_D14	CF_D15
CF_nIOR	CF_nIOW	CF_IRQ	CF_nRESET
CF_IORDY	CF_nCS0	CF_nCS1	CF_SA0
CF_SA1	CF_SA2	CF_nCD1	CF_nCD2
SmartMedia INTERFACE (17 Pins)			
SM_D0	SM_D1	SM_D2	SM_D3
SM_D4	SM_D5	SM_D6	SM_D7
SM_ALE	SM_CLE	SM_nRE	SM_nWE
SM_nWP	SM_nB/R	SM_nCE	SM_nCD
SM_nWPS			
Memory Stick INTERFACE (7 Pins)			
MS_BS	MS_SDIO/MS_D0	MS_SCLK	MS_INS
MS_D1	MS_D2	MS_D3	
SD INTERFACE (7 Pins)			
SD_CMD	SD_CLK	SD_DAT0	SD_DAT1
SD_DAT2	SD_DAT3	SD_nWP	

Table 3.1 USB2601/USB2602 128-Pin Package (continued)

MISC (23 Pins)			
GPIO1	GPIO2	GPIO4	GPIO5
GPIO6	GPIO7	GPIO8/CRD_PWR0	GPIO9
GPIO10/CRD_PWR1	GPIO11/CRD_PWR2	GPIO12	GPIO13
GPIO14	GPIO15	TEST	RESET_N
ATEST	RBIAS	XTAL1/CLKIN	XTAL2
CLK_SEL0	CLK_SEL1	SEL_CLKDRV	
ANALOG POWER (5 Pins)			
(3)VDDA33	VDD33PLL	VDD18PLL	
DIGITAL, POWER & GROUND (22 Pins)			
(5)VDD33	(11)VSS	(3)VDD18	(3)NC
Total 128			

3.2 128-Pin List Table

Table 3.2 USB2601/USB2602 128-Pin TQFP

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
1	PRTPWR_POL	-	33	VDD18	-	65	CF_D7	8	97	SD_nWP	-
2	PRTPWR2	12	34	VSS	-	66	CF_D15	8	98	SD_DAT1	8
3	OCS2_N	-	35	VSS	-	67	CF_nCS0	8	99	SD_DAT0	8
4	PRTPWR3	12	36	SM_nWPS	-	68	CF_nCS1	8	100	SD_CLK	8
5	OCS3_N	-	37	SM_CLE	8	69	CF_nIOR	8	101	VDD33	-
6	PRTPWR4	12	38	SM_nCE	8	70	CF_nIOW	8	102	GPIO11/ CRD_PWR2	-
7	OCS4_N	-	39	SM_ALE	8	71	CF_IRQ	8	103	SD_CMD	8
8	VDDA33	-	40	SM_nRE	8	72	CF_nRESET	8	104	SD_DAT3	8
9	USBDN_DP3	--	41	SM_nWE	8	73	CF_IORDY	8	105	SD_DAT2	8
10	USBDN_DM3	-	42	SM_nB/R	-	74	CF_SA2	8	106	GPIO4	8
11	VSS	-	43	VDD33	-	75	CF_SA1	8	107	GPIO5	8
12	USBDN_DM4	-	44	GPIO10/ CRD_PWR1	-	76	CF_SA0	8	108	VSS	-

Table 3.2 USB2601/USB2602 128-Pin TQFP (continued)

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
13	USBDN_DP4	-	45	SM_nWP	8	77	CF_D0	8	109	VSS	-
14	VDDA33	-	46	SM_D0	8	78	CF_D1	8	110	USBUP_DM	-
15	VDD33	-	47	SM_D1	8	79	CF_D8	8	111	USBUP_DP	-
16	GR2_N	8	48	SM_D7	8	80	CF_D2	8	112	VDDA33	-
17	GR3_N	8	49	SM_D2	8	81	CF_D9	8	113	USBDN_DP2	-
18	GR4_N	8	50	SM_D6	8	82	CF_D10	8	114	USBDN_DM2	-
19	GPIO6	8	51	SM_D3	8	83	CF_nCD2	-	115	VSS	-
20	MS_BS	8	52	SM_D5	8	84	VSS	-	116	VBUS_DET	12
21	MS_D1	8	53	SM_D4	8	85	VSS	-	117	VSS	-
22	MS_SDIO/MS_D0	8	54	SM_nCD	-	86	VDD18	-	118	RESET_N	-
23	MS_D2	8	55	GPIO9	8	87	VDD33	-	119	VDD18	-
24	MS_INS	-	56	CF_nCD1	-	88	GPIO1	8	120	TEST	-
25	MS_D3	8	57	CF_D3	8	89	GPIO2	8	121	VSS	-
26	MS_SCLK	8	58	CF_D11	8	90	GPIO7	8	122	XTAL2	-
27	SEL_CLKDRV	-	59	CF_D4	8	91	VDD33	-	123	XTAL1/CLKIN	-
28	CLK_SEL1	-	60	CF_D12	8	92	GPIO8/CRD_PWR0	-	124	VDD18PLL	-
29	CLK_SEL0	-	61	CF_D5	8	93	GPIO12	8	125	VDD33PLL	-
30	NC	-	62	CF_D13	8	94	GPIO13	8	126	ATEST	-
31	NC	-	63	CF_D6	8	95	GPIO14	8	127	RBIAS	-
32	NC	-	64	CF_D14	8	96	GPIO15	8	128	VSS	-

Notes:

- RBIAS is connected to the Analog Ground plane VSS via a resistor.
- When the internal 1.8V regulators are enabled, VDD18 (Pin 86) & VDD18PLL (Pin 124), MUST have a 10uf +/- 20%, (equivalent series resistance (ESR) <0.1ohm) bypass capacitor to VSS. These capacitors must be as close to the pins as possible.

Chapter 4 Pin Configuration

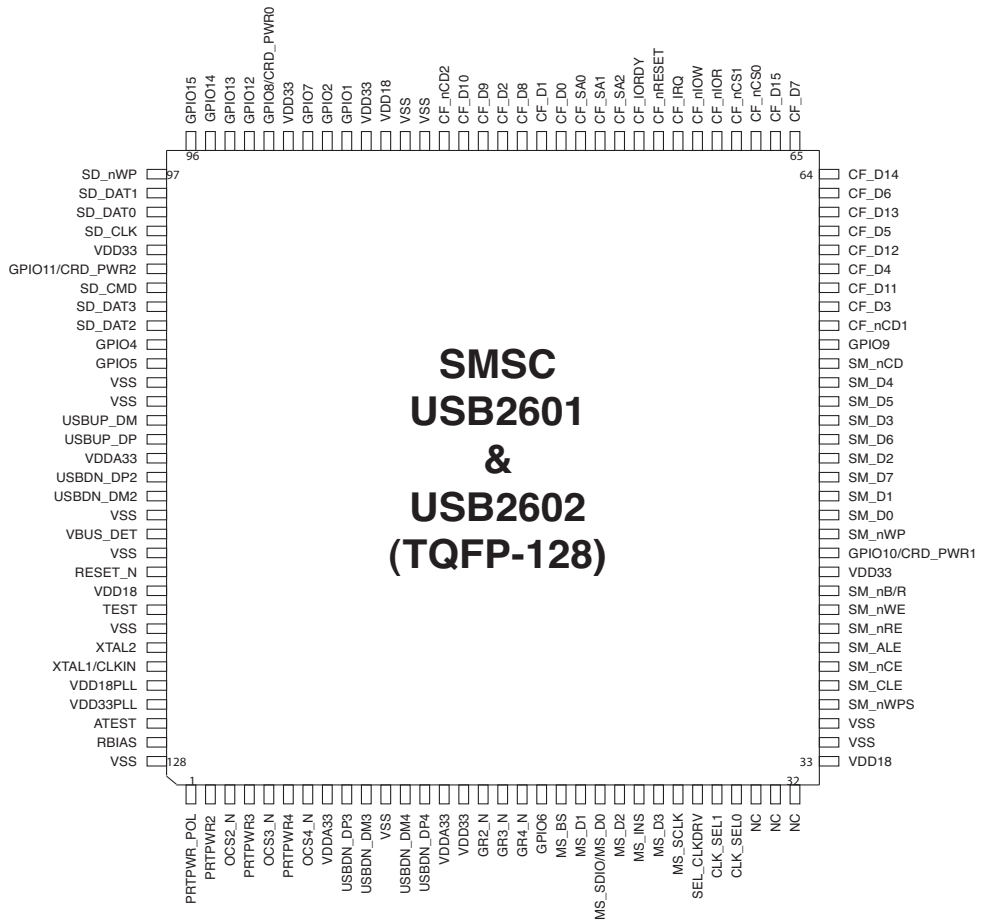

Figure 4.1 USB2601/USB2602 128-Pin TQFP

Chapter 5 Block Diagram

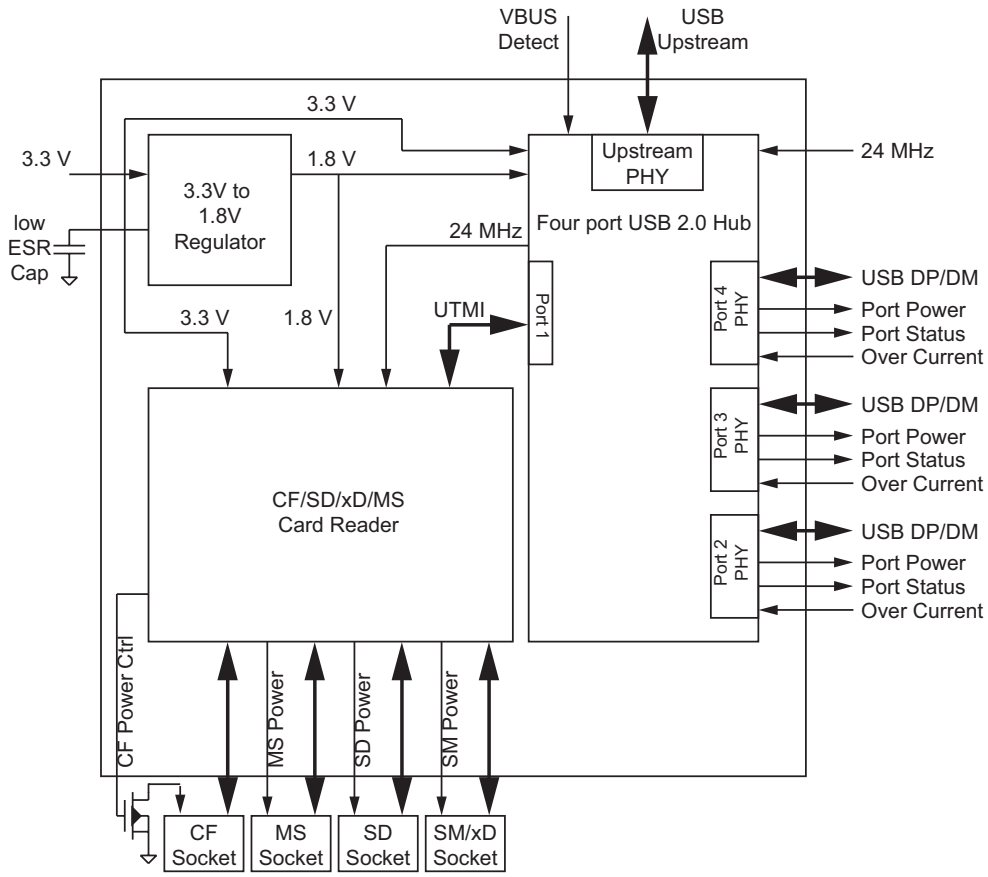

Figure 5.1 USB2601/USB2602 Block Diagram

Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” or “_N”symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name (or “_N” after the signal name), the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

6.1 PIN Descriptions

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
UPSTREAM USB INTERFACE			
USB Bus Data	USBUP_DM USBUP_DP	IO-U	These pins connect to the Upstream USB bus data signals.
Detect Upstream VBUS Power	VBUS_DET	I/O12	Detects state of Upstream VBUS power. The SMSC Hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signalling a connect event). When designing a detachable hub, this pin must be connected to the VBUS power pin of the USB port that is upstream of the hub. For self-powered applications with a permanently attached host, this pin must be pulled-up to either 3.3V or 5.0V (typically VDD33).
3-PORT USB INTERFACE			
USB Bus Data	USBDN_DM [4:2} USBDN_DP [4:2}	IO-U	These pins connect to the Downstream USB bus data signals.
USB Power Enable	PRTPWR[4:2]	I/O12	Enables power to USB peripheral devices (downstream). The active signal level of the PRTPWR[4:2] pins is determined by the Power Polarity Strapping function of the PRTPWR_POL pin.
Port Power Polarity Strapping	PRTPWR_POL	I/O12	Port Power Polarity strapping determination for the active signal polarity of the PRTPWR[4:2] pins. While RESET_N is asserted, the logic state of this pin will (though the use of internal combinatorial logic) determine the active state of the PRTPWR[4:2] pins in order to ensure that downstream port power is not inadvertently enabled to inactive ports during a hardware reset. ‘1’ = PRTPWR[4:2] pins have an active ‘high’ polarity ‘0’ = PRTPWR[4:2] pins have an active ‘low’ polarity

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Over Current Sense	OCS[4:2]_N	IPU	Input from external current monitor indicating an over-current condition. {Note: Contains internal pull-up to 3.3V supply}
Green LED	GR[4:2]_N	I/O8	Green indicator LED for ports 2, 3 and 4. Will be active low when LED support is enabled via EEPROM or SMBus.
CompactFlash (In True IDE mode) INTERFACE			
CF Chip Select 1	CF_nCS1	O8PU	This pin is the active low chip select 1 signal for the CF ATA device
CF Chip Select 0	CF_nCS0	O8PU	This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF Register Address 2	CF_SA2	O8	This pin is the register select address bit 2 for the CF ATA device.
CF Register Address 1	CF_SA1	O8	This pin is the register select address bit 1 for the CF ATA device
CF Register Address 0	CF_SA0	O8	This pin is the register select address bit 0 for the CF ATA device.
CF Interrupt	CF_IRQ	IPD	This is the active high interrupt request signal from the CF device.
CF Data 15-8	CF_D[15:8]	I/O8PD	The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
CF Data7-0	CF_D[7:0]	I/O8PD	The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
IO Ready	CF_IORDY	IPU	This pin is active high input signal. This pin has an internally controlled weak pull-up resistor.
CF Card Detection2	CF_nCD2	IPU	This card detection pin is connected to the ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF Card Detection1	CF_nCD1	IPU	This card detection pin is connected to ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF Hardware Reset	CF_nRESET	O8	This pin is an active low hardware reset signal to CF device.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
CF IO Read	CF_nIOR	O8	This pin is an active low read strobe signal for CF device.
CF IO Write Strobe	CF_nIOW	O8	This pin is an active low write strobe signal for CF device.
SmartMedia INTERFACE			
SM Write Protect	SM_nWP	O8PD	This pin is an active low write protect signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled
SM Address Strobe	SM_ALE	O8PD	This pin is an active high Address Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled
SM Command Strobe	SM_CLE	O8PD	This pin is an active high Command Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled
SM Data7-0	SM_D[7:0]	I/O8PD	These pins are the bi-directional data signal SM_D7-SM_D0. The bi-directional data signal has an internal weak pull-down resistor.
SM Read Enable	SM_nRE	08PU	This pin is an active low read strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM Write Enable	SM_nWE	O8PU	This pin is an active low write strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM Write Protect Switch	SM_nWPS	IPU	A write-protect seal is detected, when this pin is low. This pin has an internally controlled weak pull-up resistor.
SM Busy or Data Ready	SM_nB/R	I	This pin is connected to the BSY/RDY pin of the SM device. An external pull-up resistor is required on this signal. The pull-up resistor must be pulled up to the same power source that powers the SM/NAND flash device.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
SM Chip Enable	SM_nCE	O8PU	This pin is the active low chip enable signal to the SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM Card Detection	SM_nCD	IPU	This is the card detection signal from SM device to indicate if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MEMORY STICK INTERFACE			
MS Bus State	MS_BS	O8	This pin is connected to the BS pin of the MS device. It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS System Data In/Out	MS_SDIO/MS_D0	I/O8PD	This pin is a bi-directional data signal for the MS device. Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS System Data In/Out	MS_D1	I/O8PD	This pin is a bi-directional data signal for the MS device. This pin has internally controlled weak pull-up and pull-down resistors for various operational modes.
MS System Data In/Out	MS_D[3:2]	I/O8PD	This pin is a bi-directional data signal for the MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS Card Insertion	MS_INS	IPU	This pin is the card detection signal from the MS device to indicate, if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MS System CLK	MS_SCLK	O8	This pin is an output clock signal to the MS device. The clock frequency is software configurable.
SD INTERFACE			
SD Data3-0	SD_DAT[3:0]	I/O8PU	These are bi-directional data signals. These pins have internally controlled weak pull-up resistors.
SD Clock	SD_CLK	O8	This is an output clock signal to SD/MMC device. The clock frequency is software configurable.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
SD Command	SD_CMD	I/O8PU	This is a bi-directional signal that connects to the CMD signal of SD/MMC device. This pin has an internally controlled weak pull-up resistor.
SD Write Protected	SD_nWP	IPD	This pin is an input signal with an internal weak pull-down. This pin has an internally controlled weak pull-down resistor.
MISC			
General Purpose I/O	GPIO1	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO2	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO4	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO5	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO6	GPIO6	IPU	This pin has an internal weak pull-up resistor that is enabled or disabled by the state of RESET_N. The pull-up is enabled when RESET_N is active. The pull-up is disabled, when the RESET_N is inactive (some clock cycles later, after the rising edge of RESET_N). The state of this pin is latched internally on the rising edge of RESET_N to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register.
		I/O8	After the rising edge of RESET_N, this pin may be used as GPIO6. When this pin is left unconnected or pulled high by a weak pull-up resistor, the USB2601/USB2602 uses the internal ROM for program execution. This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO7	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O Or Card Power	GPIO8/ CRD_PWR0	I/O8	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
General Purpose I/O	GPIO9	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O Or Card Power	GPIO10/ CRD_PWR1	I/O8	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
General Purpose I/O Or Card Power	GPIO11/ CRD_PWR2	I/O8	GPIO: These pins may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 200mA.
General Purpose I/O	GPIO[15:12]	I/O8	These pins may be used either as input, or output.
RESET input	RESET_N	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1µs wide.
TEST Input	TEST	IPD	Used for testing the IC. User must treat either as a no-connect, or connect to the ground.
USB Transceiver Bias	RBIAS	I	A 12.0kΩ, ± 1.0% resistor is attached from VSS to this pin, in order to set the transceiver's internal bias currents.
Analog Test	ATEST	AIO	This signal is used for testing the analog section of the chip and should be connected to VDDA33 for normal operation.
Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	24Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 24Mhz clock when a crystal is not used. **Note:** The 'SEL_CLKDRV and CLK_SEL[1:0]' pins will be sampled while RESET_N is asserted, and the value will be latched upon RESET_N negation. This will determine the clock source and value.
Crystal Output	XTAL2	OCLKx	24Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
Select Clock Drive	SEL_CLKDRV	I/O8PD	SEL_CLKDRV. During RESET_N assertion, this pin will select the operating clock mode (crystal or externally driven clock source), and a weak pull-down resistor is enabled. When RESET_N is negated, the value will be internally latched and the internal pull-down will be disabled. '0' = Crystal operation (24MHz) '1' = Externally driven clock source (24MHz)
Clock Select	CLK_SEL[1:0]	I/O8PD	SEL[1:0]. During RESET_N assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When RESET_N is negated, the value on these pins will be internal latched and the internal pull-downs will be disabled. SEL[1:0] = '00'. 24MHz SEL[1:0] = '01'. RESERVED SEL[1:0] = '10'. RESERVED SEL[1:0] = '11'. RESERVED
ANALOG POWER			
1.8V PLL Power	VDD18PLL		1.8v Output from the internal 1.8V PLL regulator
3.3V PLL Power	VDD33PLL		3.3V Input to the internal 1.8V PLL regulator.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
3.3V Analog Power	VDDA33		3.3v Analog PHY Power
DIGITAL POWER, GROUNDS, and NO CONNECTS			
1.8v Digital Core Power	VDD18		+1.8V Core power All VDD18 pins must be connected together on the circuit board.
3.3v Power & & Voltage Regulator Input	VDD33		3.3V Power & Regulator Input. pin 87 supplies 3.3V power to the internal 1.8V VDD18 regulator.
Ground	VSS		Ground Reference
No Connect	NC		No Connect. No trace or signal should be routed/attached to these pins.

Notes:

- Hot-insertion capable card connectors are required for all flash media. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.
- nMCE is normally asserted except when the 8051 is in standby mode.

6.2 Buffer Type Descriptions

Table 6.1 USB2601/USB2602 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O8	Input/Output buffer with 8mA sink and 8mA source.
I/O8PU	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
I/O8PD	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
I/O12	Input/Output, 12mA
O8	Output buffer with 8mA sink and 8mA source.
O8PU	Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
O8PD	Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog Input/Output Defined in USB specification
AIO	Analog Input/Output

Chapter 7 DC Parameters

7.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$

Storage Temperature Range ..... -55^o to $+150^oC$

Lead Temperature Range (soldering, 10 seconds) ..... $+325^oC$

Positive Voltage on GPIO3, with respect to Ground 5.5V

Positive Voltage on any signal pin, with respect to Ground 4.6V

Positive Voltage on XTAL1, with respect to Ground 4.0V

Positive Voltage on XTAL2, with respect to Ground 2.5V

Negative Voltage on GPIO8, 10 & 11, with respect to Ground (see Note 7.2) ..... -0.5V

Negative Voltage on any pin, with respect to Ground ..... -0.5V

Maximum V_{DD18}, $V_{DD18PLL}$ ..... +2.5V

Maximum V_{DD33}, V_{DDA33} ..... +4.6V

*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 7.1 When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

Note 7.2 When internal power FET operation of these pins is enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63V and T_A is less than 70°C.

7.2 DC Electrical Characteristics

(T_A = 0°C - 70°C, V_{DD33}, V_{DDA33} = *+3.3 V* ± 0.3 V, V_{DD18}, $V_{DD18PLL}$ = *+1.8 V* ± 10%,)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I,IPU & IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		500		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	mA	V_{IN} = V_{DD33}
O8. O8PU & 08PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -8mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.3)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
I/O8, I/O8PU & I/O8PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} -0.4			V	I_{OH} = -8 mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.3)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA @ V_{DD33} = 3.3V
Output Leakage	I_{OL}			+10	uA	V_{IN} = 0 to V_{DD33} (Note 1)
IO-U (Note 7.4)						
Integrated Power FET for GPIO8 & GPIO10						
Output Current	I_{OUT}	100			mA	GPIO8, or 10; $Vdrop_{FET}$ = 0.23V
Short Circuit Current Limit	I_{SC}			140	mA	GPIO8, or 10; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	GPIO8, or 10; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	GPIO8, or 10; C_{LOAD} = 10µF
Integrated Power FET for GPIO11						
Output Current	I_{OUT}	200			mA	GPIO11; $Vdrop_{FET}$ = 0.46V
Short Circuit Current Limit	I_{SC}			181	mA	GPIO11; $Vout_{FET}$ = 0V
On Resistance	R_{DSON}			2.1	Ω	GPIO11; I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	GPIO11; C_{LOAD} = 10µF
Supply Current Hub, Card Reader, Unconfigured						
High-Speed Host Full-Speed Host	I_{CCINIT} I_{CCINIT}		90 83		mA mA	
Supply Current Configured (High-Speed Host)						Total from all supplies
3 Ext Ports @HS Card Reader Active			302		mA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Supply Current Configured (High-Speed Host) 1 Ext Port @HS Card Reader Active			242		mA	Total from all supplies
Supply Current Configured (Full-Speed Host) 1 Ext Port @ FS/LS Card Reader Active			200		mA	Total from all supplies
Supply Current Suspend	I_{CSBY}		298		µA	Total from all supplies.
Supply Current Reset	I_{RST}		91		µA	Total from all supplies.

Note 7.3 Output leakage is measured with the current pins in high impedance.

Note 7.4 See Appendix A for USB DC electrical characteristics.

Note 7.5 The Maximum power dissipation parameters of the package should not be exceeded

Note 7.6 The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to the settings listed in Table 9.1, “GPIO Usage (ROM Rev -01),” on page 26

7.3 Capacitance

T_A = 25°C; fc = 1MHz; V_{DD18}, $V_{DD18PLL}$ ***= 1.8V***

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 8 Package Outline

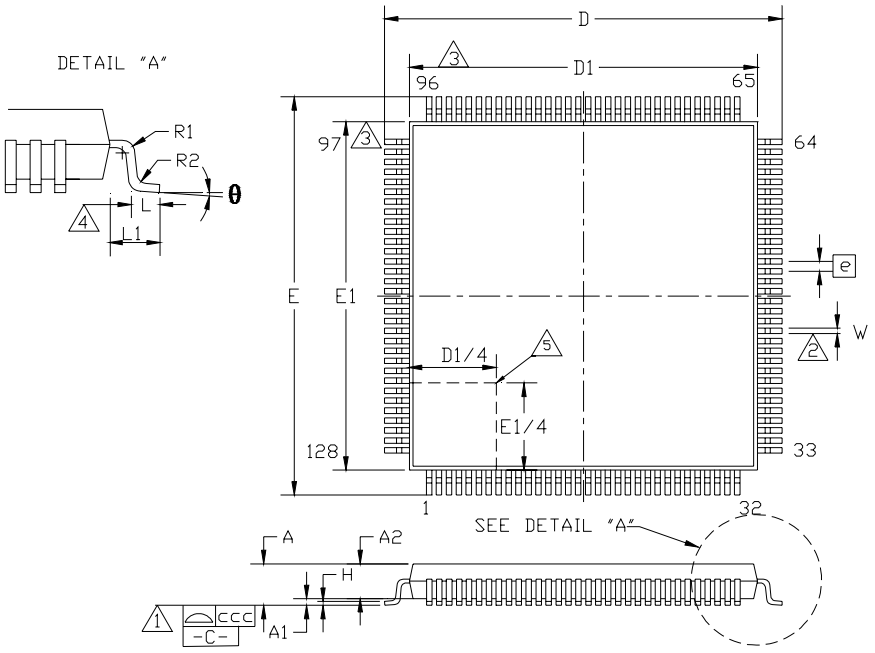

Figure 8.1 USB2601/USB2602 128-Pin TQFP Package Outline

Table 8.1 USB2601/USB2602 128-Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.035 mm maximum.
   Package body dimensions D1 and E1 do not include the mold protrusion.
3. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 9 GPIO Usage

Table 9.1 GPIO Usage (ROM Rev -01)

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	Flash Media Activity LED/ xD_Door	Indicates media activity. Media or USB cable must not be removed with LED lit. Also may be used for xD Door functionality
GPIO2	H	EE_CS	Serial EE PROM chip select
GPIO3	H	V_BUS	USB V bus detect
GPIO4	H	EE_DIN/EE_DOUT/xDID	Serial EE PROM input/output and xD Identify
GPIO5	H	HS_IND/SD_CD	HS Indicator LED or SD Card Detect Switch input
GPIO6	H	A16/ROMEN	A16 address line connect for DFU or debug LED indicator optional.
GPIO7	H	EE_CLK/ UNCONF_LED	Serial EE PROM clock output or Unconfigured LED.
GPIO8	L	MS_PWR_CTRL/ CRD_PWR0	Memory Stick Card Power Control, or Internal Power FET0.
GPIO9	L	CF_PWR_CTRL	CompactFlash Card Power Control
GPIO10	L	SM_PWR_CTRL/ CRD_PWR1	SmartMedia Card Power Control, or Internal Power FET1.
GPIO11	L	SD/MMC_PWR_CTRL/ CRD_PWR2	SD/MMC Card Power Control, or Internal Power FET2.
GPIO12	H	MS_ACT_IND/ Media Activity	Memory Stick Activity Indicator, or Media Activity LED.
GPIO13	H	CF_ACT_IND	CompactFlash Activity Indicator
GPIO14	H	SM_ACT_IND	SmartMedia Activity Indicator
GPIO15	H	SD/MMC_ACT_IND	SD/MMC Activity Indicator