USB2250/51/59

Ultra Fast USB 2.0 Multi-Format Flash Media Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB2250/51/59 is a USB 2.0 compliant, high speed Mass Storage Class Peripheral Controller intended for reading and writing to more than 24 popular flash media formats from the CompactFlash® (CF), SmartMedia™ (SM), xD Picture Card™ (xD)[1], Memory Stick™ (MS), Secure Digital (SD), and MultiMediaCard™ (MMC) families.

The SMSC USB2250/51/59 is a fully integrated, single chip solution capable of ultra high performance operation. Average sustained transfer rates exceeding 35MB/s are possible if the media and host can support those rates.

General Features

- 128-pin VTQFP lead-free RoHS compliant package
- Targeted for applications in which single or "combo" media sockets are used. Supports multiple simultaneous card insertions
- Flexible assignment of number of LUNs and how card types are associated with the LUNs
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media

Hardware Features

- Single Chip Flash Media Controller with non-multiplexed interface for independent card sockets
- Flash Media Specification Revision Compliance
  - Compact Flash Specification 4.1
    - CF UDMA Modes 0-4
    - CF PIO Modes 0-6
  - Memory Stick Specification 1.43
  - Memory Stick Pro Format Specification 1.02
  - Memory Stick Pro-HG Duo Format Specification 1.01
    - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
  - xD Picture Card 1.2
  - Smart Media Specification 1.3
  - Secure Digital 2.0
    - HS-SD, HC-SD, TransFlash™ and reduced form factor media
  - MultiMediaCard Specification 4.2
    - 1/4/8 bit MMC
- SDIO and MMC Streaming Mode support
- Extended configuration options
  - xD player mode operation
  - Socket switch polarities, etc.
- Media Activity LED
- GPIO configuration and polarity
  - Up to 11 GPIOs (based on configuration) for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Four GPIO's with up to 200 mA drive.
  - An additional 16 GPIO's if CF is not used.
- On Board 24MHz Crystal Driver Circuit
- Optional external 24MHz clock input
- 4 Independent Internal Card Power FETs
  - 200mA each
  - "Fold-back" short circuit current protected
- 8051 8-bit microprocessor
  - 60MHz - single cycle execution
  - 64KB ROM[2]; 14KB RAM
- Internal Regulator for 1.8V core operation
- Optimized pinout improves signal routing, easing implementation and allowing for improved signal integrity.

OEM Selectable Features

- VID/PID/Language ID
- 28-character Manufacturer ID and Product string
- 12-hex digit (max) Serial Number string
- Customizable Vendor specific data by optional use of external serial EEPROM
- Bus- or Self-powered selection
- LED blink interval or duration
- Internal power FET configuration

Software Features

- Optimized for low latency interrupt handling
- Reduced memory footprint
- Device Firmware Upgrade (DFU) support of external EEPROM or External Flash
  - Assembly line support
  - End user field upgrade support
  - DFU Package consists of driver, firmware, sample DFU application and source code, DFU driver API
- Optional (Mandatory on the USB2259) custom firmware with external ROM (up to 128k)
- Please see the USB2250/USB2251 Software Release Notes for additional Software Features

Applications

- Flash Media Card Reader/Writer
- Printers
- Desktop and Mobile PCs
- Consumer A/V
- Media Players/Viewers
- Vista ReadyBoost™

1.) xD Picture Card not applicable to USB2251

2.USB2259 uses external ROM only, internal ROM unavailable

ORDER NUMBER:

USB2250/51/59-NU-XX for 128 pin, VTQFP Lead-Free RoHS Compliant Package

Note: "XX" does not apply to the USB2259 because there is no ROM.

"XX" in the order number indicates the internal ROM firmware revision level. Please contact your SMSC sales representative for more information.

Table 0.1 USB2250/51/59 Comparison of Features

	ROM	CompactFlash® Memory Stick™ MultiMediaCard™ Secure Digital SmartMedia™	xD Picture Card™
USB2250	▪	▪	▪
USB2251	▪	▪	
USB2259	External Only	▪	▪

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Table of Contents

List of Figures

List of Tables

Chapter 1 Acronyms

SM: SmartMedia

SMC: SmartMedia Controller

CF: Compact Flash

CFC: CompactFlash Controller

SD: Secure Digital

SDC: Secure Digital Controller

MMC: MultiMediaCard

MS: Memory Stick

MSC: Memory Stick Controller

xD: xD Picture Card

Chapter 2 Block Diagram

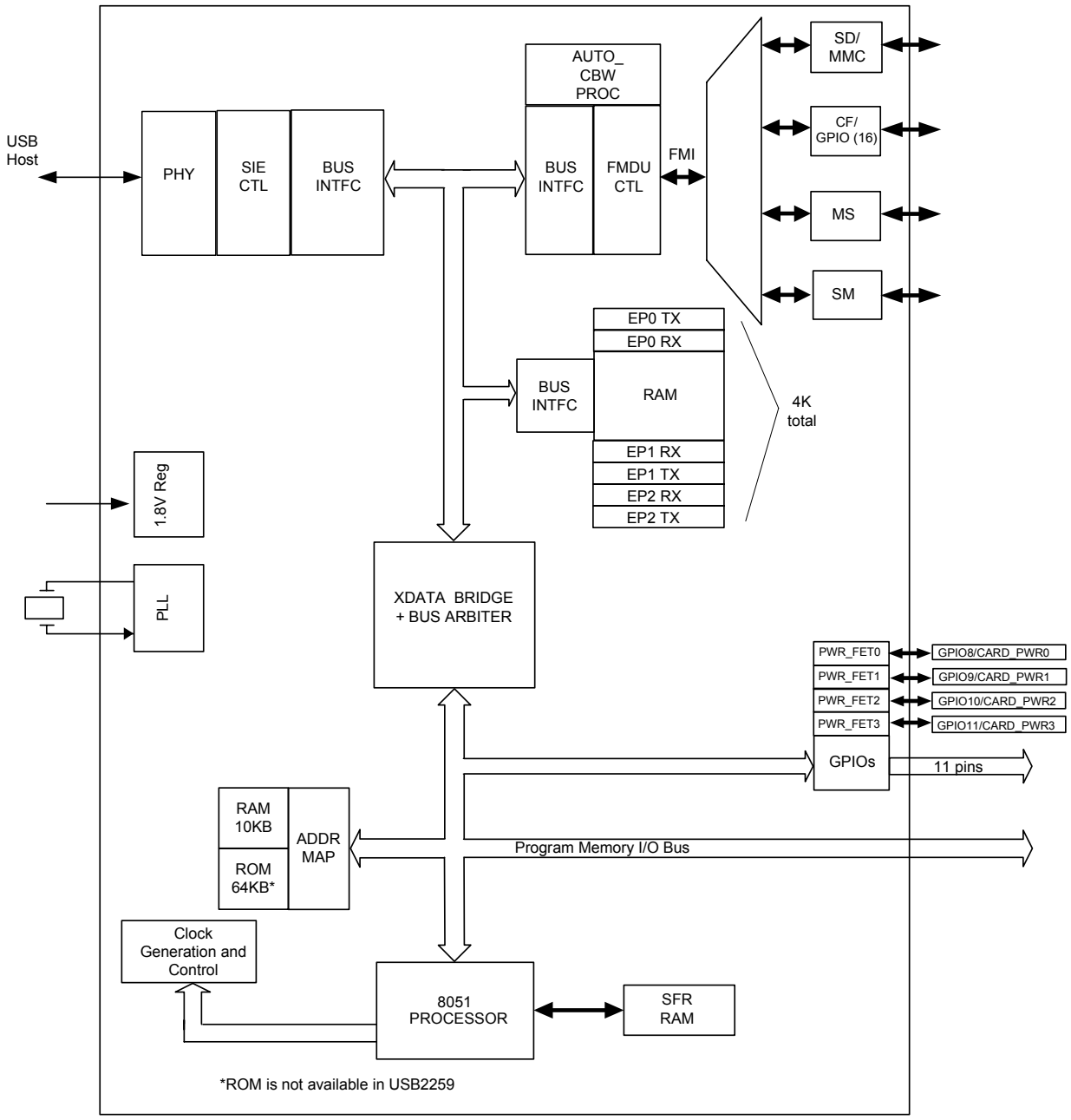

Figure 2.1 USB2250/2251 Block Diagram

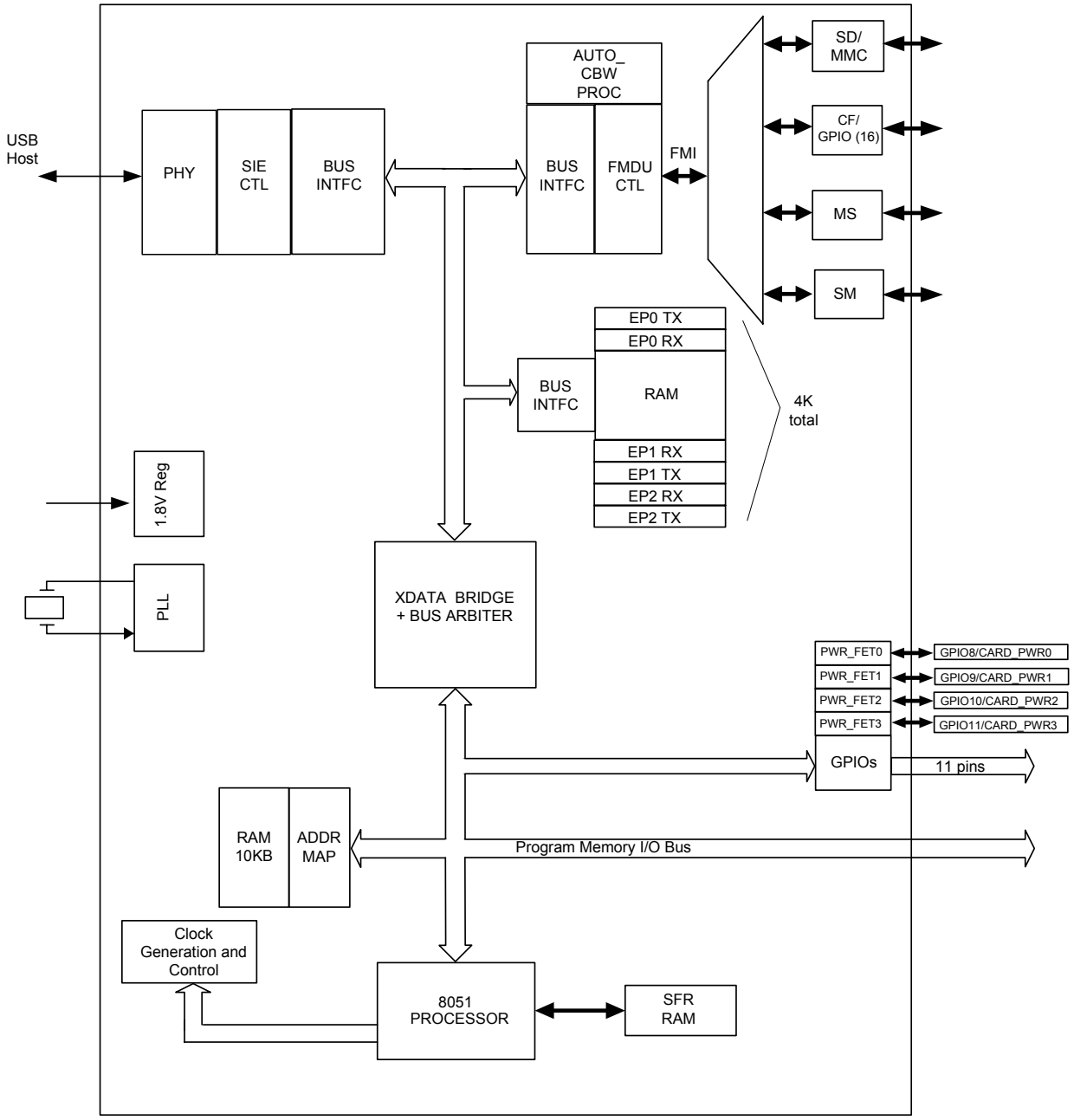

Figure 2.2 USB2259 Block Diagram

Chapter 3 Pin Table

3.1 128-Pin Package

Table 3.1 USB2250/51/59 128-Pin VTQFP Package

COMPACTFLASH INTERFACE (28 PINS)			
CF_D0/GPIO16	CF_D1/GPIO17	CF_D2/GPIO18	CF_D3/GPIO19
CF_D4/GPIO20	CF_D5/GPIO21	CF_D6/GPIO22	CF_D7/GPIO23
CF_D8/GPIO24	CF_D9/GPIO25	CF_D10/GPIO26	CF_D11/GPIO27
CF_D12/GPIO28	CF_D13/GPIO29	CF_D14/GPIO30	CF_D15/GPIO31
CF_nIOR	CF_nIOW	CF_IRQ	CF_nRESET
CF_IORDY	CF_nCS0	CF_DMACK/GPIO7/TXD	CF_SA0
CF_SA1	CF_SA2	GPIO13 (CF_nCD)	CF_DMARQ/GPIO2/RXD
SMARTMEDIA INTERFACE (17 PINS)			
SM_D0	SM_D1	SM_D2	SM_D3
SM_D4	SM_D5	SM_D6	SM_D7
SM_ALE	SM_CLE	SM_nRE	SM_nWE
SM_nWP	SM_nB/R	SM_nCE	GPIO14 (SM_nCD)
SM_nWPS			
MEMORY STICK INTERFACE (11 PINS)			
MS_BS	MS_D0/MS_SDIO	MS_SCLK	GPIO12 (MS_INS)
MS_D1	MS_D2	MS_D3	MS_D4
MS_D5	MS_D6	MS_D7	
SD/MMC INTERFACE (12 PINS)			
SD_CMD	SD_CLK	SD_D0	SD_D1
SD_D2	SD_D3	GPIO6 (SD_WP)	GPIO15 (SD_nCD)
SD_D4	SD_D5	SD_D6	SD_D7
USB INTERFACE (8 PINS)			
USB+	USB-	RBIAS	VDD18PLL
VDDA33	XTAL2	XTAL1/CLKIN	REG_EN

Table 3.1 USB2250/51/59 128-Pin VTQFP Package (continued)

MEMORY/IO INTERFACE (28 PINS)			
MA0/CLK_SEL0	MA1/CLK_SEL1	MA2	MA3
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
MA16	MD0	MD1	MD2
MD3	MD4	MD5	MD6
MD7	nMRD	nMWR	nMCE
MISC (10 PINS)			
nRESET	GPIO3 (VBUS_DET)	GPIO4 (SCL/xD_ID)	GPIO5 (SDA)
GPIO1 (LED1)	GPIO8/CARD_PWR0	GPIO9/CARD_PWR1	GPIO10/CARD_PWR2
GPIO11/CARD_PWR3	TEST		
DIGITAL, POWER (14 PINS)			
(5) VDD33	(1) VDD18	(8) VSS	
TOTAL 128			

3.2 128-Pin List

Table 3.2 USB2250/51/59 128-Pin List

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
1	MA12	12	33	MD7	12	65	VDD33	-	97	MS_D6	12
2	MA15	12	34	MD3	12	66	CF_D13 / GPIO29	12	98	GPIO12 (MS_INS)	12
3	nMWR	12	35	MD2	12	67	CF_D6 / GPIO22	12	99	MS_D3	12
4	MA14	12	36	MD1	12	68	CF_D14 / GPIO30	12	100	MS_D7	12
5	GPIO5 (SDA)	12	37	MD0	12	69	CF_D7 / GPIO23	12	101	MS_SCLK	12
6	REG_EN	12	38	SM_nWPS	-	70	CF_D15 / GPIO31	12	102	VSS	-
7	USB+	-	39	SM_D7	12	71	CF_nCS0	12	103	TEST	-
8	USB-	-	40	SM_D6	12	72	CF_nIOR	12	104	VDD33	-
9	VSS	-	41	SM_D5	12	73	CF_nIOW	12	105	GPIO6 (SD_WP)	12
10	SD_D1	12	42	SM_D4	12	74	CF_IRQ	12	106	MA7	12
11	SD_D6	12	43	SM_D3	12	75	VSS	-	107	MA13	12
12	SD_D0	12	44	SD_D2	12	76	GPIO10 / CRD_ PWR2	12	108	MA6	12
13	SD_D7	12	45	SM_D1	12	77	VDD33	-	109	MA8	12
14	GPIO8 / CRD_ PWR0	12	46	SM_D0	12	78	GPIO9 / CRD_ PWR1	12	110	MA5	12
15	VDD33	-	47	SM_nWP	12	79	CF_nRESET	12	111	MA9	12
16	GPIO11 / CRD_ PWR3	12	48	SM_nWE	12	80	CF_IORDY	12	112	MA4	12
17	VSS	-	49	VDD18	-	81	VSS	-	113	MA11	12
18	SD_CLK	12	50	VDD33	-	82	CF_SA2	-	114	MA3	12
19	SD_D5	12	51	VSS	-	83	CF_SA1	12	115	nMRD	12
20	SD_CMD	12	52	SM_ALE	12	84	CF_SA0	12	116	MA2	12
21	SD_D4	12	53	SM_CLE	12	85	CF_D0 / GPIO16	12	117	CF_DMARQ / RXD / GPIO2	12
22	SD_D3	12	54	SM_nCE	12	86	CF_D1 / GPIO17	12	118	GPIO4 (SCL)	12

Table 3.2 USB2250/51/59 128-Pin List (continued)

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
23	SD_D2	12	55	SM_nRE	12	87	CF_D8 / GPIO24	12	119	CF_DMACK / TXD / GPIO7	12
24	MA10	12	56	SM_nB/R	-	88	CF_D2 / GPIO18	12	120	LED1 / GPIO1	12
25	MA1 / CLK_ SEL1	12	57	GPIO14 (SM_nCD)	12	89	CF_D9 / GPIO25	12	121	GPIO3 (VBUS_DET)	12
26	nMCE	12	58	GPIO13 (CF_nCD)	12	90	CF_D10 / GPIO26	12	122	VSS	-
27	MA0 / CLK_ SEL0	12	59	CF_D3 / GPIO19	12	91	MS_BS	12	123	XTAL2	-
28	MA16	12	60	CF_D11 / GPIO27	12	92	MS_D1	12	124	XTAL1 / CLKIN	-
29	MD6	12	61	CF_D4 / GPIO20	12	93	MS_D5	12	125	VDDPLL18	-
30	MD5	12	62	CF_D12 / GPIO28	12	94	MS_D0 / MS_DIO	12	126	VSS	-
31	MD4	12	63	CF_D5 / GPIO21	12	95	MS_D4	12	127	RBIAS	-
32	GPIO15 (SD_nCD)	12	64	nRESET	-	96	MS_D2	12	128	VDDA33	-

Chapter 4 Pin Configuration

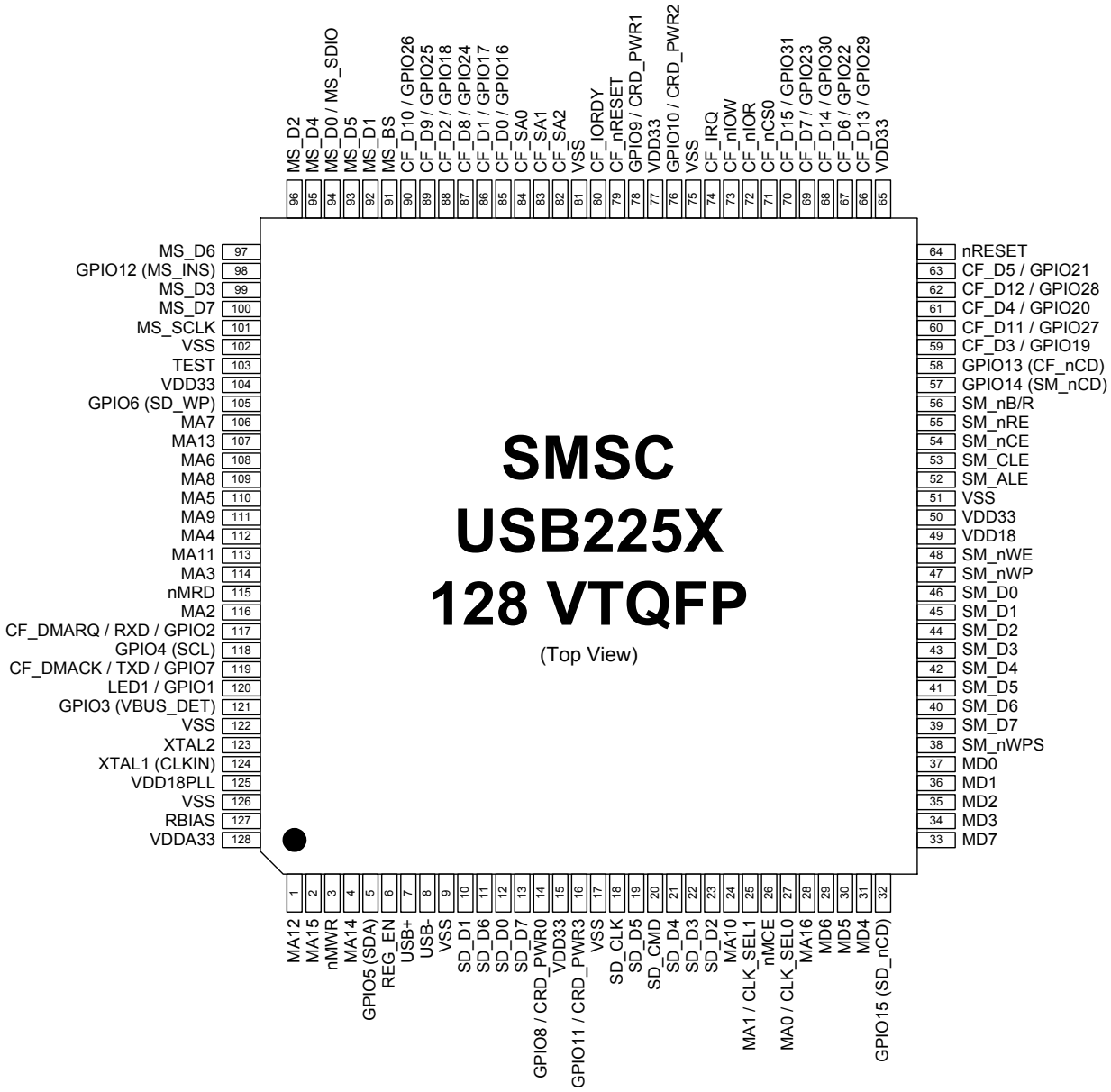

Figure 4.1 USB2250/51/59 128-Pin VTQFP Diagram

Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
COMPACT FLASH INTERFACE				
CF Chip Select 0	CF_nCS0	71	O12	This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF Register Address	CF_SA[2:0]	82 83 84	I/O12	These pins are the register select address bits for the CF ATA device.
CF Interrupt	CF_IRQ	74	IPD	This is the active high interrupt request signal from the CF device. This pin has an internal weak pull-down resistor that can be controlled by: CF_INTF_EN bit of CFC_ATA_MODE_CTL
CF Data 15-8 / GPIO	CF_D[15:8] / GPIO[31:24]	70 68 66 62 60 90 89 87	I/O12PD	CF_D[15:8]: The bi-directional data signals CF_D15 - CF_D8 in True IDE mode data transfer. In the True IDE Mode, all of task file register operations occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
			I/O12	GPIO[31:24]: These Pins are GPIOs if CF_INTF_EN bit of CFC_ATA_MODE CTL is disabled and EXTENDED_GPIO bit is set in UTIL_CONFIG1 is enabled.

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
CF Data 7-0 / GPIO	CF_D[7:0] / GPIO[23:16]	69 67 63 61 59 88 86 85	I/O12PD	CF_D[7:0]: The bi-directional data signals CF_D7 - CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of the task file register operations occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
			I/O12	GPIO[23:16]: These Pins are GPIOs if CF_INTF_EN bit of CFC_ATA_MODE CTL is disabled and EXTENDED_GPIO bit is set in UTIL_CONFIG1 is enabled.
IO Ready	CF_IORDY	80	IPU	This pin is active high input signal for IORDY. This pin has an internal weak pull-up resistor that can be controlled by: CF_INTF_EN bit of CFC_ATA_MODE CTL
CF Card Detection1	CF_nCD (GPIO13)	58	I/O12	This is a GPIO designated as the Compact Flash card detection pin.
CF Hardware Reset	CF_nRESET	79	O12	This pin is an active low hardware reset signal to CF device.
CF IO Read	CF_nIOR	72	O12	This pin is an active low read strobe signal for CF device.
CF IO Write Strobe	CF_nIOW	73	O12	This pin is an active low write strobe signal for CF device.
CF DMA request	CF_DMARQ / GPIO2 / RXD	117	I	CF_DMARQ: This pin is the DMA request from the device to the CF controller.
			I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			I	RXD: The signal can be used as input to the RXD of UART in the device, when the TXD_RXD_SEL bit in UTIL_CONFIG1 register is cleared to "0".
CF DMA acknowledge	CF_nDMACK/ GPIO / TXD	119	O12	CF_nDMACK: This pin is an active low dma acknowledge signal for CF device.
			I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			O12	TXD: In addition, as an output, the GPIO7 can be used as an output TXD of UART in the device, when the GPIO2/TXD bit in UTL_CONFIG register is set to "1"
SMART MEDIA INTERFACE				
SM Write Protect	SM_nWP	47	O12PD	This pin is an active low write protect signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SM Address Strobe	SM_ALE	52	O12PD	This pin is an active high Address Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM Command Strobe	SM_CLE	53	O12PD	This pin is an active high Command Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM Data 7-0	SM_D[7:0]	39 40 41 42 43 44 45 46	I/O12PD	These pins are the bi-directional data signals SM_D7-SM_D0. The bi-directional data signal has an internal weak pull-down resistor.
SM Read Enable	SM_nRE	55	O12PU	This pin is an active low read strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET, and is controlled by the SM_PU bit of the SMC_CTL register. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Write Enable	SM_nWE	48	O12PU	This pin is an active low write strobe signal for SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET, and is controlled by the SM_PU bit of the SMC_CTL register. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Write Protect Switch	SM_nWPS	38	IPU	A write-protect seal is detected when this pin is low. This pin has an internal weak pull-up resistor that is controlled by the SM_INTF_EN bit of the SMC_MODE_CTL2 register.
SM Busy or Data Ready	SM_nBR	56	IPU	This pin is connected to the BSY/RDY pin of the SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET, and is controlled by the SM_PU bit of the SMC_CTL register. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SM Chip Enable	SM_nCE	54	O12PU	This pin is the active low chip enable signal to the SM device. When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET, and is controlled by the SM_PU bit of the SMC_CTL register. If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Card Detection GPIO	SM_nCD (GPIO14)	57	I/O12	This is a GPIO designated as the Smart Media card detection pin.
MEMORY STICK INTERFACE				
MS Bus State	MS_BS	91	O12	This pin is connected to the BS pin of the MS device. It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS Card Insertion GPIO	MS_INS (GPIO12)	98	IPU	This is a GPIO designated as the Memory Stick card detection pin.
MS System CLK	MS_SCLK	101	O12	This pin is an output clock signal to the MS device. The clock frequency is software configurable.
MS System Data In/Out	MS_D[7:1]	100 97 93 95 99 96 92	I/O12PD	MS_D[7:0]: These pins are the bi-directional data signal for the MS device. MS_D2 and MS_D3 have weak pull-down resistors. MS_D1 has a pull down resistor if in parallel mode, otherwise it is disabled. In 4 or 8 bit parallel mode, there is a weak pull-down resistor on all MS_D7~0 signals. The resistors are controlled by MSC_SYSTEM_0, MSC_MODE_CTL and MSC_PRO_HG registers.
MS System Data In/Out	MS_D0 / MS_SDIO	94	I/O12PD	MS_D0: This pin is one of the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on MS_D0. MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. MS_D1 has a pull down resistor if in parallel mode, otherwise it is disabled. In 4 or 8 bit parallel mode, there is a weak pull-down resistor on all MS_D7~0 signals. The resistors are controlled by MSC_SYSTEM_0, MSC_MODE_CTL and MSC_PRO_HG registers.
				MS_SDIO: Serial Data Bus. Transfer direction and types of data change depending on the Bus State.

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SD / MMC INTERFACE				
SD Data 7-0	SD_D[7:0]	13 11 19 21 22 23 10 12	I/O12PU	These are the bi-directional data signals SD_D0 - SD_D7. The bi-directional signals should have weak pull-up resistors. The register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE_CTL
SD Clock	SD_CLK	18	O12	This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD Command	SD_CMD	20	I/O12PU	This is a bi-directional signal that connects to the CMD signal of SD/MMC device. The bi-directional signal should have an internal weak pull-up resistor. The pull-up register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE CTL
SD Write Protected GPIO	GPIO6 (SD_WP)	105	I/O12	This is a GPIO designated as the Secure Digital card mechanical write detect pin.
SD Card Detect GPIO	GPIO15 (SD_nCD)	32	I/O12	This is a GPIO designated as the Secure Digital card detection pin.
USB INTERFACE				
USB Bus Data	USB+ USB-	7 8	I/O-U	These pins connect to the USB bus data signals.
USB Transceiver Bias	RBIAS	127	I-R	A 12.0k , 1.0% resistor is attached from VSSA to this pin in order to set the transceiver's internal bias currents.
Crystal Input/External Clock Input	XTAL1 (CLKIN)	124	ICLKx	24MHz Crystal or external clock input. XTAL: This pin can be connected to one terminal of the crystal or can be connected to an external 24/48MHz clock when a crystal is not used. **Note:** The MA[1:0] pins will be sampled while nRESET is asserted, and the value will be latched upon nRESET negation. This will determine the clock source and value.
Crystal Output	XTAL2	123	OCLKx	24MHz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
MEMORY / IO INTERFACE				
Memory Data Bus	MD[7:0]	33 29 30 31 34 35 36 37	I/O12	These signals are used to transfer data between the internal CPU and the external program memory. **Note:** These pins have internal weak pull-up resistors that are controlled by the MD_PU_DIS bit of the PWR_MGMT_CTL1 register.
Memory Address Bus	MA16	28	O12	These signals address memory locations within the external memory. MA16 is a bit generated by the ROM Mapper.
Memory Address Bus	MA[15:2]	2 4 107 1 113 24 111 109 106 108 110 112 114 116	O12	These signals address memory locations within the external memory. **Note:** USB2259 requires that MA2 be tied to 3.3V via a 10K resistor.
Memory Address Bus	MA1[1:0] / CLK_ SEL1[1:0]	25 27	O12	MA[1:0]: These signals address memory locations within the external memory.
			I/O12PD	CLK_SEL[1:0]: During nRESET assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When nRESET is negated, the value on these pins will be internal latched and these pins will revert to MA[1:0] functionality; the internal pull-downs will be disabled. CLK_SEL[1:0] = '00'. 24MHz CLK_SEL[1:0] = '01'. RESERVED CLK_SEL[1:0] = '10'. RESERVED CLK_SEL[1:0] = '11'. 48MHz **Note:** If the latched value is '1', then the corresponding MA pin is tri-stated when the chip is in the powerdown state. If the latched value is '0', then the corresponding MA pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).
Memory Write Strobe	nMWR	3	O12	Program Memory Write; active low
Memory Read Strobe	nMRD	115	O12	Program Memory Read; active low

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
Memory Chip Enable	nMCE	26	O12	Program Memory Chip Enable; active low. This signal is asserted when any external access is being done by the processor. This signal is held to logic 'high' while nRESET is asserted.
MISC				
General Purpose I/O	LED1 / GPIO1	120	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
				In addition, as an output, the GPIO1 can be used output controlled by the LED1_GPIO1 register.
General Purpose I/O	GPIO3 (VBUS_DET)	121	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. This pin is not 5V tolerant. An external resistor divider must be used when connected to VBUS.
General Purpose I/O	GPIO4 (SCL)	118	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
			O12	SCL: This is the clock output when used with an external EEPROM.
General Purpose I/O	GPIO5 (SDA)	5	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. SDA: This is the data pin when used with an external serial EEPROM.
General Purpose I/O	GPIO8 / CRD_PWR0	14	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			I/O200	CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.
General Purpose I/O	GPIO9 / CRD_PWR1	78	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			I/O200	CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.
General Purpose I/O	GPIO10 / CRD_PWR2	76	I/O12	GPIO: These pins may be used either as input, edge sensitive interrupt input, or output. It is a requirement that this is the only FET used to power SM devices. Failure to do this will violate SM voltage specification on SM device pins.
			I/O200	CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.
General Purpose I/O	GPIO11 / CRD_PWR3	16	I/O12	GPIO: These pins may be used either as input, edge sensitive interrupt input, or output.
			I/O200	CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.

Table 5.1 USB2250/51/59 128-Pin VTQFP Pin Descriptions (continued)

NAME	SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
RESET Input	nRESET	64	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1μs wide.
TEST Input	TEST	103	I	This signal is used for testing the chip. User should normally tie this pin low externally, if the test function is not used.
Regulator Enable	REG_EN	6	IPU	This signal is used to enable the internal 1.8V regulator.
ANALOG / DIGITAL POWER, and GROUND				
1.8V Digital Core Power	VDD18	49		All VDD18 pins must be connected together on the circuit board. +1.8V Core power. If the internal regulator is enabled, then this pin must have a 1.0μF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
3.3V Power & Voltage Regulator Input	VDD33	15 50 65 77 104		3.3V Power & Voltage Regulator Input
1.8V PLL Power	VDD18PLL	125		This pin is the 1.8V Power for the PLL. If the internal regulator is enabled, then this pin must have a 1.0μF (or greater) ±20% (ESR <0.1Ω) capacitor to VSS.
3.3V Analog Power	VDDA33	128		3.3V Analog Power
Ground	VSS	9 17 51 75 81 102 122 126		Ground Reference

Notes:

1. Hot-insertion capable card connectors are required for all flash media. It is required for the SD connector to have a Write Protect switch. This allows the chip to detect the MMC card.
2. nMCE is normally asserted except when the 8051 is in standby mode.
3. Refer to PWR_MGMT_CTL1 register for controlling pull-up / down resistors associated with the pins as well as the individual card control registers.

5.2 Buffer Type Descriptions

Table 5.2 USB2250/51/59 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger.
I/O12	Input/Output buffer with 12mA sink and 12mA source.
I/O200	Input/Output buffer 12mA with FET disabled, 100/200mA source only with FET enabled.
I/O12PD	Input/Output buffer with 12mA sink and 12mA source, with an internal weak pull-down resistor.
I/O12PU	Input/Output buffer with 12mA sink and 12mA source with a pull-up resistor.
O12	Output buffer with 12mA source.
O12PU	Output buffer with 12mA sink and 12mA source, with a pull-up resistor.
O12PD	Output buffer with 12mA sink and 12mA source, with a pull-down resistor.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog Input/Output Defined in USB specification.
I-R	RBIAS.

Chapter 6 Pin Reset State Table

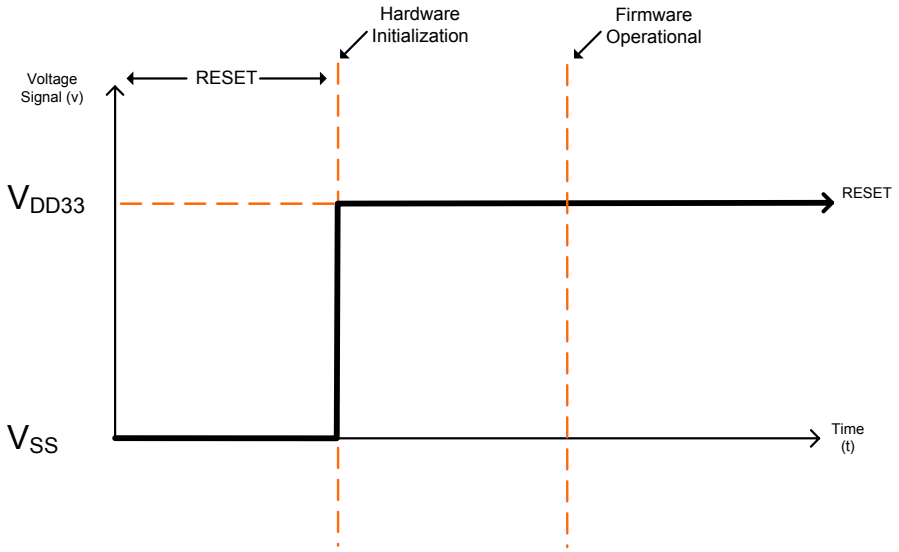

Figure 6.1 Pin Reset States

LEGEND	
yes	hardware enables function
--	hardware disables function
z	hardware disables output driver
pu	hardware enables pullup
pd	hardware enables pulldown
hw	hardware controls function, but state is protocol dependent
(fw)	firmware controls function through registers
VDD	hardware supplies power through pin, applicable only to CARD_PWR pins
none	hardware disables pad

Figure 6.2 Legend for Pin Reset States Table

6.1 128-Pin Reset States

Table 6.1 USB2250/51/59 128-Pin Reset States

		RESET STATE				Post-Reset State xD Mode				Post-Reset State SD Mode				Post-Reset State MS Mode			
PIN	PIN NAME	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT
85	CF_D0/GPIO16	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
86	CF_D1/GPIO17	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
88	CF_D2/GPIO18	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
59	CF_D3/GPIO19	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
61	CF_D4/GPIO20	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
63	CF_D5/GPIO21	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
67	CF_D6/GPIO22	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
69	CF_D7/GPIO23	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
87	CF_D8/GPIO24	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
89	CF_D9/GPIO25	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
90	CF_D10/GPIO26	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
60	CF_D11/GPIO27	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
62	CF_D12/GPIO28	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
66	CF_D13/GPIO29	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
68	CF_D14/GPIO30	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
70	CF_D15/GPIO31	GPIO	z	--	--	CF	hw	pd	hw	GPIO	(fw)	(fw)	(fw)				
72	CF_nIOR	CF	z	--	--	CF	hw	--	--								

Table 6.1 USB2250/51/59 128-Pin Reset States (continued)

		RESET STATE				Post-Reset State xD Mode				Post-Reset State SD Mode				Post-Reset State MS Mode			
PIN	PIN NAME	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT
73	CF_nIOW	CF	z	--	--	CF	hw	--	--								
74	CF_nIRQ	CF	z	--	--	CF	z	pd	yes								
79	CF_nRESET	CF	z	--	--	CF	(fw)	--	--								
80	CF_IORDY	CF	z	--	--	CF	z	pu	yes								
71	CF_nCS0	CF	z	--	--	CF	hw	(fw)	--								
84	CF_SA0	CF	z	--	--	CF	hw	--	--								
83	CF_SA1	CF	z	--	--	CF	hw	--	--								
82	CF_SA2	CF	z	--	--	CF	hw	--	--								
119	CF_DMACK/GPIO7/TXD	GPIO	0	--	--	CF	hw	--	--	GPIO	(fw)	(fw)	(fw)	TXD	hw	--	--
117	CF_DMARQ/GPIO2/RXD	GPIO	0	--	--	CF	z	pd	yes	GPIO	(fw)	(fw)	(fw)	RXD	z	(fw)	yes
58	GPIO13(CF_nCD)	GPIO	z	pu	yes	GPIO	(fw)	(fw)	(fw)								
46	SM_D0	SM	z	pd	--	SM	hw	pd	yes								
45	SM_D1	SM	z	pd	--	SM	hw	pd	yes								
44	SM_D2	SM	z	pd	--	SM	hw	pd	yes								
43	SM_D3	SM	z	pd	--	SM	hw	pd	yes								
42	SM_D4	SM	z	pd	--	SM	hw	pd	yes								
41	SM_D5	SM	z	pd	--	SM	hw	pd	yes								
40	SM_D6	SM	z	pd	--	SM	hw	pd	yes								

Table 6.1 USB2250/51/59 128-Pin Reset States (continued)

	RESET STATE				Post-Reset State xD Mode				Post-Reset State SD Mode				Post-Reset State MS Mode		
PIN NAME	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD	IN-PUT	FUNCTION	OUT-PUT	PU/PD
SM_D7	SM	z	pd	--	SM	hw	pd	yes							
SM_ALE	SM	z	pd	--	SM	hw	pd	--							
SM_CLE	SM	z	pd	--	SM	hw	pd	--							
SM_nWP	SM	z	pd	--	SM	(fw)	pd	--							
SM_nWPS	SM	z	--	--	SM	z	pu	yes							
GPIO14(SM_nCD)	GPIO	z	pu	yes	GPIO	(fw)	(fw)	(fw)							
MS_BS	MS	z	pd	--	MS	hw	hw	--							
MS_SCLK	MS	z	pd	--	MS	hw	hw	--							
MS_D0	MS	z	pd	--	MS	hw	pd	yes							
MS_D1	MS	z	pd	--	MS	hw	hw	yes							
MS_D2	MS	z	pd	--	MS	hw	pd	yes							
MS_D3	MS	z	pd	--	MS	hw	pd	yes							
MS_D4	MS	z	pd	--	MS	hw	pd	yes							
MS_D5	MS	z	pd	--	MS	hw	hw	yes							
MS_D6	MS	z	pd	--	MS	hw	pd	yes							
MS_D7	MS	z	pd	--	MS	hw	pd	yes							
GPIO12(MS_INS)	GPIO	z	pu	yes	GPIO	(fw)	(fw)	(fw)							
SD_CMD	SD	z	--	--	SD	hw	pu	yes							
SD_CLK	SD	z	--	--	SD	hw	--	yes							
SD_D0	SD	z	--	--	SD	hw	pu	yes							
SD_D1	SD	z	--	--	SD	hw	pu	yes							
SD_D2	SD	z	--	--	SD	hw	pu	yes							
SD_D3	SD	z	--	--	SD	hw	pu	yes							
SD_D4	SD	z	--	--	SD	hw	pu	yes							
SD_D5	SD	z	--	--	SD	hw	pu	yes							
SD_D6	SD	z	--	--	SD	hw	pu	yes							
SD_D7	SD	z	--	--	SD	hw	pu	yes							
GPIO6(SD_WP)	GPIO	0	--	--	GPIO	(fw)	(fw)	(fw)							

Table 6.1 USB2250/51/59 128-Pin Reset States (continued)

	RESET STATE				Post-Reset State xD Mode				Post-Reset State SD Mode				Post-Reset State MS Mode		
PIN NAME	**FUNCTION**	**OUT-PUT**	**PU/ PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/ PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/ PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/ PD**
GPIO15(SD_nCD)	GPIO	z	pu	yes	GPIO	(fw)	(fw)	(fw)							
MA0	MA	z	pd	yes	MA	hw	--	--							
MA1	MA	z	pd	yes	MA	hw	--	--							
MA2	MA	z	pd	yes	MA	hw	--	--							
MA3	MA	z	pd	yes	MA	hw	--	--							
MA4	MA	0	--	--	MA	hw	--	--							
MA5	MA	0	--	--	MA	hw	--	--							
MA6	MA	0	--	--	MA	hw	--	--							
MA7	MA	0	--	--	MA	hw	--	--							
MA8	MA	0	--	--	MA	hw	--	--							
MA9	MA	0	--	--	MA	hw	--	--							
MA10	MA	0	--	--	MA	hw	--	--							
MA11	MA	0	--	--	MA	hw	--	--							
MA13	MA	0	--	--	MA	hw	--	--							
MA16	MA	0	--	--	MA	hw	--	--							
MD0	MA	z	pu	--	MA	hw	hw	hw							
MD1	MA	z	pu	--	MA	hw	hw	hw							
MD2	MA	z	pu	--	MA	hw	hw	hw							
MD3	MA	z	pu	--	MA	hw	hw	hw							
MD4	MA	z	pu	--	MA	hw	hw	hw							
MD5	MA	z	pu	--	MA	hw	hw	hw							
MD6	MA	z	pu	--	MA	hw	hw	hw							
MD7	MA	z	pu	--	MA	hw	hw	hw							
nMRD	MA	1	--	--	MA	hw	--	--							
nMCE	MA	1	--	--	MA	0	--	--							
GPIO1(LED1)	GPIO	0	--	--	GPIO	(fw)	(fw)	(fw)							
GPIO4	GPIO	0	--	--	GPIO	(fw)	(fw)	(fw)							
GPIO8/CARD_PWR0	GPIO	z	--	--	GPIO	(fw)	(fw)	(fw)	PWR	VDD	--	--			

Table 6.1 USB2250/51/59 128-Pin Reset States (continued)

	RESET STATE				Post-Reset State xD Mode				Post-Reset State SD Mode				Post-Reset State MS Mode		
PIN NAME	**FUNCTION**	**OUT-PUT**	**PU/PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/PD**	**IN-PUT**	**FUNCTION**	**OUT-PUT**	**PU/PD**
GPIO9/CARD_PWR1	GPIO	z	--	--	GPIO	(fw)	(fw)	(fw)	PWR	VDD	--	--			
GPIO10/CARD_PWR2	GPIO	z	--	--	GPIO	(fw)	(fw)	(fw)	PWR	VDD	--	--			
GPIO11/CARD_PWR3	GPIO	z	--	--	GPIO	(fw)	(fw)	(fw)	PWR	VDD	--	--			
TEST	TEST	z	--	yes	TEST	z	--	yes							
nRESET	nRESET	z	--	yes	nRESET	z	--	yes							
MA12	MA	0	--	--	MA	hw	--	--							
MA14	MA	0	--	--	MA	hw	--	--							
MA15	MA	0	--	--	MA	hw	--	--							
nMWR	MA	1	--	--	MA	hw	--	--							
GPIO3	GPIO	z	--	yes	GPIO	(fw)	(fw)	(fw)							
GPIO5	GPIO	0	pu	--	GPIO	(fw)	(fw)	(fw)							
SM_nRE	SM	z	--	--	SM	hw	(fw)	--							
SM_nWE	SM	z	--	--	SM	hw	(fw)	--							
SM_nB/R	SM	z	--	--	SM	z	(fw)	yes							
SM_nCE	SM	z	--	--	SM	hw	(fw)	--							
USB+	USB+	z	--	--	USB+	z	hw	hw							
USB-	USB-	z	--	--	USB-	z	hw	hw							
RBIAS															
XTAL1(CLKIN)															
XTAL2															
REG_EN															

Chapter 7 DC Parameters

7.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3V supply voltage + 2) ≤ 6	V	
Voltage on GPIO8, 9, 10 & 11		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63V and T_A is less than 70°C.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note 7.1 Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 7.2 When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

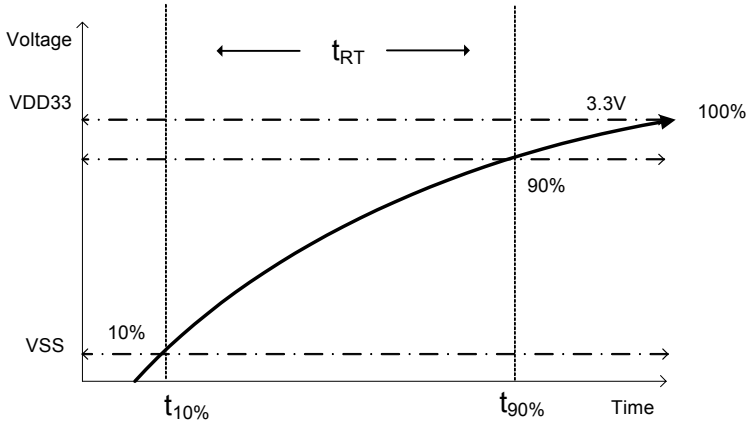

Figure 7.1 Supply Rise Time Model

Note 7.3 When powering the device, the maximum power supply ramp time should be set at a rate faster than 400µs. This speed is important to ensure that the device resets properly. Measure rise time at 10% and 90%.

7.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature	T_A	0	70	°C	
3.3V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	(Note 7.4)
3.3V supply rise time	t_{RT}	0	400	µs	(See Figure 7.1 and Note 7.3)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: (3.3V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DDA33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Note 7.4 A 3.3V regulator with an output tolerance of 1% must be used if the output of the internal power FET's must support a 5% tolerance.

7.3 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		420		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.5)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA @ V_{DD33}= 3.3V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12mA @ V_{DD33}= 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 7.5)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 7.6)						
I-R (Note 7.7)						
I/O200 Integrated Power FET for GPIO8, GPIO9, GPIO10, & GPIO11						
High Output Current Mode Short Circuit Current Limit 200mA	I_{OUT} I_{SC200}	200		 TBD	mA mA	$Vdrop_{FET}$ = 0.46V $Vout_{FET}$ = 0V
Low Output Current Mode Short Circuit Current Limit 100mA (Note 7.8)	I_{OUT} I_{SC100}	100		 TBD	mA mA	$Vdrop_{FET}$ = 0.23V $Vout_{FET}$ = 0V
On Resistance (Note 7.8)	R_{DSON}			2.1	Ω	I_{FET} = 70mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10µF
Supply Current Unconfigured	I_{CCINIT}		80	90	mA	
Supply Current Active Full Speed High Speed	I_{CC} I_{CC}		110 135	140 165	mA mA	V_{DD}, V_{DDP} = 1.8V V_{DD33}, V_{DDA} = 3.3V
Supply Current Standby	I_{CSBY}		350	750	µA	V_{DD}, V_{DDP} = 1.8V V_{DD33}, V_{DDA} = 3.3V

Note 7.5 Output leakage is measured with the current pins in high impedance.

Note 7.6 See The USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

Note 7.7 RBIAS is a 3.3V tolerant analog pin.

Note 7.8 Output current range is controlled by program software.

Note 7.9 The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to

the settings listed in Table 10.1, “USB2250/51/59 GPIO Usage (ROM Rev 0x00),” on page 36.

Note 7.10 The 3.3V supply should be at least at 75% of its operating condition before the 1.8V supply is allowed to ramp up.

7.4 Capacitance

T_A = 25°C; fc = 1MHz; V_{DD}, V_{DDP} = *1.8V*

Table 7.1 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 8 AC Specifications

8.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz ± 100ppm.

External Clock: 50% Duty cycle ± 10%, 24/48 MHz ± 100ppm, Jitter < 100ps rms.

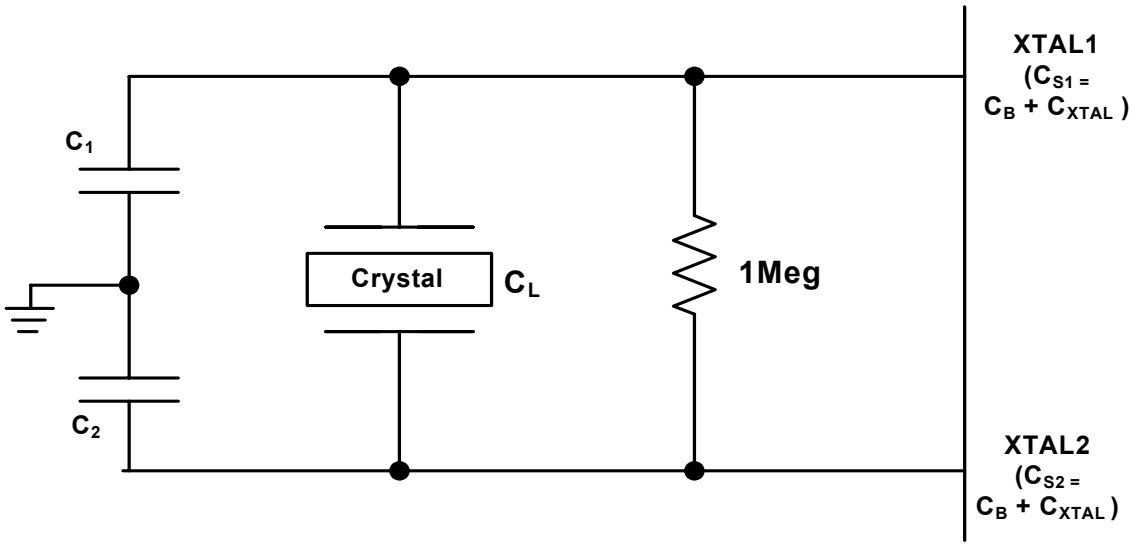

Figure 8.1 Typical Crystal Circuit

Note: C_B equals total board/trace capacitance.

$$\frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})} = C_L$$

Figure 8.2 Formula to Find Value of C_1 and C_2

Chapter 9 Package Outline

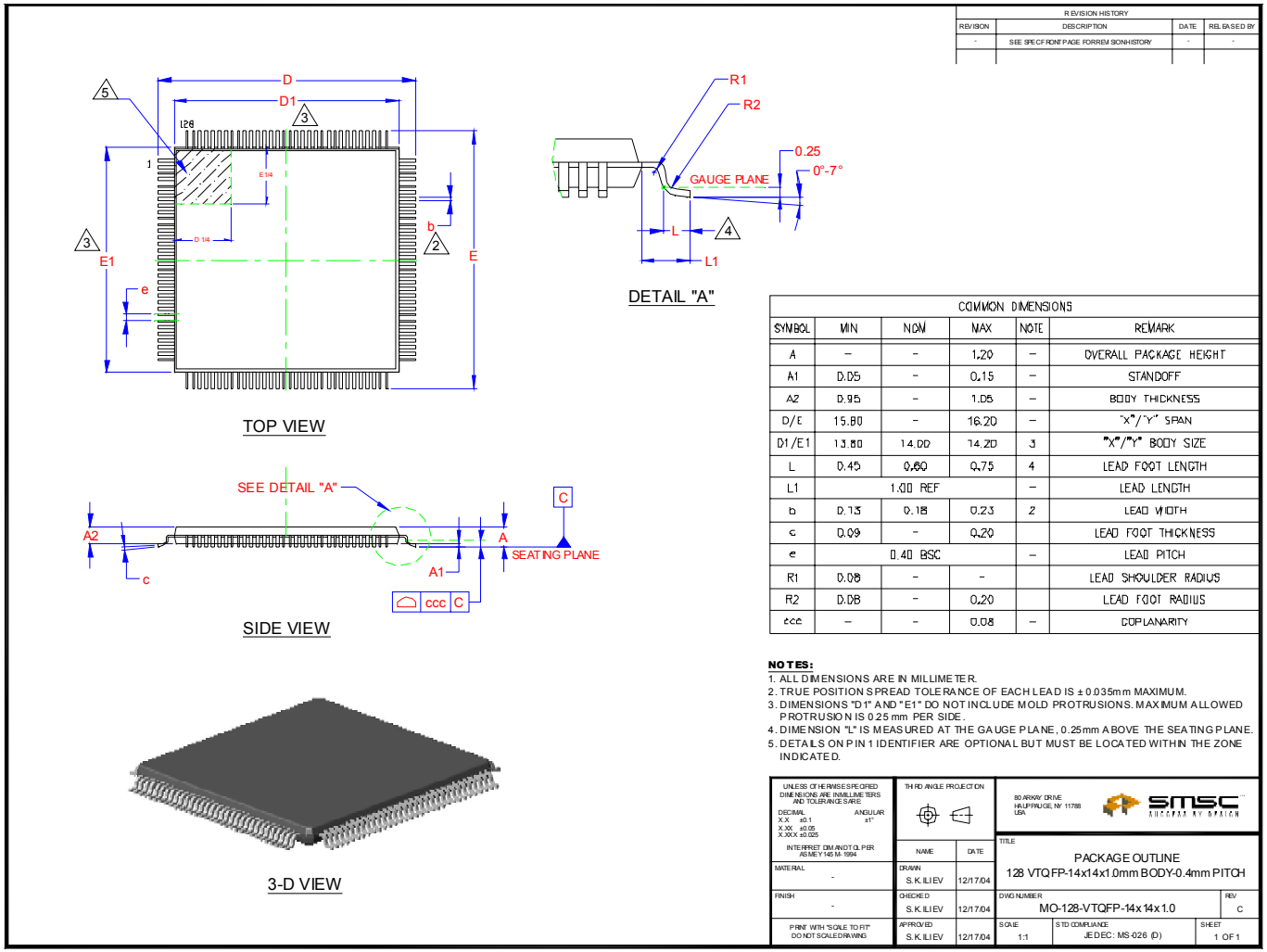

Figure 9.1 USB2250/51/59 128-Pin VTQFP, 14x14x1.0mm Body, 2.0mm Pitch

Chapter 10 GPIO Usage

Table 10.1 USB2250/51/59 GPIO Usage (ROM Rev 0x00)

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED1	LED indicator
GPIO2	H	CF_DMARQ / RXD	Compact Flash DMA request / Receive Port of Debugger
GPIO3	H	VBUS_DET	USB Vbus detect
GPIO4	H	SCL / xD_ID	Serial EEPROM clock output / xD card detect
GPIO5	H	SDA	Serial EEPROM data
GPIO6	L	SD_WP	SD Write Protect
GPIO7	H	CF_nDMACK / TXD	Compact Flash DMA acknowledge / Transmit Port of Debugger
GPIO8	L	CRD_PWR0	Card Power Control
GPIO9	L	CRD_PWR1	Card Power Control
GPIO10	L	CRD_PWR2	Card Power Control
GPIO11	L	CRD_PWR3	Card Power Control
GPIO12	L	MS_INS	Memory Stick Card Insertion
GPIO13	L	CF_nCD	Compact Flash card detect
GPIO14	L	xD_nCD	xD card detect
GPIO15	L	SD_nCD	Secure Digital card detect
GPIO16-32	USER	GPIO [32:16]	User defined