National Semiconductor

MM5241 3072-Bit (64 × 6 × 8) ROM

General Description

The MM5241 3072-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

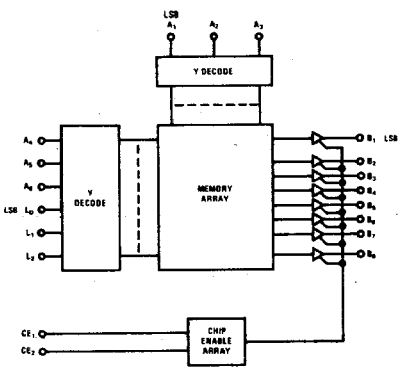
Features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

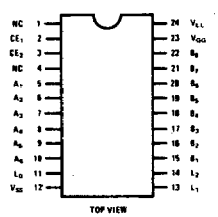
Applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5241J
See NS Package J24A

Order Number MM5241N
See NS Package N24B

Typical Applications

TTL/MOS Interface

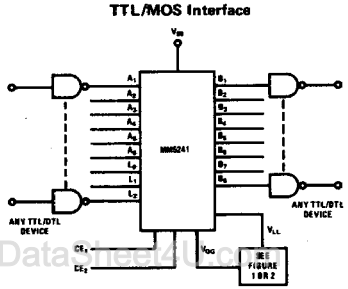


FIGURE 1. Power Saver for Small Memory Arrays

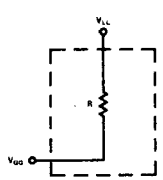
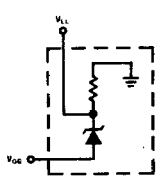


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME V_{LL} (MIN) = (−3V) +
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If CE_1 = 1 and CE_2 = 1 outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = V_S − 2V; 0 = most negative voltage level = V_{SS} − 4V).

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{LL} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature Range	–25°C to +70°C

Electrical Characteristics (Negative Logic) (Note 5)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{LL}$ = –12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "1"	I_L = 1.6 mA sink			.4	V
Logical "0"	I_L = 100 μA source	2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} – 4.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = –12, V_{LL} = –12, T_A = 25°C		23	50	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2) T_{ACCESS}	T_A = 25°C, V_{SS} = 5 $V_{GG} = V_{LL}$ = –12V	150	700	900	ns
Output AND Connections (Note 3)				20	

Note 1: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 2: Capacitances are measured periodically only.

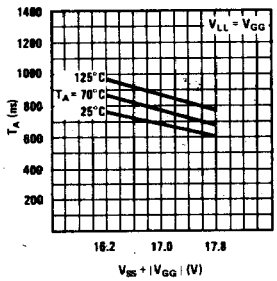
Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

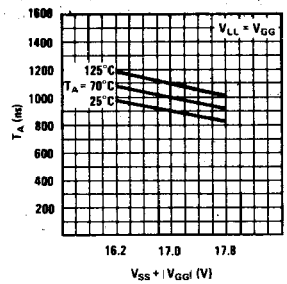
Note 5: All addresses and outputs are in negative true logic with the exception of L_0, L_1, and L_2 which are in positive logic.

Performance Characteristics

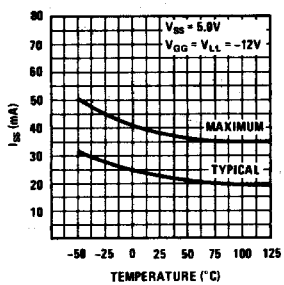
Typical Access Time vs Supply Voltage



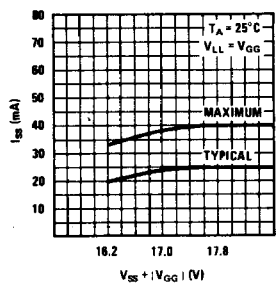
Guaranteed Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



Timing Diagram/Address Time