National Semiconductor

MOS ROMs

MM5240 2560-Bit Static Character Generator

General Description

The MM5240 2560-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 8 word by 5-bit memory organization.

The MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

Features

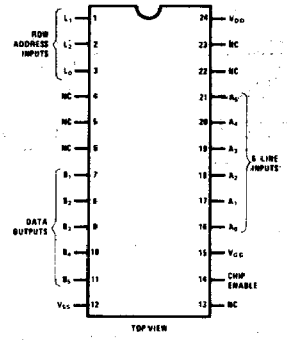
- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

Applications

- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

Connection Diagram

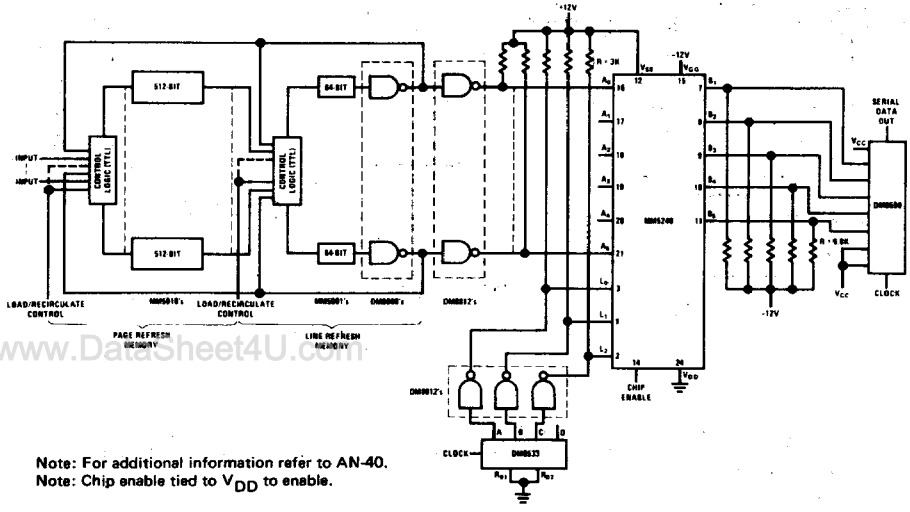
Dual-In-Line Package



Order Number MM5240J
See NS Package J24A

Order Number MM5240N
See NS Package N24B

Typical Application



Note: For additional information refer to AN-40.
Note: Chip enable tied to V_{DD} to enable.

Absolute Maximum Ratings

V_{GG} Supply Voltage V_{SS} – 30V
V_{DD} Supply Voltage V_{SS} – 15V
Input Voltage $(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature –65°C to +150°C
Lead Temperature (Soldering, 10 sec) 300°C

Operating Conditions

Operating Temperature 0°C to +70°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1MΩ to GND			V_{SS} – 9.0	V
Logical "0"		V_{SS} – 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 8.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	55	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, $V_{IN} = 0V$		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for $V_{SS} = +12V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+70°C$ unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns

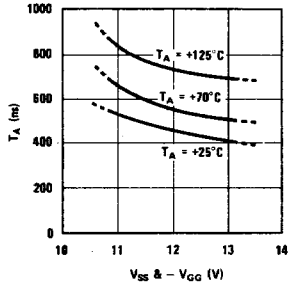
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

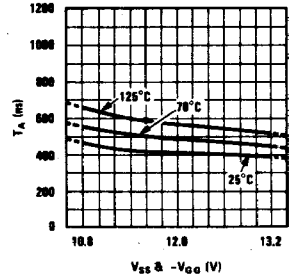
Note 5: Guaranteed by design.

Performance Characteristics

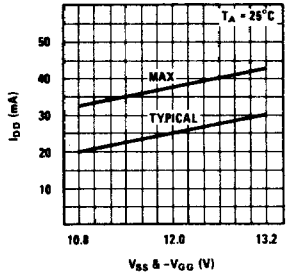
Guaranteed Access Time (T_A) vs Supply Voltage



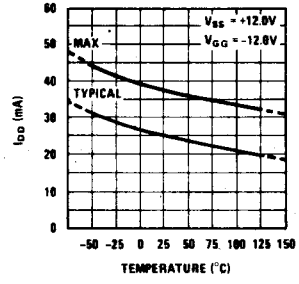
Typical Access Time (T_A) vs Supply Voltage



Power Supply Current vs Voltage



V_{DD} Power Supply Current vs Temperature



Timing Diagram/Address Time