2SJ540

Silicon P Channel MOS FET
High Speed Power Switching

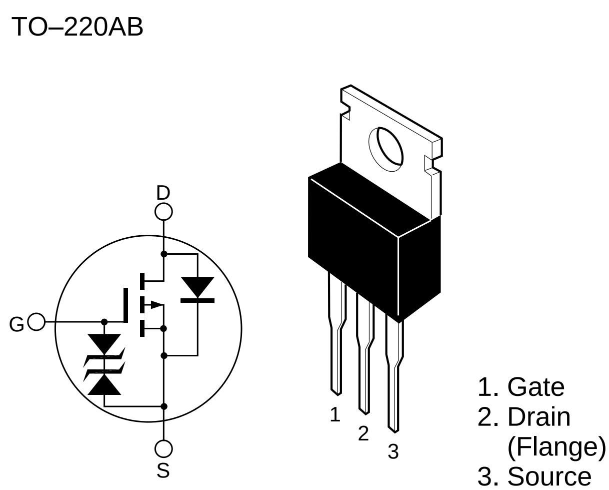
HITACHI

ADE-208-642A (Z)
2nd. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 0.11 Ω typ.
- Low drive current
- 4 V gete drive devices
- High speed switching

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–12	A
Drain peak current	$I_{D(pulse)}$ Note1	–48	A
Body-drain diode reverse drain current	I_{DR}	–12	A
Avalenche current	I_{AP} Note3	–12	A
Avalenche energy	E_{AR} Note3	12	mJ
Channel dissipation	Pch Note2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

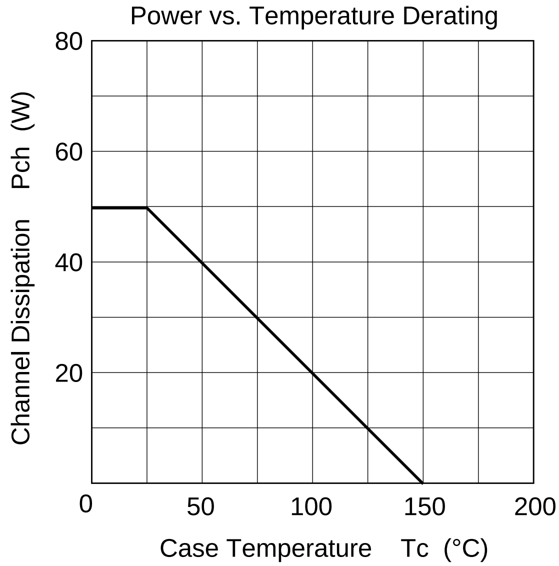
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

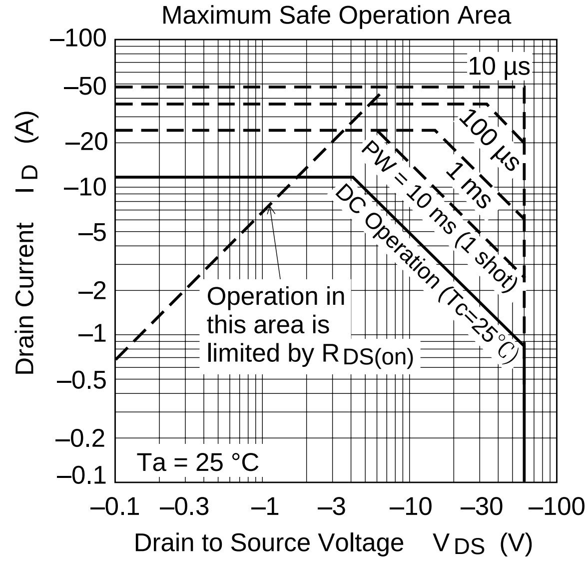
Electrical Characteristics (Ta = 25°C)

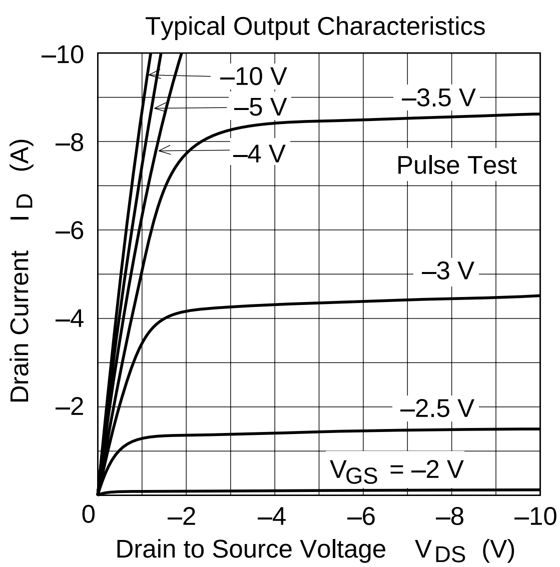
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1mA, V_{DS} = –10V
Static drain to source on state	$R_{DS(on)}$	—	0.11	0.15	Ω	I_D = –6A, V_{GS} = –10V Note4
resistance	$R_{DS(on)}$	—	0.16	0.23	Ω	I_D = –6A, V_{GS} = –4V Note4
Forward transfer admittance	$\|y_{fs}\|$	5	8	—	S	I_D = –6A, V_{DS} = –10V Note4
Input capacitance	Ciss	—	580	—	pF	V_{DS} = –10V
Output capacitance	Coss	—	300	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	85	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = –10V, I_D = –6A
Rise time	t_r	—	55	—	ns	R_L = 6Ω
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	60	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.2	—	V	I_F = –12A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = –12A, V_{GS} = 0 diF/ dt = 50A/µs

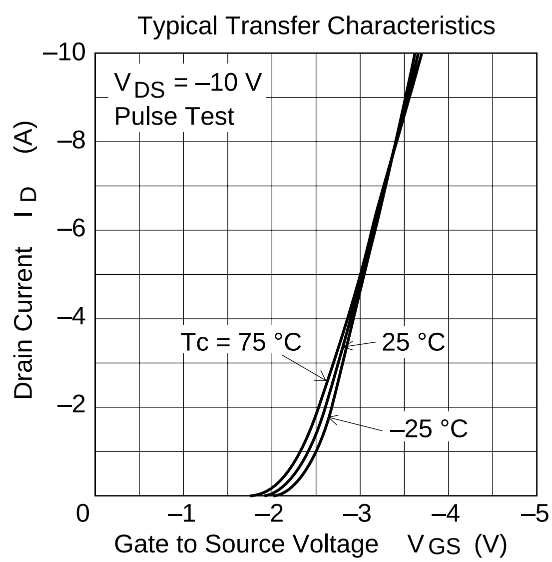
Note: 4. Pulse test

Main Characteristics

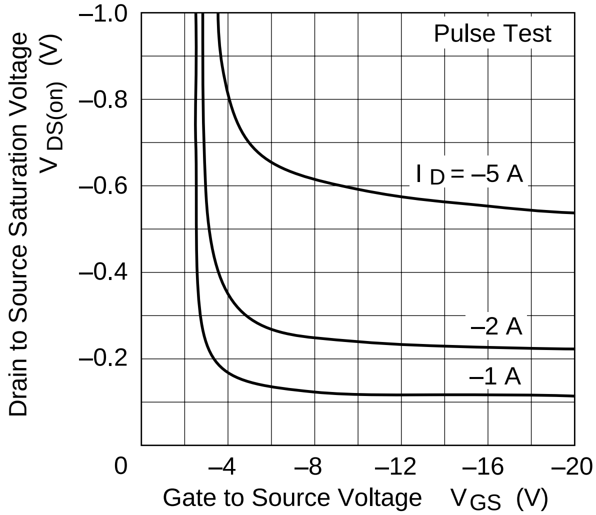




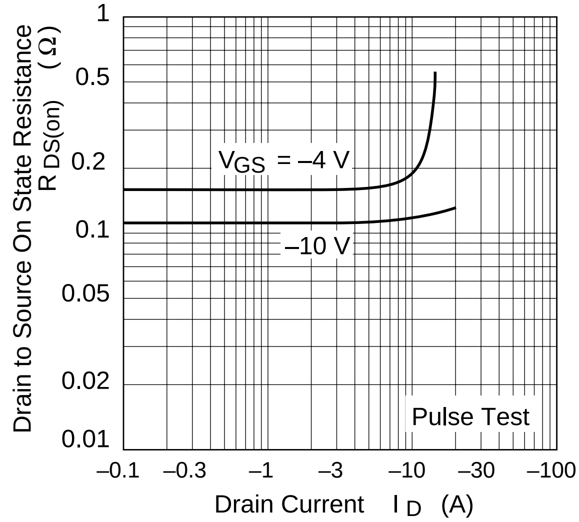




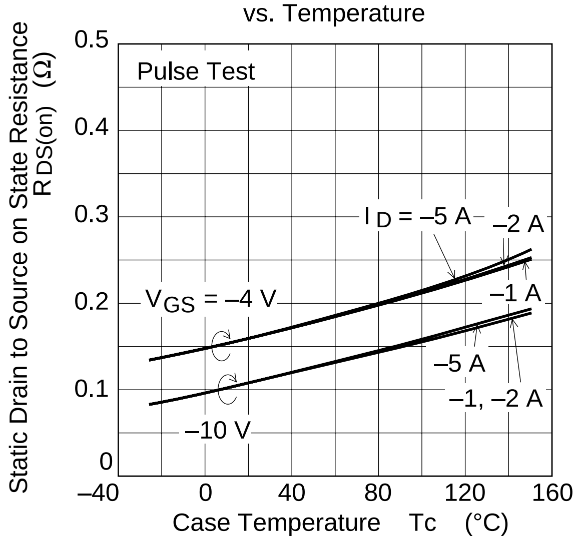
Drain to Source Saturation Voltage vs. Gate to Source Voltage



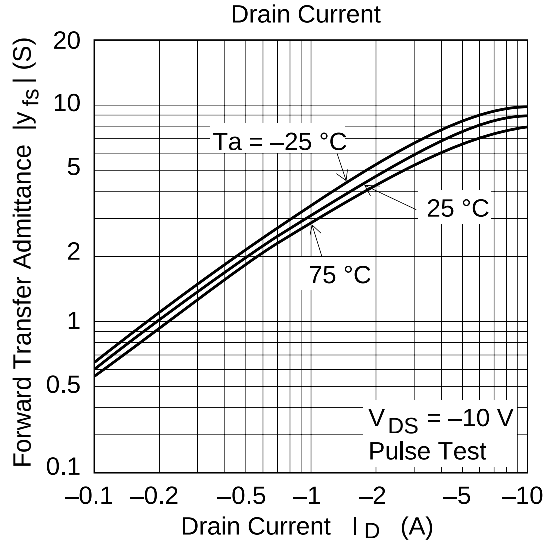
Static Drain to Source on State Resistance vs. Drain Current



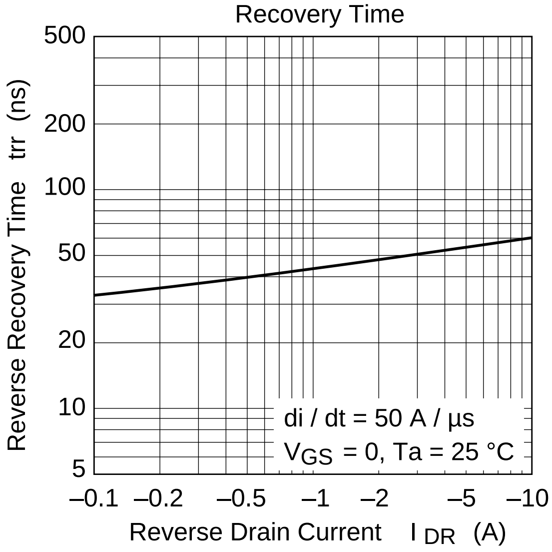
Static Drain to Source on State Resistance vs. Temperature



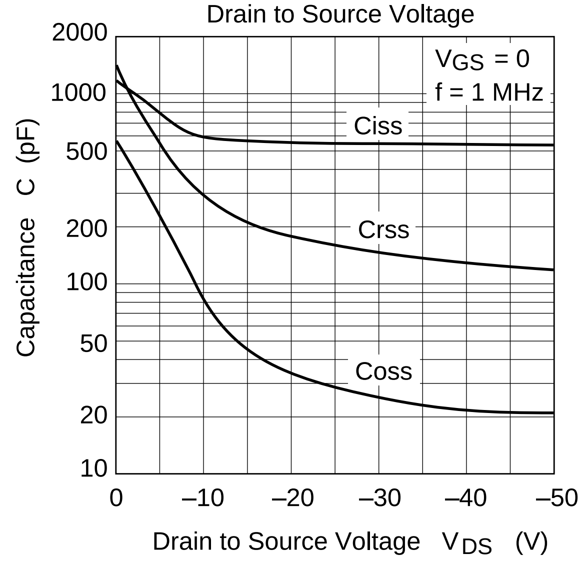
Forward Transfer Admittance vs. Drain Current



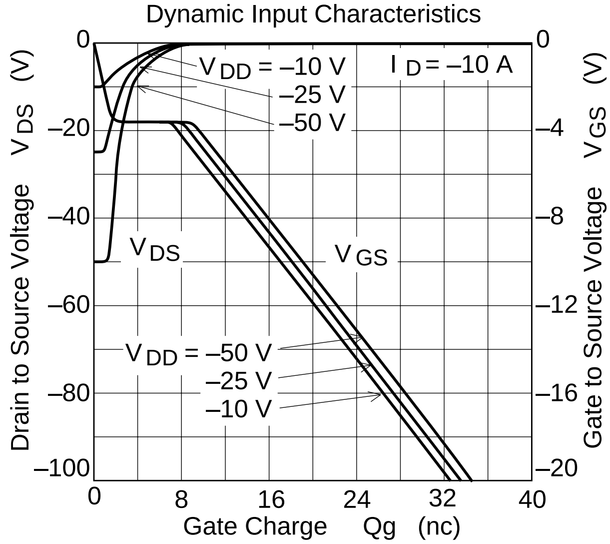
Body–Drain Diode Reverse Recovery Time



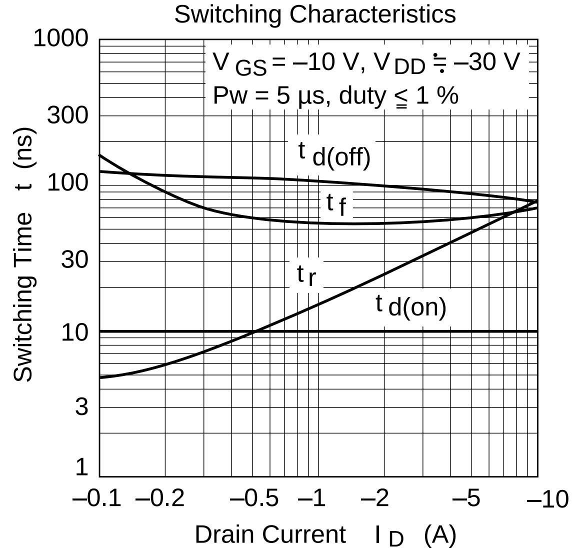
Typical Capacitance vs. Drain to Source Voltage



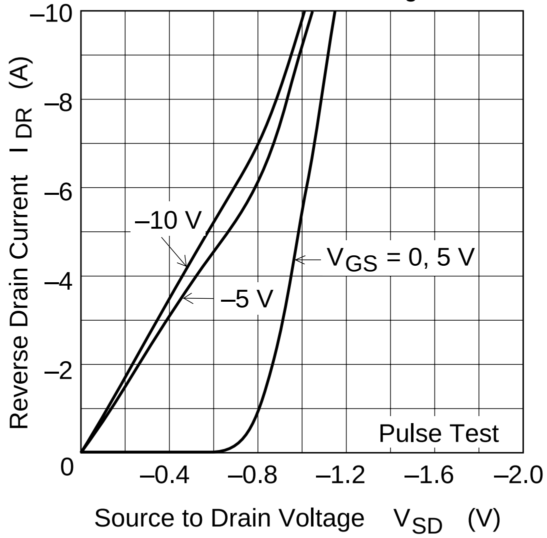
Dynamic Input Characteristics



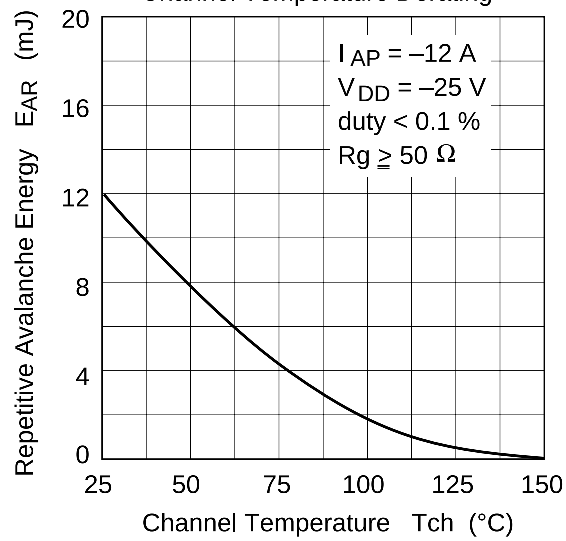
Switching Characteristics



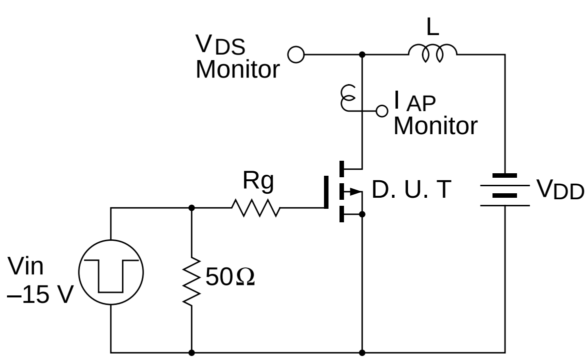
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

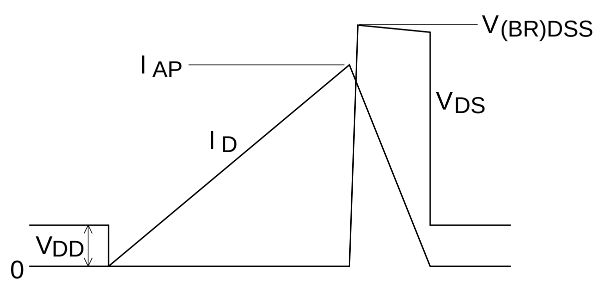


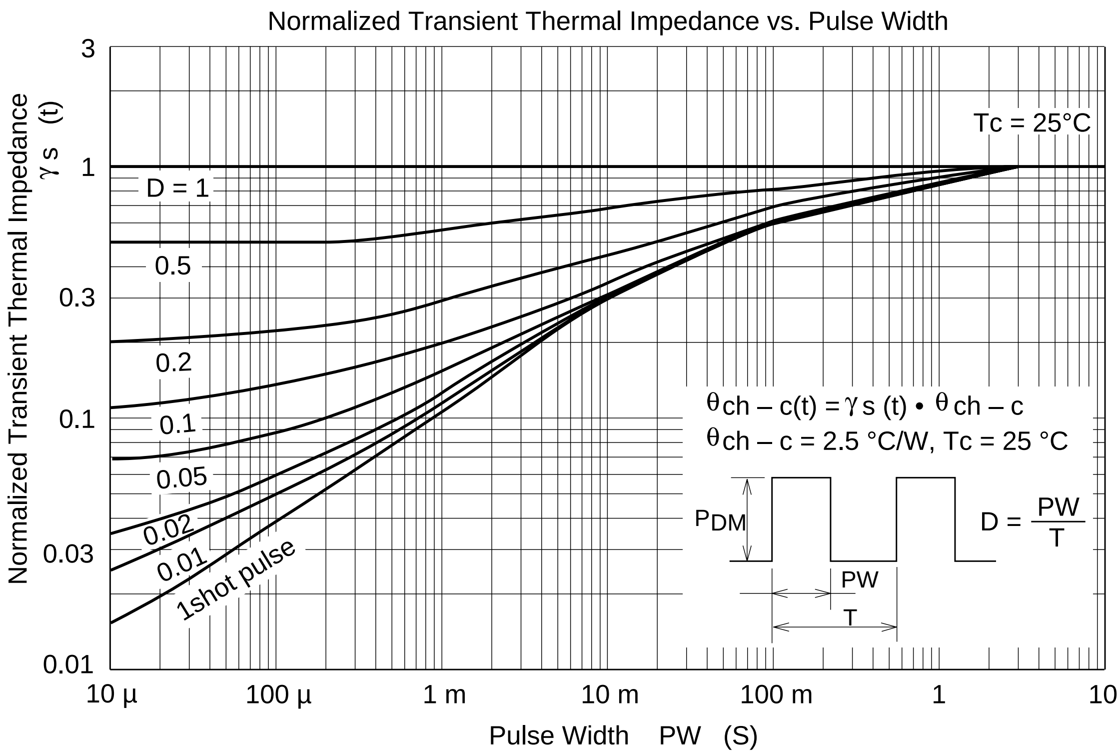
Avalanche Test Circuit



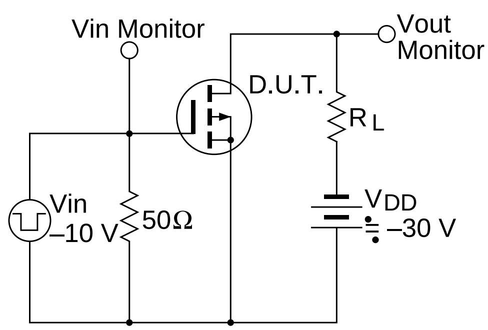
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}{}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

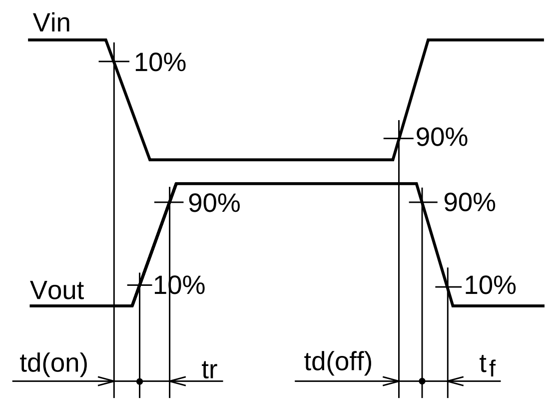




Switching Time Test Circuit

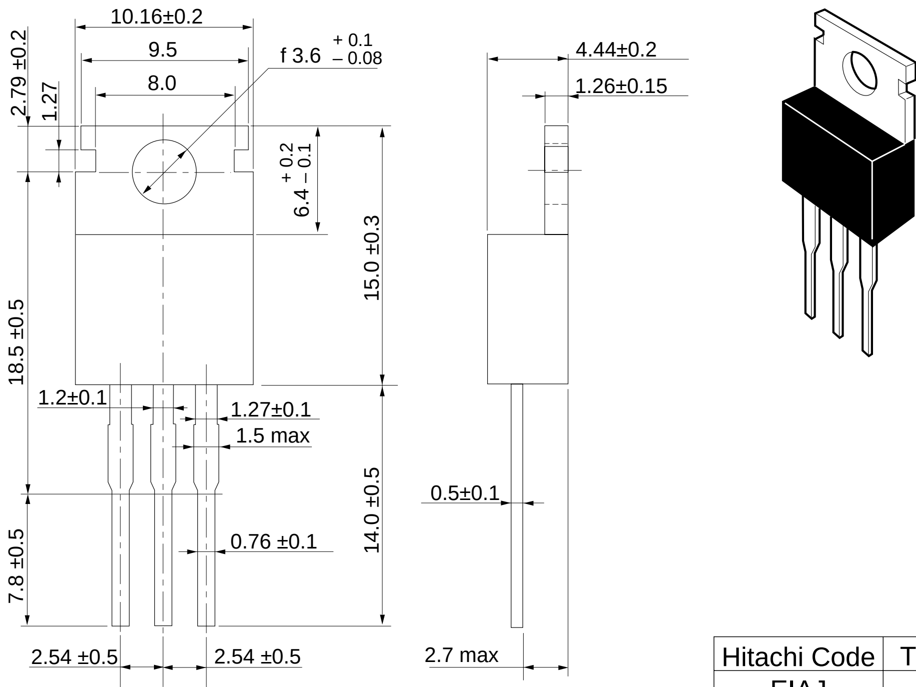


Waveform



Package Dimensions

Unit: mm



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