HT45R36
C/R to F Type 8-Bit OTP MCU

Technical Document

- Tools Information
- FAQs
- Application Note

Features

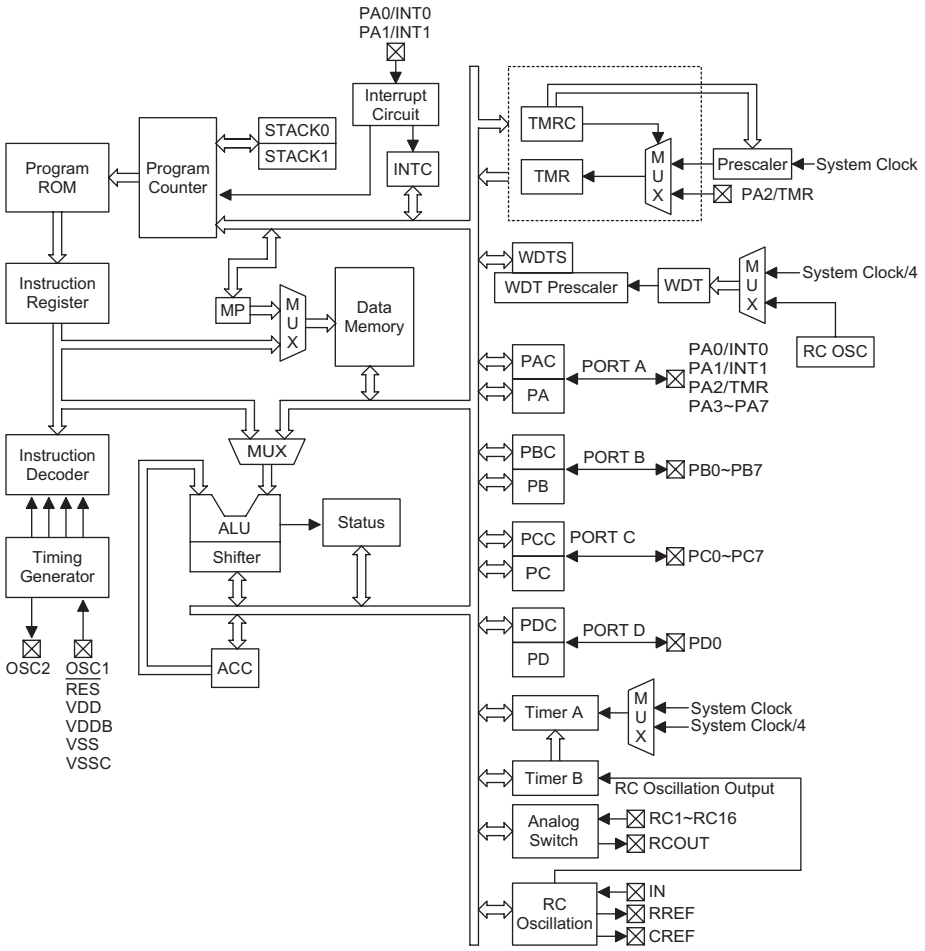
- Operating voltage:
  f_{SYS}=4MHz: 2.2V~5.5V
  f_{SYS}=8MHz: 3.3V~5.5V
- 25 bidirectional I/O lines
- Two external interrupt inputs shared with I/O lines
- 8-bit programmable timer/event counter with overflow interrupt and 7-stage prescaler
- External RC oscillation converter
- On-chip crystal and RC oscillator
- Watchdog Timer
- 16 capacitor/resistor sensor input
- 2048×14 program memory
- 120×8 data memory RAM
- Power Down and Wake-up function reduce power consumption
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- All instructions executed in one or two machine cycles
- 14-bit table read instruction
- Four-level subroutine nesting
- Bit manipulation instruction
- 63 powerful instructions
- Low voltage reset function
- 44/52-pin QFP package

General Description

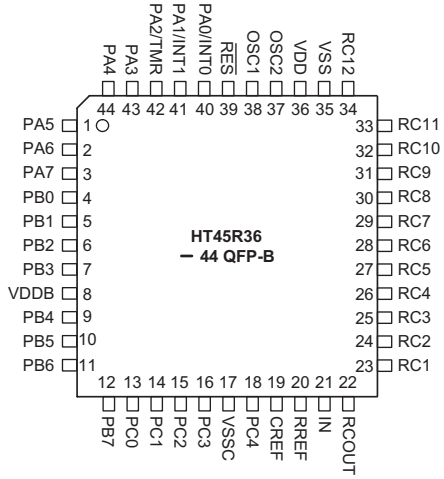
The HT45R36 is an 8-bit high performance, RISC architecture microcontroller device specifically designed for cost-effective multiple I/O control product applications.

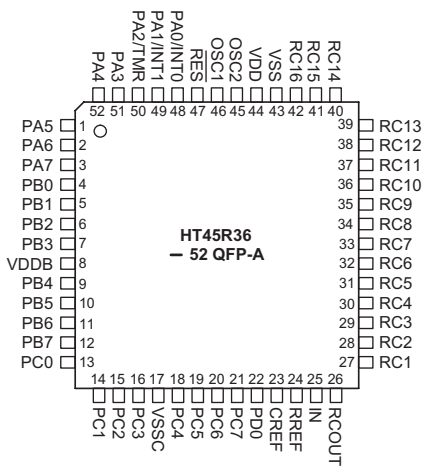
The advantages of low power consumption, I/O flexibility, timer functions, oscillator options, Power Down and wake-up functions, Watchdog Timer, enhance the versatility of these devices to suit a wide range of application possibilities such as industrial control, consumer products, subsystem controllers, etc.

Block Diagram



Pin Assignment





Pin Description

Pin Name	I/O	Options	Description
PA0/INT0 PA1/INT1 PA2/TMR PA3~PA7	I/O	Pull-high* Wake-up	Bidirectional 8-bit I/O port. Each pin can be configured as a wake-up input via configuration options. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. Pull-high resistors can be added to the whole port via a configuration option. Pins PA0 and PA1 are pin-shared with external interrupt input pins INT0 and INT1, respectively. Configuration options determine the interrupt enable/disable and the interrupt low/high trigger type. Pins PA2 is pin-shared with the external timer input pins TMR.
PB0~PB7	I/O	Pull-high	Bidirectional 8-bit input/output port. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. Pull-high resistors can be added to the whole port via a configuration option.
PC0~PC7	I/O	Pull-high	Bidirectional 8-bit input/output port. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. Pull-high resistors can be added to the whole port via a configuration option.
PD0	I/O	Pull-high	Bidirectional 1-bit input/output port. Software instructions determine if the pin is a CMOS output or Schmitt trigger input. A pull-high resistor can be added via a configuration option.
RC1~RC16	I	—	Capacitor or resistor connection pins
RCOUT	I	—	Capacitor or resistor connection pin to RC OSC
IN	I	—	Oscillation input pin
RREF	O	—	Reference resistor connection pin
CREF	O	—	Reference capacitor connection pin
$\overline{RES}$	I	—	Schmitt trigger reset input. Active low
VSS	—	—	Negative power supply, ground
VSSC	—	—	Negative power supply for PC, ground
VDD	—	—	Positive power supply
VDDB	—	—	Positive power supply PB
OSC1 OSC2	I O	Crystal or RC	OSC1, OSC2 are connected to an RC network or Crystal determined by a configuration option, for the internal system clock. In the case of the RC oscillator, OSC2 can be used to monitor the system clock. Its frequency is 1/4 system clock.

Note: *All pull-high resistors are controlled by an option bit.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V

Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V

I_{OL} Total 300mA

Total Power Dissipation 500mW

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –40°C to 85°C

I_{OH} Total ..... –200mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	f_{SYS}=4MHz	2.2	—	5.5	V
			f_{SYS}=8MHz	3.3	—	5.5	V
I_{DD1}	Operating Current (Crystal OSC, RC OSC)	3V	No load, f_{SYS}=4MHz	—	1	2	mA
		5V		—	3	5	mA
I_{DD2}	Operating Current (Crystal OSC, RC OSC)	5V	No load, f_{SYS}=8MHz	—	4	8	mA
I_{STB1}	Standby Current (WDT Enabled)	3V	No load, system HALT	—	—	5	μA
		5V		—	—	10	μA
I_{STB2}	Standby Current (WDT Disabled)	3V	No load, system HALT	—	—	1	μA
		5V		—	—	2	μA
V_{IL1}	Input Low Voltage for I/O Ports, TMR, INT0 and INT1	—	—	0	—	$0.3V_{DD}$	V
V_{IH1}	Input High Voltage for I/O Ports, TMR, INT0 and INT1	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	$0.9V_{DD}$	—	V_{DD}	V
V_{LVR}	Low Voltage Reset	—	LVR enabled	2.7	3.0	3.3	V
I_{OL1}	PA, PB, PD0, RREF and CREF Sink Current	3V	V_{OL}=0.1V_{DD}	4	8	—	mA
		5V		10	20	—	mA
I_{OH1}	PA, PC, PD0, RREF and CREF Source Current	3V	V_{OH}=0.9V_{DD}	–2	–4	—	mA
		5V		–5	–10	—	mA
I_{OL2}	PC Sink Current	3V	V_{OL}=0.1V_{DD}	8	16	—	mA
		5V		20	40	—	mA
I_{OH2}	PB Source Current	3V	V_{OH}=0.9V_{DD}	–4	–8	—	mA
		5V		–10	–20	—	mA
R_{PH}	Pull-high Resistance	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock (Crystal OSC, RC OSC)	—	2.2V~5.5V	400	—	4000	kHz
		—	3.3V~5.5V	400	—	8000	kHz
f_{TIMER}	Timer I/P Frequency	—	2.2V~5.5V	0	—	4000	kHz
		—	3.3V~5.5V	0	—	8000	kHz
t_{WDTOSC}	Watchdog Oscillator Period	3V	—	45	90	180	μs
		5V	—	32	65	130	μs
t_{WDT1}	Watchdog Time-out Period (WDT RC OSC)	3V	Without WDT prescaler	11	23	46	ms
		5V		8	17	33	ms
t_{WDT2}	Watchdog Time-out Period (System Clock/4)	—	Without WDT prescaler	—	1024	—	t_{SYS}
t_{RES}	External Reset Low Pulse Width	—	—	1	—	—	μs
t_{SST}	System Start-up Timer Period	—	Wake-up from HALT	—	1024	—	t_{SYS}
t_{INT}	Interrupt Pulse Width	—	—	1	—	—	μs
t_{LVR}	Low Voltage Reset Time	—	—	0.25	1	2	ms

Functional Description

Execution Flow

The system clock for the microcontroller is derived from either a crystal or an RC oscillator. The system clock is internally divided into four non-overlapping clocks. One instruction cycle consists of four system clock cycles.

Instruction fetching and execution are pipelined in such a way that a fetch takes an instruction cycle while decoding and execution takes the next instruction cycle. However, the pipelining scheme causes each instruction to effectively execute in a cycle. If an instruction changes the program counter, two cycles are required to complete the instruction.

Program Counter – PC

The program counter (PC) controls the sequence in which the instructions stored in program ROM are executed and its contents specify full range of program memory.

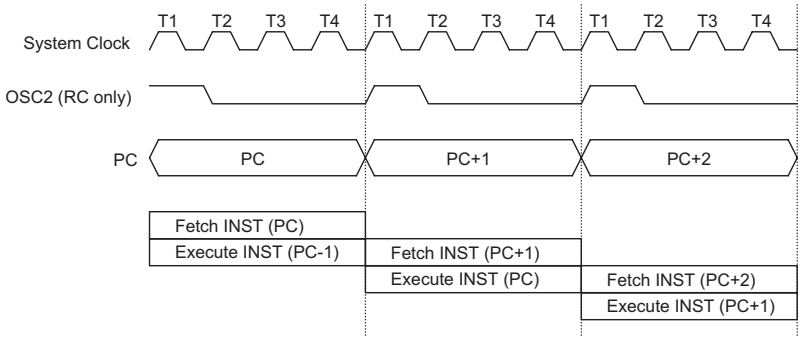
After accessing a program memory word to fetch an instruction code, the contents of the program counter are incremented by one. The program counter then points to the memory word containing the next instruction code.

When executing a jump instruction, a conditional skip execution, loading the PCL register, a subroutine call, an initial reset, an internal interrupt, an external interrupt or return from a subroutine, the PC manipulates the program transfer by loading the address corresponding to each instruction.

The conditional skip is activated by instructions. Once the condition is met, the next instruction, fetched during the current instruction execution, is discarded and a dummy cycle replaces it to get the proper instruction. Otherwise the program will proceed with the next instruction.

The lower byte of the program counter (PCL) is a readable and writable register (06H). Moving data into the PCL performs a short jump. The destination must be within the current Program Memory Page.

When a control transfer takes place, an additional dummy cycle is required.



Execution Flow

Mode	Program Counter										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
Initial Reset	0	0	0	0	0	0	0	0	0	0	0
External Interrupt 0	0	0	0	0	0	0	0	0	1	0	0
External Interrupt 1	0	0	0	0	0	0	0	1	0	0	0
Timer/Event Counter Overflow	0	0	0	0	0	0	0	1	1	0	0
External RC Oscillation Converter Interrupt	0	0	0	0	0	0	1	0	0	0	0
Skip	Program Counter+2										
Loading PCL	*10	*9	*8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, Call Branch	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from Subroutine	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Program Counter

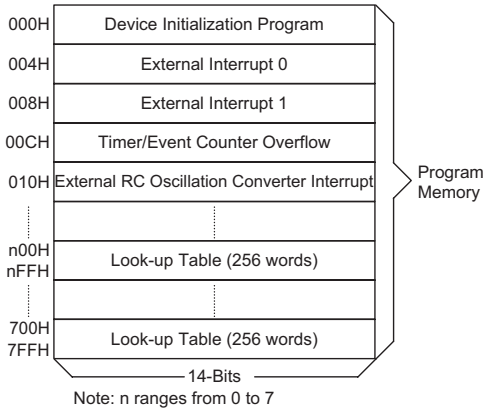
Note: *10~*0: Program Counter bits
#10~#0: Instruction code bits
S10~S0: Stack register bits
@7~@0: PCL bits

Program Memory – ROM

The program memory is used to store the program instructions which are to be executed. It also contains data, table, and interrupt entries, and is organized into 2048×14 bits, addressed by the program counter and table pointer.

Certain locations in the program memory are reserved for special usage:

- Location 000H
  This area is reserved for program initialisation. After a device reset, the program always begins execution at location 000H.
- Location 004H
  This location is reserved for the external interrupt 0 service program. If the INT0 input pin is activated, the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Location 008H
  This location is reserved for the external interrupt 1 service program. If the INT1 input pin is activated, the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Location 00CH
  This location is reserved for the Timer/Event Counter interrupt service program. If a Timer interrupt results from a Timer/Event Counter overflow, and the interrupt is enabled and the stack is not full, the program begins execution at this location.



Note: n ranges from 0 to 7

Program Memory

- Location 010H
  This location is reserved for the external RC oscillation converter interrupt service program. If an external RC oscillation converter interrupt results from an external RC oscillation converter interrupt is activated, and the interrupt is enabled and the stack is not full, the program begins execution at this location.
- Table location
  Any location in the program memory can be used as a look-up table. The instructions "TABRDC [m]" (the current page, 1 page=256 words) and "TABRDL [m]" transfer the contents of the lower-order byte to the specified data memory, and the higher-order byte to TBLH (08H). Only the destination of the lower-order byte in the table is well-defined, the other bits of the table word are transferred to the lower portion of TBLH, and the remaining 2 bits are read as "0". The Table Higher-order byte register (TBLH) is read only. The table pointer (TBLP) is a read/write register (07H), which indicates the table location. Before accessing the table, the location must be placed in TBLP. The TBLH is read only and cannot be restored. If the main routine and the ISR (Interrupt Service Routine) both employ the table read instruction, the contents of the TBLH in the main routine are likely to be changed by the table read instruction used in the ISR. Errors may therefore occur. In other words, using the table read instruction in the main routine and also in the ISR should be avoided. However, if the table read instruction has to be used in both the main routine and in the ISR, the interrupt should be disabled prior to the table read instruction execution. The interrupt should not be re-enabled until the TBLH has been backed up. All table related instructions require two cycles to complete the operation. These areas may function as normal program memory depending upon the requirements.

Stack Register – STACK

This is a special part of the memory which is used to save the contents of the program counter only. The stack is organised into 4-levels and is neither part of the data nor part of the program space, and is neither readable nor writable. The activated level is indexed by the stack pointer (SP) and is neither readable nor writeable. At a subroutine call or interrupt acknowledgment, the contents of the program counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled

Instruction	Table Location										
	*10	*9	*8	*7	*6	*5	*4	*3	*2	*1	*0
TABRDC [m]	P10	P9	P8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	1	@7	@6	@5	@4	@3	@2	@1	@0

Table Location

Note: *10~*0: Table location bits

P10~P8: Current program counter bits

@7~@0: Table pointer bits

by a return instruction, RET or RETI, the program counter is restored to its previous value from the stack. After a device reset, the SP will point to the top of the stack.

If the stack is full and a non-masked interrupt takes place, the interrupt request flag will be recorded but the acknowledgment will be inhibited. When the stack pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. In a similar case, if the stack is full and a "CALL" is subsequently executed, stack overflow occurs and the first entry will be lost as only the most recent 4 return addresses are stored.

Data Memory – RAM

The data memory has a capacity of 150×8 bits. The data memory is divided into two functional groups: special function registers and general purpose data memory (120×8). Most are read/write, but some are read only. The general purpose data memory, addressed from 28H to 7FH at Bank 0 and from 40H to 5FH at Bank 1, is used for data and control information under instruction commands.

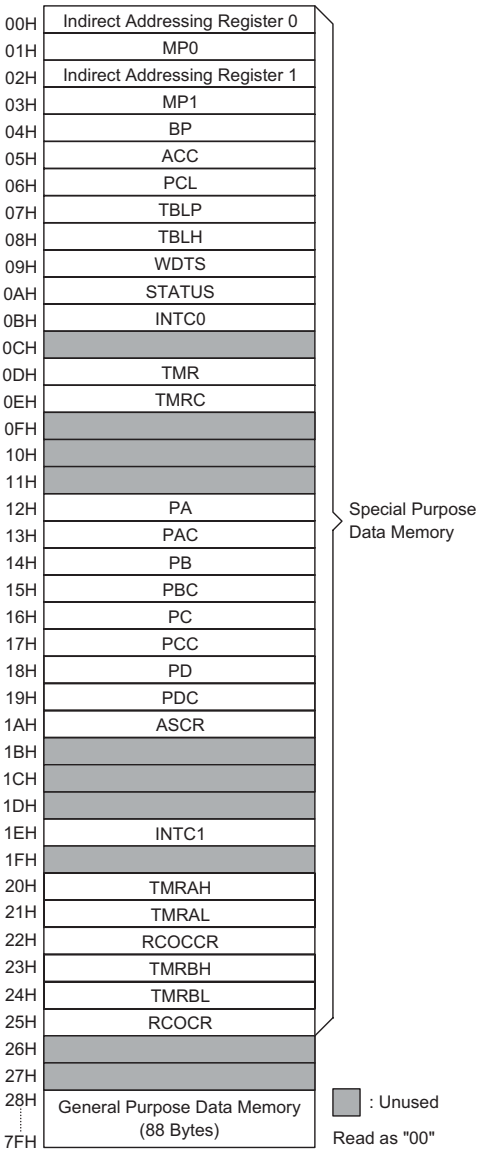
All of the data memory areas can handle arithmetic, logic, increment, decrement and rotate operations directly. Except for some dedicated bits, each bit in the data memory can be set and reset by the "SET [m].i" and "CLR [m].i" bit manipulation instructions. They are also indirectly accessible through the memory pointer registers (MP0;01H, MP1;02H).

Bank 1 must be addressed indirectly using the memory pointer MP1 and the indirect addressing register IAR1. Any direct addressing or any indirect addressing using MP0 and IAR0 will always result in data from Bank 0 being accessed.

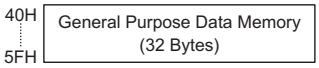
Indirect Addressing Register

The method of indirect addressing allows data manipulation using memory pointers instead of the usual direct memory addressing method where the actual memory address is defined. Any action on the indirect addressing registers will result in corresponding read/write operations to the memory location specified by the corresponding memory pointers. This device contains two indirect addressing registers known as IAR0 and IAR1 and two memory pointers MP0 and MP1. Note that these indirect addressing registers are not physically implemented and that reading the indirect addressing registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

The two memory pointers, MP0 and MP1, are physically implemented in the data memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data.



RAM Mapping Bank 0



RAM Mapping Bank 1

When any operation to the relevant indirect addressing registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related memory pointer.

Bit 7 of the memory pointers are not implemented. However, it must be noted that when the memory pointers in this device is read, a value of "1" will be read.

Bank Pointer – BP

When using instructions to access the general purpose data memory in Bank 0 or Bank 1, it is necessary to ensure that the correct area is selected. The general purpose data memory is sub-divided into two banks, Bank 0 and Bank 1 for this device. Selecting the correct data memory area is achieved by using the bank pointer. If data in Bank 0 or Bank 1 is to be accessed, the BP must be set to the values ″00H″ or ″01H″ respectively, however, it must be noted that data in Bank 1 can only be addressed indirectly using the MP1 memory pointer and the IAR1 indirect addressing register.

Any direct addressing or any indirect addressing using MP0 and IAR0 will always result in data from Bank 0 being accessed. The data memory is initialized to Bank 0 after a reset, except for the WDT time-out reset in the Power Down Mode, in which case, the data memory bank remains unchanged.

It should be noted that the special function data memory is not affected by the bank selection, which means that the special function registers can be accessed from within either Bank 0 or Bank 1.

Accumulator

The accumulator is closely related to ALU operations. It is also mapped to location ″05H″ of the data memory and can carry out immediate data operations. The data movement between two data memory locations must pass through the accumulator.

Arithmetic and Logic Unit – ALU

This circuit performs 8-bit arithmetic and logic operations. The ALU provides the following functions:

- Arithmetic operations (ADD, ADC, SUB, SBC, DAA)
- Logic operations (AND, OR, XOR, CPL)
- Rotation (RL, RR, RLC, RRC)
- Increment and Decrement (INC, DEC)
- Branch decision (SZ, SNZ, SIZ, SDZ ....)

The ALU not only saves the results of a data operation but also changes the status register.

Status Register – STATUS

This 8-bit register (0AH) contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). It also records the status information and controls the operation sequence.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition operations related to the status register may give different results from those intended. The TO flag can be affected only by a system power-up, a WDT time-out or executing the ″CLR WDT″ or ″HALT″ instruction.

The PDF flag can be affected only by executing a ″HALT″ or ″CLR WDT″ instruction or a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

In addition, on entering the interrupt sequence or executing the subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status are important and if the subroutine can corrupt the status register, precautions must be taken to save it properly.

Bit No.	Label	Function
0	C	C is set if the operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
1	AC	AC is set if the operation results in a carry out of the low nibbles in addition or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
2	Z	Z is set if the result of an arithmetic or logic operation is zero; otherwise Z is cleared.
3	OV	OV is set if the operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
4	PDF	PDF is cleared by system power-up or executing the ″CLR WDT″ instruction. PDF is set by executing the ″HALT″ instruction.
5	TO	TO is cleared by system power-up or executing the ″CLR WDT″ or ″HALT″ instruction. TO is set by a WDT time-out.
6~7	—	Unused bit, read as ″0″

Status (0AH) Register

Interrupt

The devices provides two external interrupts, one internal 8-bit timer/event counter interrupt and one external RC oscillation converter interrupt. The interrupt control register 0 (INTC0;0BH) and interrupt control register 1 (INTC1;1EH) both contain the interrupt control bits that are used to set the enable/disable and interrupt request flags.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked, by clearing the EMI bit. This scheme may prevent further interrupt nesting. Other interrupt requests may happen during this interval but only the interrupt request flag is recorded. If a certain interrupt requires servicing within the service routine, the EMI bit and the corresponding bit of the INTC0 and INTC1 registers may be set to allow interrupt nesting.

If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the SP is decremented. If immediate service is desired, the stack must be prevented from becoming full.

All interrupts have a wake-up capability. As an interrupt is serviced, a control transfer occurs by pushing the program counter onto the stack, followed by a branch to a subroutine at a specified location in the program memory. Only the program counter is pushed onto the stack. If the contents of the accumulator or status register are altered by the interrupt service program, this may corrupt the desired control sequence, therefore their contents should be saved in advance.

External interrupts are triggered by an edge transition on pins INT0 or INT1. A configuration option enables these pins as interrupts and selects if they are active on high to low or low to high transitions. If active their related interrupt request flag, EIF0; bit 4 in INTC0, and EIF1; bit 5 in INTC0, will be set. After the interrupt is enabled, the stack is not full, and the external interrupt is active, a subroutine call to location ″04H″ or ″08H″ will occur. The interrupt request flags, EIF0 or EIF1, and the EMI bit will all be cleared to disable other interrupts.

The internal Timer/Event Counter interrupt is initialised by setting the Timer/Event Counter interrupt request flag, TF; bit 6 in INTC0. A timer interrupt will be generated when the timer overflows. After the interrupt is enabled, and the stack is not full, and the TF bit is set, a subroutine call to location ″0CH″ will occur. The related interrupt request flag, TF, is reset, and the EMI bit is cleared to disable other interrupts.

The external RC oscillation converter interrupt is initialized by setting the external RC oscillation converter interrupt request flag, RCOCF; bit 4 of INTC1. This is caused by a Timer A or Timer B overflow. When the interrupt is enabled, and the stack is not full and the RCOCF bit is set, a subroutine call to location ″10H″ will occur. The related interrupt request flag, RCOCF, will be reset and the EMI bit cleared to disable further interrupts.

During the execution of an interrupt subroutine, other interrupt acknowledgments are held until the ″RETI″ instruction is executed or the EMI bit and the related interrupt control bit are set to 1, if the stack is not full. To return from the interrupt subroutine, a ″RET″ or ″RETI″ instruction may be invoked. RETI will set the EMI bit to enable an interrupt service, but RET will not.

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In the case of simultaneous requests the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

No.	Interrupt Source	Priority	Vector
a	External Interrupt 0	1	04H
b	External Interrupt 1	2	08H
c	Timer/Event Counter Overflow	3	0CH
d	External RC Oscillation Converter Interrupt	4	10H

Interrupt Priority

The Timer/Event Counter interrupt request flag, TF, external interrupt 1 request flag, EIF1, external interrupt 0 request flag, EIF0, enable Timer/Event Counter interrupt bit, ETI, enable external interrupt 1 bit, EEI1, enable external interrupt 0 bit, EEI0, and enable master interrupt bit, EMI, form the interrupt control register 0, INTC0, which is located at ″0BH″ in the RAM.

The external RC oscillation converter interrupt request flag, RCOCF, enable external RC oscillation converter interrupt bit, ERCOCI, form the interrupt control register 1 (INTC1) which is located at ″1EH″ in the RAM.

EMI, EEI0, EEI1, ETI and ERCOCI are all used to control the enable/disable status of interrupts. These bits prevent the requested interrupt from being serviced. Once the interrupt request flags, TF, RCOCF, EIF1 and EIF0, are all set, they remain in the INTC1 or INTC0 registers respectively until the interrupts are serviced or cleared by a software instruction.

It is recommended that a program does not use the ″CALL subroutine″ within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and enabling the interrupt is not well controlled, the original control sequence may be damaged once the ″CALL″ is executed in the interrupt subroutine.

Bit No.	Label	Function
0	EMI	Controls the master (global) interrupt (1= enabled; 0= disabled)
1	EEI0	Controls the external interrupt 0 (1= enabled; 0= disabled)
2	EEI1	Controls the external interrupt 1 (1= enabled; 0= disabled)
3	ETI	Controls the Timer/Event Counter interrupt (1= enabled; 0= disabled)
4	EIF0	External interrupt 0 request flag (1= active; 0= inactive)
5	EIF1	External interrupt 1 request flag (1= active; 0= inactive)
6	TF	Internal Timer/Event Counter request flag (1= active; 0= inactive)
7	—	Unused bit, read as "0"

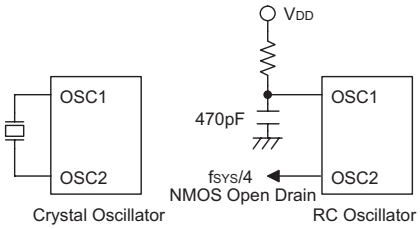
INTC0 (0BH) Register

Bit No.	Label	Function
0	ERCOCI	Controls the external RC oscillation converter interrupt (1= enabled; 0= disabled)
1~3, 5~7	—	Unused bit, read as "0"
4	RCOCF	External RC oscillation converter request flag (1= active; 0= inactive)

INTC1 (1EH) Register

Oscillator Configuration

There are two oscillator circuits in the microcontroller.



System Oscillator

Both are designed for system clocks, namely the RC oscillator and the Crystal oscillator, the choice of which is determined by a configuration option. When the device enters the Power Down Mode, the system oscillator will stop running and will ignore external signals to conserve power.

If an RC oscillator is used, an external resistor between OSC1 and VDD is required to produce oscillation. The resistance must range from 24kΩ to 1MΩ. The system clock, divided by 4, is available on OSC2, which can be used to synchronize external logic. The RC oscillator provides the most cost effective solution, however, the frequency of oscillation may vary with VDD, temperatures and the device itself due to process variations. It is, therefore, not suitable for timing sensitive operations where an accurate oscillator frequency is desired.

If the Crystal oscillator is used, a crystal across OSC1 and OSC2 is needed to provide the feedback and phase shift required for the oscillator. No other external components are required. Instead of a crystal, a resonator can also be connected between OSC1 and OSC2 to get a frequency reference, but two external capacitors connected between OSC1, OSC2 and ground are required, if the oscillator frequency is less than 1MHz.

The WDT oscillator is a free running on-chip RC oscillator which requires no external components. Even if the system enters the Power Down Mode, where the system clock is stopped, the WDT oscillator will continue to operate with a period of approximately 65μs at 5V. The WDT oscillator can be disabled by a configuration option to conserve power.

Watchdog Timer – WDT

The WDT clock can be sourced from its own dedicated internal oscillator (WDT oscillator), or from the or instruction clock, which is the system clock divided by 4. The choice is determined via a configuration option. The WDT timer is designed to prevent a software malfunction or sequence from jumping to an unknown location with unpredictable results. The Watchdog Timer can be disabled by a configuration option. If the Watchdog Timer is disabled, any executions related to the WDT result in no operation.

The WDT clock source is first divided by 256. If the internal WDT oscillator is used ,this gives a nominal time-out period of approximately 17ms at 5V. This time-out period may vary with temperatures, VDD and process variations. By using the WDT prescaler, longer time-out periods can be realised. Writing data to the WS2, WS1, WS0 bits in the WDTS register, can give different time-out periods. If WS2, WS1, and WS0 are all equal to 1, the division ratio will be 1:128, and the maximum time-out period will be 2.1s at 5V. If the internal WDT os-

cillator is disabled, the WDT clock may still come from the instruction clock and operate in the same manner except that in the Power Down state the WDT will stop counting and lose its protecting purpose. In this situation the logic can only be restarted by external logic. The high nibble and bit 3 of the WDTS can be used for user defined flags.

If the device operates in a noisy environment, using the internal WDT oscillator is the recommended choice, since the HALT instruction will stop the system clock.

WS2	WS1	WS0	Division Ratio
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

WDTS (09H) Register

The WDT overflow under normal operation will generate a ″chip reset″ and set the status bit ″TO″. But in the Power Down mode, the overflow will generate a ″warm reset″, where only the Program Counter and SP are reset to zero. To clear the contents of the WDT, including the WDT prescaler, three methods can be used; an external reset (a low level to RES), a software instruction and a ″HALT″ instruction. The software instruction includes ″CLR WDT″ instruction and the instruction pair – ″CLR WDT1″ and ″CLR WDT2″. Of these two types of instruction, only one can be active depending on the configuration option – ″CLR WDT times selection option″. If the ″CLR WDT″ is selected, i.e. CLRWDT times equal one, any execution of the ″CLR WDT″ instruction will clear the WDT. In the case that ″CLR WDT1″ and ″CLR WDT2″ are chosen, i.e. CLRWDT times equal two, these two instructions must be executed to clear the WDT; otherwise, the WDT may reset the chip as a result of a time-out.

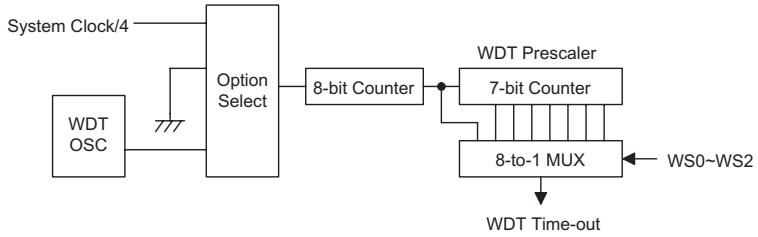
Power Down Operation – HALT

The Power Down mode is initialized by the ″HALT″ instruction and results in the following...

- The system oscillator will be turned off but the WDT oscillator keeps running, if the internal WDT oscillator has been selected as the WDT source clock.
- The contents of the on chip RAM and registers remain unchanged.
- The WDT and WDT prescaler will be cleared and will resume counting, if the internal WDT oscillator has been selected as the WDT source clock
- All of the I/O ports will maintain their original status.
- The PDF flag is set and the TO flag is cleared.

The system can leave the Power Down mode by means of an external reset, an interrupt, an external falling edge signal on port A or a WDT overflow. An external reset causes a device initialisation and the WDT overflow performs a ″warm reset″. After the TO and PDF flags are examined, the reason for chip reset can be determined. The PDF flag is cleared by a system power-up or executing the ″CLR WDT″ instruction and is set when executing the ″HALT″ instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the program counter and SP; the other registers maintain their their original status.

The port A and interrupt methods of wake-up can be considered as a continuation of normal execution. Each bit in port A can be independently selected by configuration options to wake-up the device. When awakened from an I/O port stimulus, the program will resume execution at the next instruction. If it is awakened due to an interrupt, two sequences may happen. If the related interrupt is disabled or the interrupt is enabled but the stack is full, the program will resume execution at the next instruction. If the interrupt is enabled and the stack is not full, the regular interrupt response takes place. If an interrupt request flag is set to ″1″ before entering the Power Down mode, the wake-up function of the related interrupt will be disabled. Once a wake-up event occurs, it takes 1024 t_{SYS} (system clock periods) to resume normal operation. In other words, a dummy period will be inserted after wake-up. If the wake-up results from an interrupt acknowledgment, the actual interrupt subrou-



Watchdog Timer

tine execution will be delayed by one or more cycles. If the wake-up results in the next instruction execution, this will be executed immediately after the dummy period is finished.

To minimise power consumption, all the I/O pins should be carefully managed before entering the Power Down mode.

Reset

There are three ways in which a reset can occur:

- $\overline{RES}$ reset during normal operation
- $\overline{RES}$ reset during HALT
- WDT time-out reset during normal operation

A WDT time-out, when the device is in the Power Down mode, is different from other device reset conditions, in that it can perform a "warm reset" that resets only the Program Counter and the SP, leaving the other circuits in their original state. Some registers remain unchanged during other reset conditions. Most registers are reset to their "initial condition" when the reset conditions are met. By examining the PDF and TO flags, the program can distinguish between the different device reset types.

TO	PDF	RESET Conditions
0	0	$\overline{RES}$ reset during power-up
u	u	$\overline{RES}$ reset during normal operation
0	1	$\overline{RES}$ wake-up HALT
1	u	WDT time-out during normal operation
1	1	WDT wake-up HALT

Note: "u" means "unchanged"

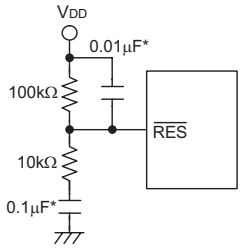
To guarantee that the system oscillator is started and stabilised, the SST or System Start-up Timer, provides an extra-delay of 1024 system clock pulses when the system is reset (power-up, WDT time-out or $\overline{RES}$ reset) or when the system awakens from a Power Down state.

When a system reset occurs, the SST delay is added during the reset period. Any wake-up from HALT will enable the SST delay.

An extra option load time delay is added during a system reset (power-up, WDT time-out at normal mode or $\overline{RES}$ reset).

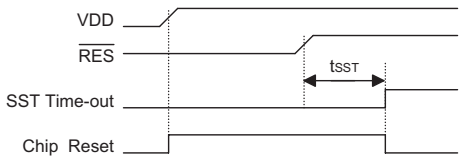
The functional unit device reset status are shown below.

Program Counter	000H
Interrupt	Disable
Prescaler	Clear
WDT	Clear. After master reset, WDT begins counting
Timer/Event Counter	Off
Input/Output Ports	Input mode
Stack Pointer	Points to the top of the stack

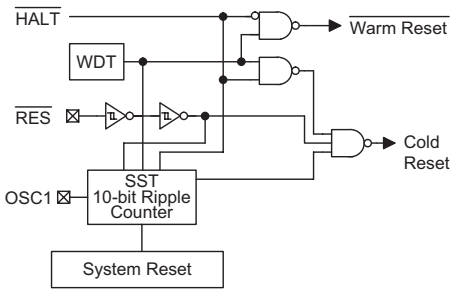


Reset Circuit

Note: "*" Make the length of the wiring, which is connected to the $\overline{RES}$ pin as short as possible, to avoid noise interference.



Reset Timing Chart



Reset Configuration

The states of the registers is summarized in the table.

Register	Reset (Power-on)	WDT Time-out (Normal Operation)	$\overline{RES}$ Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*
MP0	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu	-uuu uuuu
MP1	-xxx xxxx	-uuu uuuu	-uuu uuuu	-uuu uuuu	-uuu uuuu
BP	---- ---0	---- ---0	---- ---0	---- ---0	---- ---0
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
Program Counter	000H	000H	000H	000H	000H
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	--xx xxxx	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu
WDTS	0000 0111	0000 0111	0000 0111	0000 0111	uuuu uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu
TMR	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRC	00-0 1000	00-0 1000	00-0 1000	00-0 1000	uu-u uuuu
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PCC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PD	---- ---1	---- ---1	---- ---1	---- ---1	---- ---u
PDC	---- ---1	---- ---1	---- ---1	---- ---1	---- ---u
ASCR	---1 1111	---1 1111	---1 1111	---1 1111	---u uuuu
INTC1	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u
TMRAH	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRAL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
RCOCCR	0000 1---	0000 1---	0000 1---	0000 1---	uuuu u---
TMRBH	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRBL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
RCOCR	1xxx --00	1xxx --00	1xxx --00	1xxx --00	uuuu --uu

Note: "*" means "warm reset"
"u" means "unchanged"
"x" means "unknown"

Timer/Event Counter

An 8-bit timer/event counter, known as Timer/Event Counter, is implemented in the microcontroller. The Timer/Event Counter contains an 8-bit programmable count-up counter whose clock may come from an external source or from the system clock. Using the external clock input allows the user to count external events, measure time internals or pulse widths, or generate an accurate time base. Using the internal clock allows the user to generate an accurate time base.

There are 2 registers related to the Timer/Event Counter, TMR (0DH) and TMRC (0EH). Two physical registers are mapped to TMR location; writing to TMR places the start value be placed in the Timer/Event Counter preload register while reading TMR retrieves the contents of the Timer/Event Counter. The TMRC is a timer/event counter control register, which defines the timer operating conditions.

The TM0, TM1 bits define the operating mode. The event count mode is used to count external events, which means the clock source comes from an external TMR pin. The timer mode functions as a normal timer with the clock source coming from the f_{INT} clock. The pulse width measurement mode can be used to measure the high or low level duration of an external signal on the TMR pin. The counting is based on the f_{INT} clock source. In the event counting or timer mode, once the timer/event counter starts counting, it will count from the current contents in the Timer/Event Counter to FFH. Once overflow occurs, the counter is reloaded from the Timer/Event Counter preload register and generates an interrupt request flag (TF; bit 5 of INTC0) at the same time.

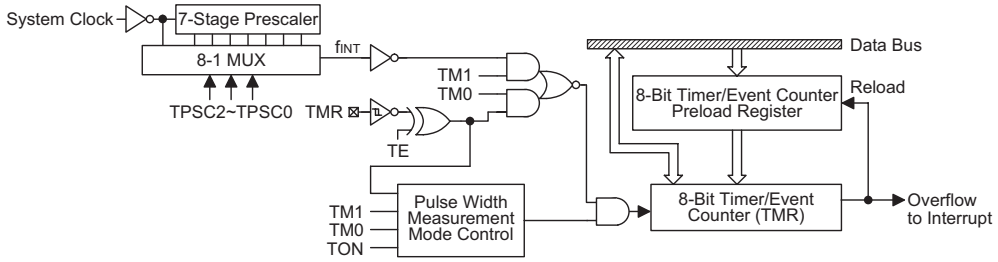
In the pulse width measurement mode, with the TON and bits equal to one, once the TMR has received a transient from low to high, or high to low if the bit is ″0″, it will start counting until the TMR pin returns to its original level and resets the TON bit. The measured result will remain in the Timer/Event Counter even if the activated transient occurs again. In other words, only a single shot measurement can be made. The TON bit must be set again by software for further measurements to be made. Note that, in this operating mode, the Timer/Event Counter starts counting not according to the logic level but according to the transient edges. In the case of counter overflows, the counter is reloaded from the Timer/Event Counter preload register and issues an interrupt request just like the other two modes.

To enable the counting operation, the Timer ON bit, TON; bit 4 of TMRC, should be set to ″1″. In the pulse width measurement mode, the TON will be cleared automatically after the measurement cycle is completed. But in the other two modes the RCOCON can only be reset by instructions. The overflow of the Timer/Event Counter is one of the wake-up sources. No matter what the operation mode is, writing a 0 to ETI can disable the interrupt service.

In the case of a Timer/Event Counter OFF condition, writing data to the Timer/Event Counter preload register will also reload that data to the Timer/Event Counter. But if the Timer/Event Counter is already running, data written to it will only be loaded into the Timer/Event Counter preload register. The Timer/Event Counter will continue to operate until an overflow occurs. When the Timer/Event Counter is read, the clock will be blocked to avoid errors. As clock blocking may results in a counting error, this must be taken into consideration by the programmer. Bit0~Bit2 of the TMRC can be used to define the pre-scaling stages of the internal clock sources of Timer/Event Counter. The definitions are as shown.

Bit No.	Label	Function
0~2	TPSC0~TPSC2	To define the prescaler stages, TPSC2, TPSC1, TPSC0= 000: $f_{INT}=f_{SYS}$ 001: $f_{INT}=f_{SYS}/2$ 010: $f_{INT}=f_{SYS}/4$ 011: $f_{INT}=f_{SYS}/8$ 100: $f_{INT}=f_{SYS}/16$ 101: $f_{INT}=f_{SYS}/32$ 110: $f_{INT}=f_{SYS}/64$ 111: $f_{INT}=f_{SYS}/128$
3	TE	To define the TMR active edge of the timer/event counter (0=active on low to high; 1=active on high to low)
4	TON	To enable or disable timer counting (0=disabled; 1=enabled)
5	—	Unused bit, read as ″0″
6 7	TM0 TM1	To define the operating mode, TM1, TM0= 01=Event count mode (external clock) 10=Timer mode (internal clock) 11=Pulse width measurement mode 00=Unused

TMRC (0EH) Register



Timer/Event Counter

External RC Oscillation Converter

An external RC oscillation mode is implemented in the device. The RC oscillation converter contains two 16-bit programmable count-up counters and the Timer A clock source may come from the system clock or system clock/4. The timer B clock source may come from the external RC oscillator.

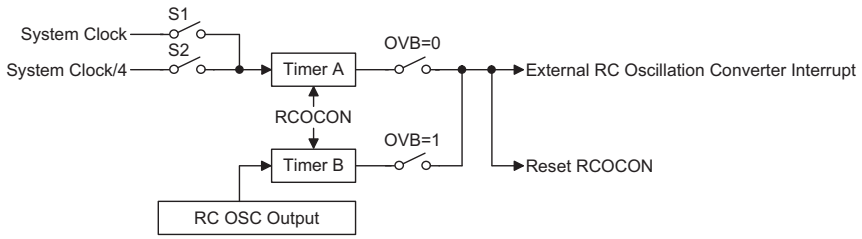
The RC oscillation converter is comprised of the TMRAL, TMRAH, TMRBL, TMRBH registers when the RCO bit, bit 1 of RCOCR register, is "1". The RC oscillation converter Timer B clock source may come from an external RC oscillator. The Timer A clock source comes from the system clock or from the system clock/4, determined by the RCOCCR register.

Bit No.	Label	Function
0~2	—	Unused bit, read as "0"
3	—	Undefined bit, this bit can read/write
4	RCOCON	To enable or disable external RC oscillation converter counting (0= disabled; 1= enabled)
5 6 7	RCOM0 RCOM1 RCOM2	To define the Timer A clock source, RCOM2, RCOM1, RCOM0= 000= System clock 001= System clock/4 010= Unused 011= Unused 100= Unused 101= Unused 110= Unused 111= Unused

RCOCCR (22H) Register

Bit No.	Label	Function
0	OVB	In the RC oscillation converter mode, this bit is used to define the timer/event counter interrupt, which comes from Timer A overflow or Timer B overflow. (0= Timer A overflow; 1= Timer B overflow)
1	RCO	Define RC oscillation converter mode. (0= Disable RC oscillation converter mode; 1= Enable RC oscillation converter mode)
2~3	—	Unused bit, read as "0"
4~7	RW	4-bit read/write registers for user defined.

RCOCR (25H) Register



External RC Oscillation Converter

There are six registers related to the RC oscillation converter, i.e., TMRAH, TMRAL, RCOCCR, TMRBH, TMRBL and RCOCR. The internal timer clock is the input to TMRAH and TMRAL, the external RC oscillation is the input to TMRBH and TMRBL. The OVB bit, bit 0 of RCOCR register, decides whether Timer A overflows or Timer B overflows, then the RCOCF bit is set and an external RC oscillation converter interrupt occurs. When the RC oscillation converter mode Timer A or Timer B overflows, the RCOCON bit is reset to ″0″ and stops counting. Writing to TMRAH/TMRBH places the start value in Timer A/Timer B while reading TMRAH/TMRBH obtains the contents of Timer A/Timer B. Writing to TMRAL/TMRBL only writes the data into a low byte buffer. However writing to TMRAH/TMRBH will write the data and the contents of the low byte buffer into the Timer A/Timer B (16-bit) simultaneously. Timer A/Timer B is changed by writing to TMRAH/TMRBH but writing to TMRAL/TMRBL will keep the Timer A/Timer B unchanged.

Reading TMRAH/TMRBH will also latch the TMRAL/TMRBL into the low byte buffer to avoid the false timing problem. Reading TMRAL/TMRBL returns the contents of the low byte buffer. In other word, the low byte of Timer A/Timer B can not be read directly. It must read the TMRAH/TMRBH first to ensure that the low byte contents of Timer A/Timer B are latched into the buffer.

The resistor and capacitor form an oscillation circuit and input to TMRBH and TMRBL. The RCOM0, RCOM1 and RCOM2 bits of RCOCCR define the clock source of Timer A. It is recommended that the clock source of Timer A uses the system clock or the instruction clock.

If the RCOCON bit, bit 4 of RCOCCR, is set to ″1″, Timer A and Timer B will start counting until Timer A or Timer B overflows, the timer/event counter will then generate an interrupt request flag which is RCOCF; bit 4 of INTC1. The Timer A and Timer B will stop counting and will reset the RCOCON bit to ″0″ at the same time. If the RCOCON bit is ″1″, TMRAH, TMRAL, TMRBH and TMRBL cannot be read or written.

External RC oscillation converter mode example program - Timer A overflow:

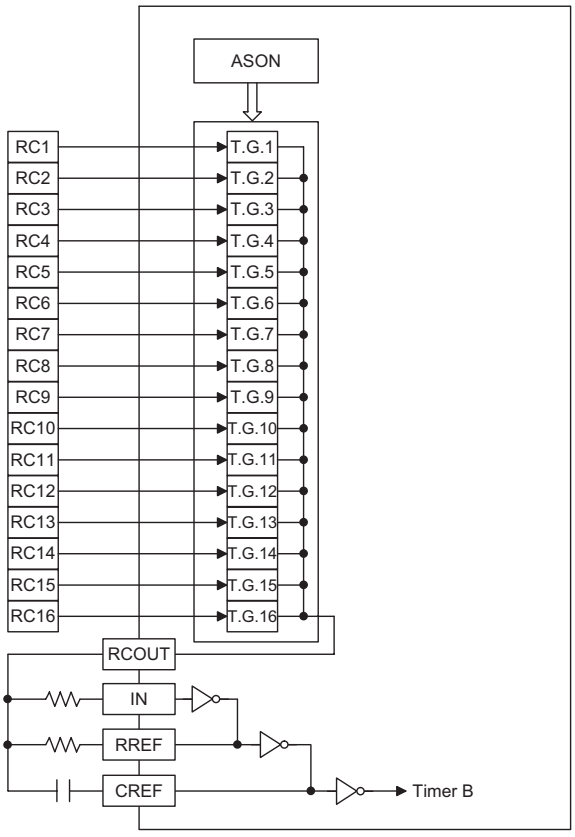
```
clr RCOCCR
mov a, 00000010b                ; Enable External RC oscillation mode and set Timer A overflow
mov RCOCR,a
clr intc1.4                     ; Clear External RC Oscillation Converter interrupt request flag
mov a, low (65536-1000)         ; Give timer A initial value
mov tmral, a                    ; Timer A count 1000 time and then overflow
mov a, high (65536-1000)
mov tmrah, a
mov a, 00h                      ; Give timer B initial value
mov tmrbl, a
mov a, 00h
mov tmrbh, a
mov a, 00110000b                ; Timer A clock source=fSYS/4 and timer on
mov RCOCCR, a
p10:
clr wdt
snz intc1.4                     ; Polling External RC Oscillation Converter interrupt request flag
jmp p10
clr intc1.4                     ; Clear External RC Oscillation Converter interrupt request flag
                                ; Program continue
```

Analog Switch

There are 16 analog switch lines in the microcontroller for RC1~RC16, and a corresponding Analog Switch control register, which is mapped to the data memory of "1AH".

Bit No.	Label	Function
0~4	ASON	Defines the analog switch for RC1~RC16 which is on. ASON= 00000b= Analog switch 1 on, other analog switch off 00001b= Analog switch 2 on, other analog switch off 00010b= Analog switch 3 on, other analog switch off 00011b= Analog switch 4 on, other analog switch off 00100b= Analog switch 5 on, other analog switch off 00101b= Analog switch 6 on, other analog switch off 00110b= Analog switch 7 on, other analog switch off 00111b= Analog switch 8 on, other analog switch off 01000b= Analog switch 9 on, other analog switch off 01001b= Analog switch 10 on, other analog switch off 01010b= Analog switch 11 on, other analog switch off 01011b= Analog switch 12 on, other analog switch off 01100b= Analog switch 13 on, other analog switch off 01101b= Analog switch 14 on, other analog switch off 01110b= Analog switch 15 on, other analog switch off 01111b= Analog switch 16 on, other analog switch off 1xxxxb= All analog switch off and RC OSC always off.
5~7	—	Unused bit, read as "0"

ASCR (1AH) Register



Analog Switch

Input/Output Ports

There are 25 bidirectional input/output lines in the microcontroller, labeled from PA to PD, which are mapped to data memory addresses,12H, 14H, 16H and 18H, respectively. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, that is, the inputs must be ready at the T2 rising edge of the "MOV A,[m]" instruction. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Each I/O line has its own control register, known as PAC, PBC, PCC, PDC, to control the input/output configuration. With this control register, the pin status as either a CMOS output or Schmitt trigger input, but can be reconfigured dynamically, i.e. on-the-fly, under software control. To function as an input, the corresponding bit in the control register must write "1". The input source also depends on the control register. If the control register bit is "1", the input will read the pad state. If the control register bit is "0", the contents of the latches will move to the internal bus. The latter is possible in the "read-modify-write" instruction.

When setup as output the output types are CMOS. These control registers are mapped to locations 13H, 15H, 17H and 19H.

After a device reset, the I/O ports will be initially all setup as inputs, and will therefore be in a high state if the configuration options have selected pull-high resistors, otherwise they will be in a floating condition. Each bit of these input/output latches can be set or cleared by "SET [m].i" and "CLR [m].i" (m=12H, 14H, 16H or 18H) instructions.

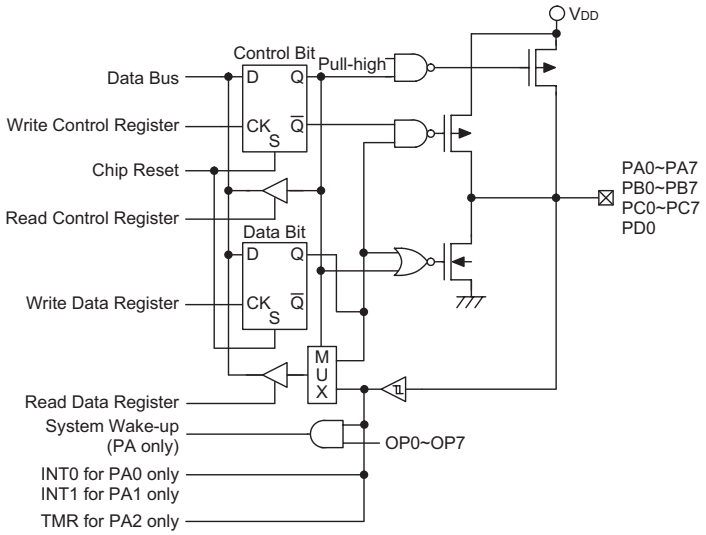
Some instructions first input data and then follow the output operations. For example, "SET [m].i", "CLR [m].i", "CPL [m]", "CPLA [m]" read the entire port states into the CPU, execute the defined operations (bit-operation), and then write the results back to the latches or the accumulator.

Each line of port A has the capability of waking-up the device. The highest 7-bit of port D are not physically implemented; on reading them a "0" is returned whereas writing then results in a no-operation. See Application note.

There are 4 pull-high options available for PA, PB, PC and PD individually. Once the pull-high option is selected, I/O lines have pull-high resistors. Otherwise, the pull-high resistors are absent. It should be noted that a non-pull-high I/O line operating in input mode will cause a floating state.

The PA0, PA1 and PA2 are pin-shared with INT0, INT1 and TMR pins, respectively.

It is recommended that unused or not bonded out I/O lines should be set as output pins by software instruction to avoid consuming power under input floating state.



Input/Output Ports

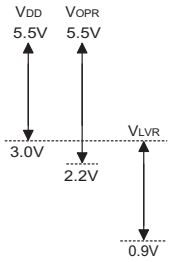
Low Voltage Reset – LVR

The microcontroller provides low voltage reset circuit in order to monitor the supply voltage of the device. If the supply voltage of the device is within the range 0.9V~V_{LVR}, such as when changing a battery, the LVR will automatically reset the device internally.

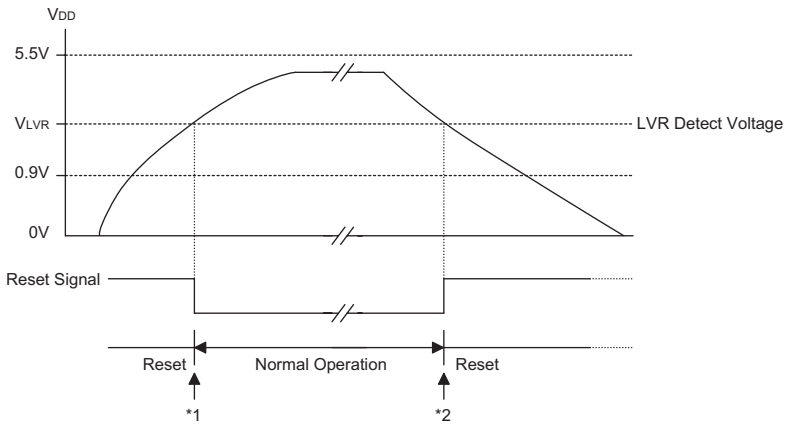
The LVR includes the following specifications:

- The low voltage (0.9V~V_{LVR}) has to remain in its original state for longer than t_{LVR}. If the low voltage state does not exceed t_{LVR}, the LVR will ignore it and will not perform a reset function.
- The LVR uses an "OR" function with the external $\overline{RES}$ signal to perform a chip reset.

The relationship between V_{DD} and V_{LVR} is shown below.



Note: V_{OPR} is the voltage range for proper chip operation at 4MHz system clock.



Low Voltage Reset

Note: *1: To make sure that the system oscillator has stabilized, the SST provides an extra delay of 1024 system clock pulses before starting the normal operation.

*2: Since low voltage has to be maintained its original state for longer than t_{LVR}, therefore a t_{LVR} delay enters the reset mode.

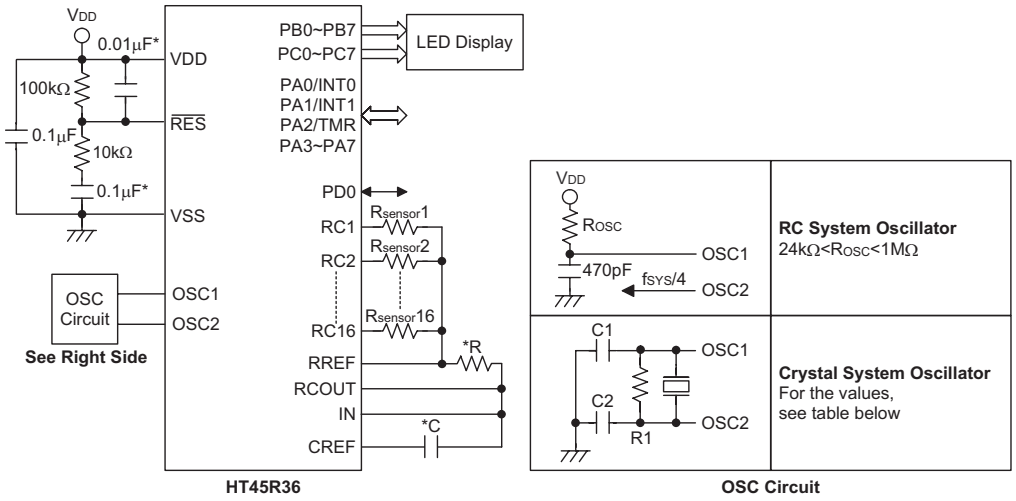
Options

The following table shows all kinds of options in the microcontroller. All of the options must be defined to ensure proper system functioning.

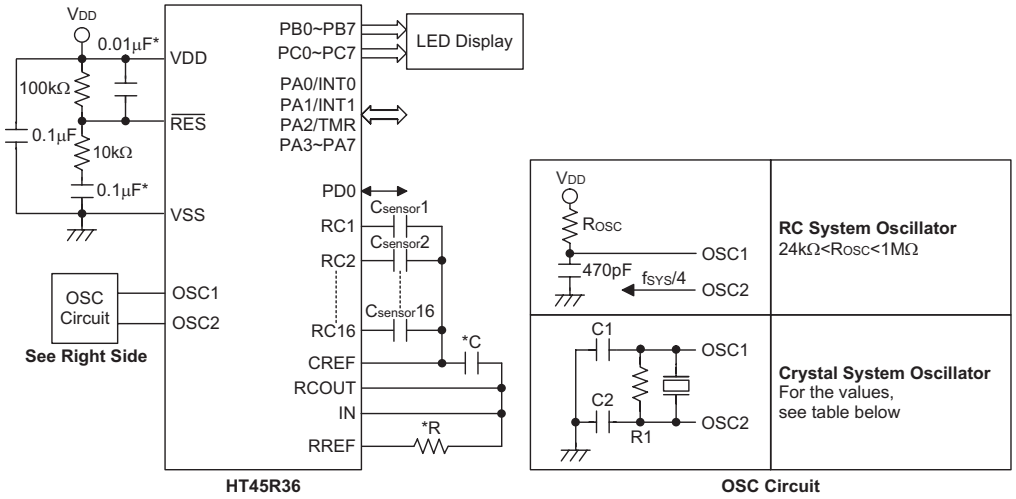
No.	Function	Description
1	Wake-up PA0~PA7 (bit option)	None wake-up or wake-up
2	Pull-high PA0~PA7 (port option)	None pull-high or pull-high
3	Pull-high PB0~PB7 (port option)	None pull-high or pull-high
4	Pull-high PC0~PC7 (port option)	None pull-high or pull-high
5	Pull-high PD0 (bit option)	None pull-high or pull-high
6	WDT clock source	WDTOSC or f_{SYS}/4
7	WDT	Enable or disable
8	CLRWDT	1 or 2 instruction
9	LVR	Disable or enable
10	OSC: X'tal mode or RC mode	X'tal mode or RC mode
11	INT0 trigger edge	Disable, rising edge, falling edge or double edge
12	INT1 trigger edge	Disable, rising edge, falling edge or double edge

Application Circuits

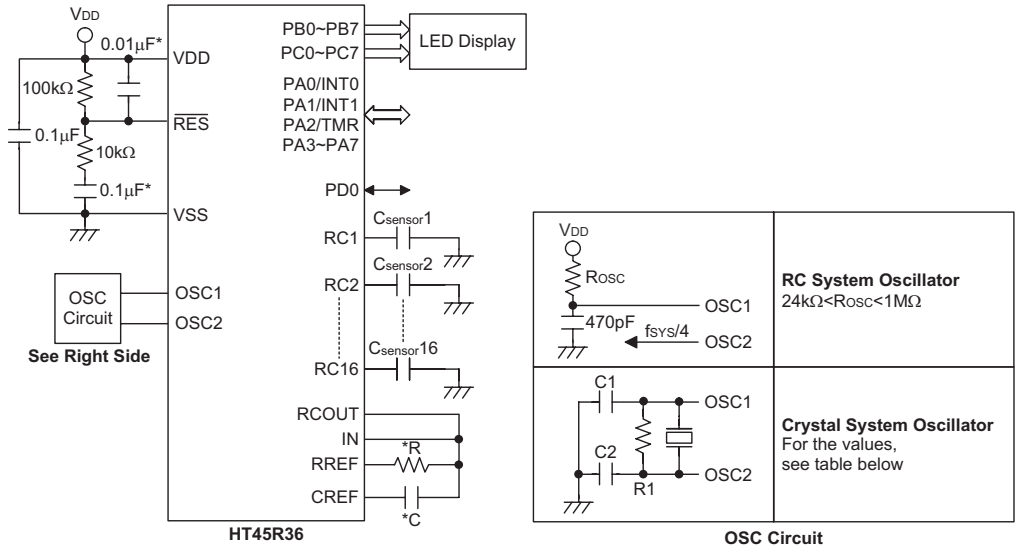
R to F Application Circuit



C to F Application Circuit 1



C to F Application Circuit 2



The following table shows the C1, C2 and R1 values corresponding to the different crystal values. (For reference only)

Crystal or Resonator	C1, C2	R1
4MHz Crystal	10pF	12kΩ
8MHz Crystal	10pF	4.3kΩ
4MHz Resonator	10pF	10kΩ
8MHz Resonator	10pF	4.7kΩ
3.58MHz Crystal	10pF	12kΩ
3.58MHz Resonator	25pF	10kΩ
2MHz Crystal	25pF	15kΩ
2MHz Resonator	35pF	15kΩ
1MHz Crystal	68pF	15kΩ
480kHz Resonator	300pF	12kΩ
455kHz Resonator	300pF	12kΩ
429kHz Resonator	300pF	12kΩ
400kHz Resonator	300pF	12kΩ
The function of the resistor R1 is to ensure that the oscillator will switch off should low voltage conditions occur. Such a low voltage, as mentioned here, is one which is less than the lowest value of the MCU operating voltage. Note however that if the LVR is enabled then R1 can be removed.		

Note: The resistance and capacitance for the reset circuit should be designed in such a way as to ensure that the VDD is stable and remains within a valid operating voltage range before bringing $\overline{RES}$ high.

"*" Make the length of the wiring, which is connected to the $\overline{RES}$ pin as short as possible, to avoid noise interference.

The "*R" resistance and "*C" capacitance should be consideration for the frequency of RC OSC.

$R_{sensor}1$~$R_{sensor}16$ are the resistance sensors.

$C_{sensor}1$~$C_{sensor}16$ are the capacitance sensors.

Instruction Set Summary

Mnemonic	Description	Instruction Cycle	Flag Affected
Arithmetic			
ADD A,[m]	Add data memory to ACC	1	Z,C,AC,OV
ADDM A,[m]	Add ACC to data memory	1(1)	Z,C,AC,OV
ADD A,x	Add immediate data to ACC	1	Z,C,AC,OV
ADC A,[m]	Add data memory to ACC with carry	1	Z,C,AC,OV
ADCM A,[m]	Add ACC to data memory with carry	1(1)	Z,C,AC,OV
SUB A,x	Subtract immediate data from ACC	1	Z,C,AC,OV
SUB A,[m]	Subtract data memory from ACC	1	Z,C,AC,OV
SUBM A,[m]	Subtract data memory from ACC with result in data memory	1(1)	Z,C,AC,OV
SBC A,[m]	Subtract data memory from ACC with carry	1	Z,C,AC,OV
SBCM A,[m]	Subtract data memory from ACC with carry and result in data memory	1(1)	Z,C,AC,OV
DAA [m]	Decimal adjust ACC for addition with result in data memory	1(1)	C
Logic Operation			
AND A,[m]	AND data memory to ACC	1	Z
OR A,[m]	OR data memory to ACC	1	Z
XOR A,[m]	Exclusive-OR data memory to ACC	1	Z
ANDM A,[m]	AND ACC to data memory	1(1)	Z
ORM A,[m]	OR ACC to data memory	1(1)	Z
XORM A,[m]	Exclusive-OR ACC to data memory	1(1)	Z
AND A,x	AND immediate data to ACC	1	Z
OR A,x	OR immediate data to ACC	1	Z
XOR A,x	Exclusive-OR immediate data to ACC	1	Z
CPL [m]	Complement data memory	1(1)	Z
CPLA [m]	Complement data memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment data memory with result in ACC	1	Z
INC [m]	Increment data memory	1(1)	Z
DECA [m]	Decrement data memory with result in ACC	1	Z
DEC [m]	Decrement data memory	1(1)	Z
Rotate			
RRA [m]	Rotate data memory right with result in ACC	1	None
RR [m]	Rotate data memory right	1(1)	None
RRCA [m]	Rotate data memory right through carry with result in ACC	1	C
RRC [m]	Rotate data memory right through carry	1(1)	C
RLA [m]	Rotate data memory left with result in ACC	1	None
RL [m]	Rotate data memory left	1(1)	None
RLCA [m]	Rotate data memory left through carry with result in ACC	1	C
RLC [m]	Rotate data memory left through carry	1(1)	C
Data Move			
MOV A,[m]	Move data memory to ACC	1	None
MOV [m],A	Move ACC to data memory	1(1)	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of data memory	1(1)	None
SET [m].i	Set bit of data memory	1(1)	None

Mnemonic	Description	Instruction Cycle	Flag Affected
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if data memory is zero	1(2)	None
SZA [m]	Skip if data memory is zero with data movement to ACC	1(2)	None
SZ [m].i	Skip if bit i of data memory is zero	1(2)	None
SNZ [m].i	Skip if bit i of data memory is not zero	1(2)	None
SIZ [m]	Skip if increment data memory is zero	1(3)	None
SDZ [m]	Skip if decrement data memory is zero	1(3)	None
SIZA [m]	Skip if increment data memory is zero with result in ACC	1(2)	None
SDZA [m]	Skip if decrement data memory is zero with result in ACC	1(2)	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read			
TABRDC [m]	Read ROM code (current page) to data memory and TBLH	2(1)	None
TABRDL [m]	Read ROM code (last page) to data memory and TBLH	2(1)	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear data memory	1(1)	None
SET [m]	Set data memory	1(1)	None
CLR WDT	Clear Watchdog Timer	1	TO,PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO(4),PDF(4)
CLR WDT2	Pre-clear Watchdog Timer	1	TO(4),PDF(4)
SWAP [m]	Swap nibbles of data memory	1(1)	None
SWAPA [m]	Swap nibbles of data memory with result in ACC	1	None
HALT	Enter Power Down Mode	1	TO,PDF

Note: x: Immediate data

m: Data memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

√: Flag is affected

–: Flag is not affected

(1): If a loading to the PCL register occurs, the execution cycle of instructions will be delayed for one more cycle (four system clocks).

(2): If a skipping to the next instruction occurs, the execution cycle of instructions will be delayed for one more cycle (four system clocks). Otherwise the original instruction cycle is unchanged.

(3): (1) and (2)

(4): The flags may be affected by the execution status. If the Watchdog Timer is cleared by executing the ″CLR WDT1″ or ″CLR WDT2″ instruction, the TO and PDF are cleared.
Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

ADC A,[m] Add data memory and carry to the accumulator

Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the accumulator.

Operation ACC ← ACC+[m]+C

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

ADCM A,[m] Add the accumulator and carry to data memory

Description The contents of the specified data memory, accumulator and the carry flag are added simultaneously, leaving the result in the specified data memory.

Operation [m] ← ACC+[m]+C

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

ADD A,[m] Add data memory to the accumulator

Description The contents of the specified data memory and the accumulator are added. The result is stored in the accumulator.

Operation ACC ← ACC+[m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

ADD A,x Add immediate data to the accumulator

Description The contents of the accumulator and the specified data are added, leaving the result in the accumulator.

Operation ACC ← ACC+x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

ADDM A,[m] Add the accumulator to the data memory

Description The contents of the specified data memory and the accumulator are added. The result is stored in the data memory.

Operation [m] ← ACC+[m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

AND A,[m] Logical AND accumulator with data memory

Description Data in the accumulator and the specified data memory perform a bitwise logical_AND operation. The result is stored in the accumulator.

Operation ACC ← ACC "AND" [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

AND A,x Logical AND immediate data to the accumulator

Description Data in the accumulator and the specified data perform a bitwise logical_AND operation. The result is stored in the accumulator.

Operation ACC ← ACC "AND" x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

ANDM A,[m] Logical AND data memory with the accumulator

Description Data in the specified data memory and the accumulator perform a bitwise logical_AND operation. The result is stored in the data memory.

Operation [m] ← ACC "AND" [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

CALL addr Subroutine call

Description The instruction unconditionally calls a subroutine located at the indicated address. The program counter increments once to obtain the address of the next instruction, and pushes this onto the stack. The indicated address is then loaded. Program execution continues with the instruction at this address.

Operation Stack ← Program Counter+1
Program Counter ← addr

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

CLR [m] Clear data memory

Description The contents of the specified data memory are cleared to 0.

Operation [m] ← 00H

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

CLR [m].i Clear bit of data memory

Description The bit i of the specified data memory is cleared to 0.

Operation [m].i ← 0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

CLR WDT Clear Watchdog Timer

Description The WDT is cleared (clears the WDT). The power down bit (PDF) and time-out bit (TO) are cleared.

Operation WDT ← 00H
PDF and TO ← 0

Affected flag(s)

TO	PDF	OV	Z	AC	C
0	0	—	—	—	—

CLR WDT1 Preclear Watchdog Timer

Description Together with CLR WDT2, clears the WDT. PDF and TO are also cleared. Only execution of this instruction without the other preclear instruction just sets the indicated flag which implies this instruction has been executed and the TO and PDF flags remain unchanged.

Operation WDT ← 00H*
PDF and TO ← 0*

Affected flag(s)

TO	PDF	OV	Z	AC	C
0*	0*	—	—	—	—

CLR WDT2 Preclear Watchdog Timer

Description Together with CLR WDT1, clears the WDT. PDF and TO are also cleared. Only execution of this instruction without the other preclear instruction, sets the indicated flag which implies this instruction has been executed and the TO and PDF flags remain unchanged.

Operation WDT ← 00H*
PDF and TO ← 0*

Affected flag(s)

TO	PDF	OV	Z	AC	C
0*	0*	—	—	—	—

CPL [m] Complement data memory

Description Each bit of the specified data memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice-versa.

Operation [m] ← $[\overline{m}]$

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

CPLA [m] Complement data memory and place result in the accumulator

Description Each bit of the specified data memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice-versa. The complemented result is stored in the accumulator and the contents of the data memory remain unchanged.

Operation ACC ← $[\overline{m}]$

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

DAA [m] Decimal-Adjust accumulator for addition

Description The accumulator value is adjusted to the BCD (Binary Coded Decimal) code. The accumulator is divided into two nibbles. Each nibble is adjusted to the BCD code and an internal carry (AC1) will be done if the low nibble of the accumulator is greater than 9. The BCD adjustment is done by adding 6 to the original value if the original value is greater than 9 or a carry (AC or C) is set; otherwise the original value remains unchanged. The result is stored in the data memory and only the carry flag (C) may be affected.

Operation If ACC.3~ACC.0 >9 or AC=1
then [m].3~[m].0 ← (ACC.3~ACC.0)+6, AC1=$\overline{AC}$
else [m].3~[m].0 ← (ACC.3~ACC.0), AC1=0
and
If ACC.7~ACC.4+AC1 >9 or C=1
then [m].7~[m].4 ← ACC.7~ACC.4+6+AC1,C=1
else [m].7~[m].4 ← ACC.7~ACC.4+AC1,C=C

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	√

DEC [m] Decrement data memory

Description Data in the specified data memory is decremented by 1.

Operation [m] ← [m]–1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

DECA [m] Decrement data memory and place result in the accumulator

Description Data in the specified data memory is decremented by 1, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation ACC ← [m]–1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

HALT Enter Power Down Mode

Description: This instruction stops program execution and turns off the system clock. The contents of the RAM and registers are retained. The WDT and prescaler are cleared. The power down bit (PDF) is set and the WDT time-out bit (TO) is cleared.

Operation:
Program Counter ← Program Counter+1
PDF ← 1
TO ← 0

Affected flag(s)

TO	PDF	OV	Z	AC	C
0	1	—	—	—	—

INC [m] Increment data memory

Description: Data in the specified data memory is incremented by 1

Operation: [m] ← [m]+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

INCA [m] Increment data memory and place result in the accumulator

Description: Data in the specified data memory is incremented by 1, leaving the result in the accumulator. The contents of the data memory remain unchanged.

Operation: ACC ← [m]+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

JMP addr Directly jump

Description: The program counter are replaced with the directly-specified address unconditionally, and control is passed to this destination.

Operation: Program Counter ←addr

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

MOV A,[m] Move data memory to the accumulator

Description: The contents of the specified data memory are copied to the accumulator.

Operation: ACC ← [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

MOV A,x Move immediate data to the accumulator

Description The 8-bit data specified by the code is loaded into the accumulator.

Operation ACC ← x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

MOV [m],A Move the accumulator to data memory

Description The contents of the accumulator are copied to the specified data memory (one of the data memories).

Operation [m] ←ACC

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

NOP No operation

Description No operation is performed. Execution continues with the next instruction.

Operation Program Counter ← Program Counter+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

OR A,[m] Logical OR accumulator with data memory

Description Data in the accumulator and the specified data memory (one of the data memories) perform a bitwise logical_OR operation. The result is stored in the accumulator.

Operation ACC ← ACC ″OR″ [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

OR A,x Logical OR immediate data to the accumulator

Description Data in the accumulator and the specified data perform a bitwise logical_OR operation. The result is stored in the accumulator.

Operation ACC ← ACC ″OR″ x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

ORM A,[m] Logical OR data memory with the accumulator

Description Data in the data memory (one of the data memories) and the accumulator perform a bitwise logical_OR operation. The result is stored in the data memory.

Operation [m] ←ACC ″OR″ [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

RET Return from subroutine

Description The program counter is restored from the stack. This is a 2-cycle instruction.

Operation Program Counter ← Stack

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RET A,x Return and place immediate data in the accumulator

Description The program counter is restored from the stack and the accumulator loaded with the specified 8-bit immediate data.

Operation Program Counter ← Stack
ACC ← x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RETI Return from interrupt

Description The program counter is restored from the stack, and interrupts are enabled by setting the EMI bit. EMI is the enable master (global) interrupt bit.

Operation Program Counter ← Stack
EMI ← 1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RL [m] Rotate data memory left

Description The contents of the specified data memory are rotated 1 bit left with bit 7 rotated into bit 0.

Operation [m].(i+1) ← [m].i; [m].i:bit i of the data memory (i=0~6)
[m].0 ← [m].7

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RLA [m] Rotate data memory left and place result in the accumulator

Description Data in the specified data memory is rotated 1 bit left with bit 7 rotated into bit 0, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.

Operation ACC.(i+1) ← [m].i; [m].i:bit i of the data memory (i=0~6)
ACC.0 ← [m].7

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RLC [m] Rotate data memory left through carry

Description The contents of the specified data memory and the carry flag are rotated 1 bit left. Bit 7 replaces the carry bit; the original carry flag is rotated into the bit 0 position.

Operation [m].(i+1) ← [m].i; [m].i:bit i of the data memory (i=0~6)
[m].0 ← C
C ← [m].7

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	√

RLCA [m] Rotate left through carry and place result in the accumulator

Description Data in the specified data memory and the carry flag are rotated 1 bit left. Bit 7 replaces the carry bit and the original carry flag is rotated into bit 0 position. The rotated result is stored in the accumulator but the contents of the data memory remain unchanged.

Operation ACC.(i+1) ← [m].i; [m].i:bit i of the data memory (i=0~6)
ACC.0 ← C
C ← [m].7

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	√

RR [m] Rotate data memory right

Description The contents of the specified data memory are rotated 1 bit right with bit 0 rotated to bit 7.

Operation [m].i ← [m].(i+1); [m].i:bit i of the data memory (i=0~6)
[m].7 ← [m].0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RRA [m] Rotate right and place result in the accumulator

Description Data in the specified data memory is rotated 1 bit right with bit 0 rotated into bit 7, leaving the rotated result in the accumulator. The contents of the data memory remain unchanged.

Operation ACC.(i) ← [m].(i+1); [m].i:bit i of the data memory (i=0~6)
ACC.7 ← [m].0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

RRC [m] Rotate data memory right through carry

Description The contents of the specified data memory and the carry flag are together rotated 1 bit right. Bit 0 replaces the carry bit; the original carry flag is rotated into the bit 7 position.

Operation [m].i ← [m].(i+1); [m].i:bit i of the data memory (i=0~6)
[m].7 ← C
C ← [m].0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	√

RRCA [m] Rotate right through carry and place result in the accumulator

Description Data of the specified data memory and the carry flag are rotated 1 bit right. Bit 0 replaces the carry bit and the original carry flag is rotated into the bit 7 position. The rotated result is stored in the accumulator. The contents of the data memory remain unchanged.

Operation ACC.i ← [m].(i+1); [m].i:bit i of the data memory (i=0~6)
ACC.7 ← C
C ← [m].0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	√

SBC A,[m] Subtract data memory and carry from the accumulator

Description The contents of the specified data memory and the complement of the carry flag are subtracted from the accumulator, leaving the result in the accumulator.

Operation ACC ← ACC+$\overline{[m]}$+C

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

SBCM A,[m] Subtract data memory and carry from the accumulator

Description The contents of the specified data memory and the complement of the carry flag are subtracted from the accumulator, leaving the result in the data memory.

Operation [m] ← ACC+$\overline{[m]}$+C

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

SDZ [m] Skip if decrement data memory is 0

Description The contents of the specified data memory are decremented by 1. If the result is 0, the next instruction is skipped. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if ([m]–1)=0, [m] ← ([m]–1)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SDZA [m] Decrement data memory and place result in ACC, skip if 0

Description The contents of the specified data memory are decremented by 1. If the result is 0, the next instruction is skipped. The result is stored in the accumulator but the data memory remains unchanged. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if ([m]–1)=0, ACC ← ([m]–1)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SET [m] Set data memory

Description Each bit of the specified data memory is set to 1.

Operation [m] ← FFH

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SET [m]. i Set bit of data memory

Description Bit i of the specified data memory is set to 1.

Operation [m].i ← 1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SIZ [m] Skip if increment data memory is 0

Description The contents of the specified data memory are incremented by 1. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if ([m]+1)=0, [m] ← ([m]+1)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SIZA [m] Increment data memory and place result in ACC, skip if 0

Description The contents of the specified data memory are incremented by 1. If the result is 0, the next instruction is skipped and the result is stored in the accumulator. The data memory remains unchanged. If the result is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if ([m]+1)=0, ACC ← ([m]+1)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SNZ [m].i Skip if bit i of the data memory is not 0

Description If bit i of the specified data memory is not 0, the next instruction is skipped. If bit i of the data memory is not 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m].i≠0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SUB A,[m] Subtract data memory from the accumulator

Description The specified data memory is subtracted from the contents of the accumulator, leaving the result in the accumulator.

Operation ACC ← ACC+$\overline{[m]}$+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

SUBM A,[m] Subtract data memory from the accumulator

Description The specified data memory is subtracted from the contents of the accumulator, leaving the result in the data memory.

Operation [m] ← ACC+$\overline{[m]}$+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

SUB A,x Subtract immediate data from the accumulator

Description The immediate data specified by the code is subtracted from the contents of the accumulator, leaving the result in the accumulator.

Operation ACC ← ACC+$\overline{x}$+1

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	√	√	√	√

SWAP [m] Swap nibbles within the data memory

Description The low-order and high-order nibbles of the specified data memory (1 of the data memories) are interchanged.

Operation [m].3~[m].0 ↔ [m].7~[m].4

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SWAPA [m] Swap data memory and place result in the accumulator

Description The low-order and high-order nibbles of the specified data memory are interchanged, writing the result to the accumulator. The contents of the data memory remain unchanged.

Operation ACC.3~ACC.0 ← [m].7~[m].4
ACC.7~ACC.4 ← [m].3~[m].0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SZ [m] Skip if data memory is 0

Description If the contents of the specified data memory are 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m]=0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SZA [m] Move data memory to ACC, skip if 0

Description The contents of the specified data memory are copied to the accumulator. If the contents is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m]=0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

SZ [m].i Skip if bit i of the data memory is 0

Description If bit i of the specified data memory is 0, the following instruction, fetched during the current instruction execution, is discarded and a dummy cycle is replaced to get the proper instruction (2 cycles). Otherwise proceed with the next instruction (1 cycle).

Operation Skip if [m].i=0

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

TABRDC [m] Move the ROM code (current page) to TBLH and data memory

Description The low byte of ROM code (current page) addressed by the table pointer (TBLP) is moved to the specified data memory and the high byte transferred to TBLH directly.

Operation [m] ← ROM code (low byte)
TBLH ← ROM code (high byte)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

TABRDL [m] Move the ROM code (last page) to TBLH and data memory

Description The low byte of ROM code (last page) addressed by the table pointer (TBLP) is moved to the data memory and the high byte transferred to TBLH directly.
Note that this instruction is not valid for HT48R07A-1/HT48C07

Operation [m] ← ROM code (low byte)
TBLH ← ROM code (high byte)

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	—	—	—

XOR A,[m] Logical XOR accumulator with data memory

Description Data in the accumulator and the indicated data memory perform a bitwise logical Exclusive_OR operation and the result is stored in the accumulator.

Operation ACC ← ACC ″XOR″ [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

XORM A,[m] Logical XOR data memory with the accumulator

Description Data in the indicated data memory and the accumulator perform a bitwise logical Exclusive_OR operation. The result is stored in the data memory. The 0 flag is affected.

Operation [m] ← ACC ″XOR″ [m]

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

XOR A,x Logical XOR immediate data to the accumulator

Description Data in the accumulator and the specified data perform a bitwise logical Exclusive_OR operation. The result is stored in the accumulator. The 0 flag is affected.

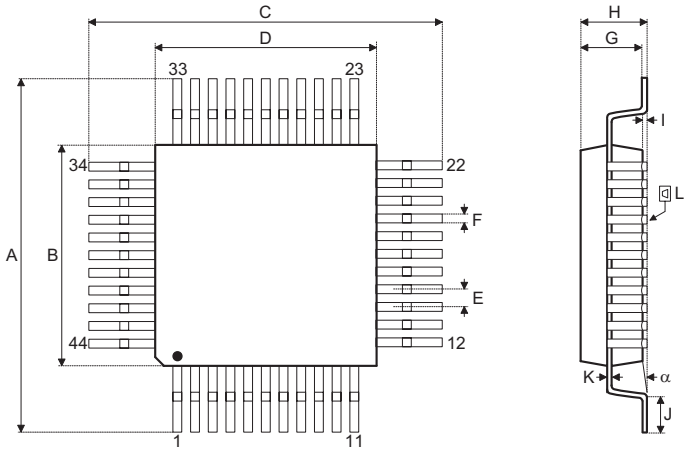
Operation ACC ← ACC ″XOR″ x

Affected flag(s)

TO	PDF	OV	Z	AC	C
—	—	—	√	—	—

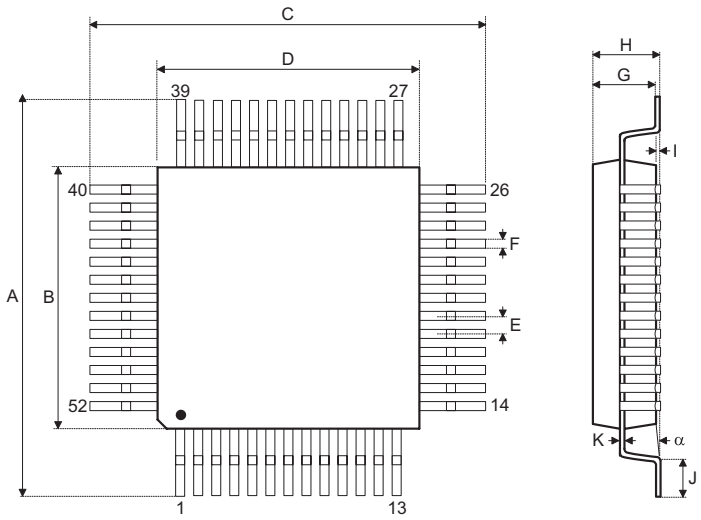
Package Information

44-pin QFP (10×10) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	13	—	13.4
B	9.9	—	10.1
C	13	—	13.4
D	9.9	—	10.1
E	—	0.8	—
F	—	0.3	—
G	1.9	—	2.2
H	—	—	2.7
I	0.25	—	0.5
J	0.73	—	0.93
K	0.1	—	0.2
L	—	0.1	—
α	0°	—	7°

52-pin QFP (14×14) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	17.3	—	17.5
B	13.9	—	14.1
C	17.3	—	17.5
D	13.9	—	14.1
E	—	1	—
F	—	0.4	—
G	2.5	—	3.1
H	—	—	3.4
I	—	0.1	—
J	0.73	—	1.03
K	0.1	—	0.2
α	0°	—	7°

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