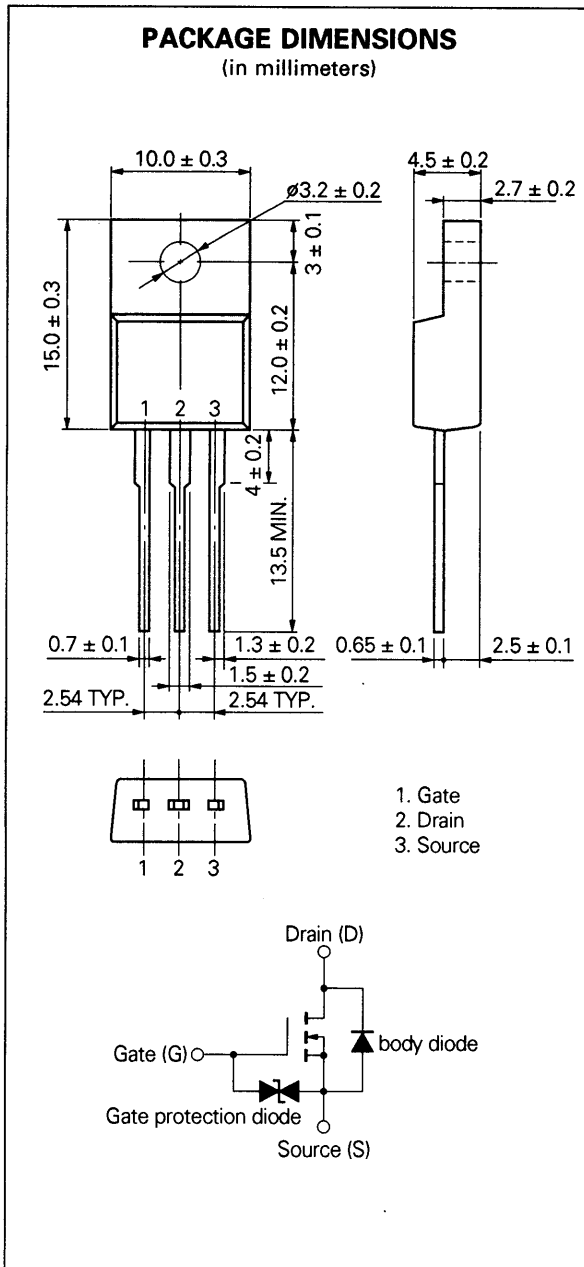


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P1 98.2

# MOS FIELD EFFECT POWER TRANSISTOR 2SK2234

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE



### DESCRIPTION

The 2SK2234 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

### FEATURES

- Low On-state Resistance  
 $R_{DS(on)} = 0.6 \Omega$  MAX. ( $V_{GS} = 10 V$ ,  $I_D = 4.0 A$ )
- Low  $C_{iss}$   $C_{iss} = 1\ 500$  pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

### ABSOLUTE MAXIMUM RATINGS

#### Maximum Temperatures

Storage Temperature	-55 to +150	°C
Channel Temperature	150	°C MAX.

#### Maximum Power Dissipation

Total Power Dissipation ( $T_c = 25\ ^\circ\text{C}$ )	40	W
Total Power Dissipation ( $T_a = 25\ ^\circ\text{C}$ )	2.0	W

#### Maximum Voltages and Currents ( $T_a = 25\ ^\circ\text{C}$ )

$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_{D(DC)}$	Drain Current (DC)	$\pm 8.0$	A
$I_{D(pulse)^*}$	Drain Current (pulse)	$\pm 32$	A

#### Maximum Avalanche Capability Ratings\*\*

$I_{AS}$	Single Avalanche Current	12	A
$E_{AS}$	Single Avalanche Energy	362	mJ

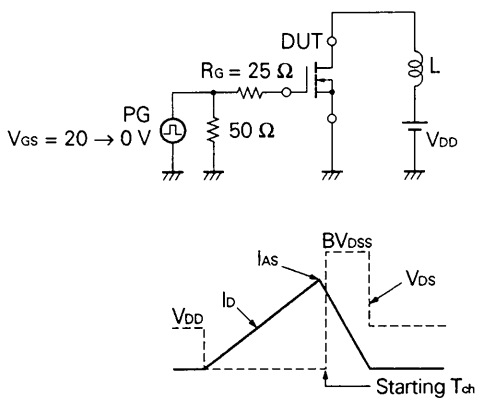
\*  $PW \leq 10\ \mu\text{s}$ , Duty Cycle  $\leq 1\ \%$

\*\* Starting  $T_{ch} = 25\ ^\circ\text{C}$ ,  $R_G = 25\ \Omega$ ,  $V_{GS} = 20\ V \rightarrow 0$

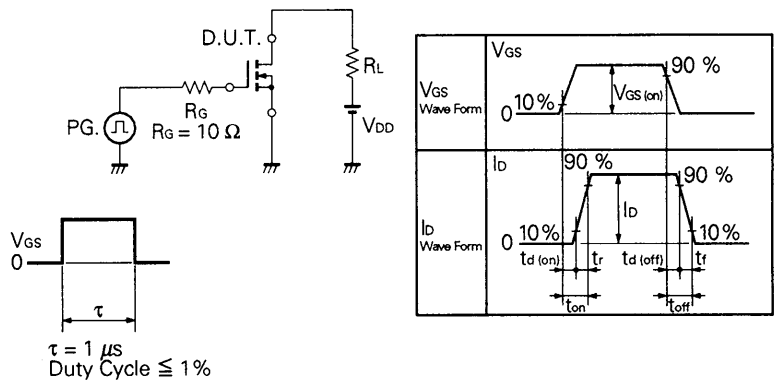
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.5	0.6	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	3.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 500		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		480		pF	
Reverse Transfer Capacitance	C <sub>res</sub>		200		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		23		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 150 V I <sub>D</sub> = 4 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 37.5 Ω
Rise Time	t <sub>r</sub>		23		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		104		ns	
Fall Time	t <sub>f</sub>		21		ns	
Total Gate Charge	Q <sub>G</sub>		57		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 8 A V <sub>DD</sub> = 400 V
Gate to Source Charge	Q <sub>GS</sub>		8.6		nC	
Gate to Drain Charge	Q <sub>GD</sub>		3.4		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		435		ns	I <sub>F</sub> = 8 A di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		2.1		μC	

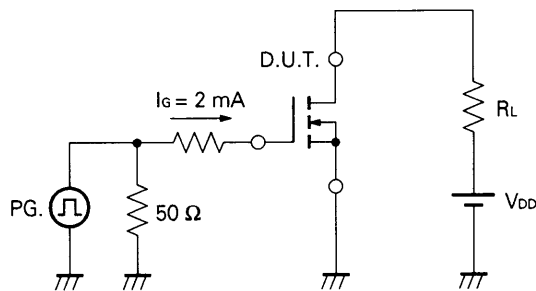
**Test Circuit 1: Avalanche Capability**



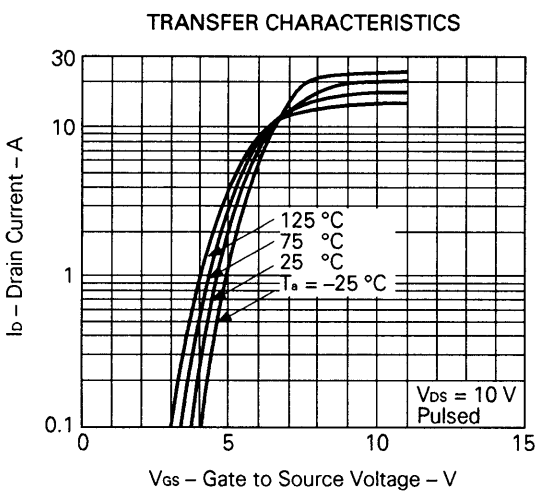
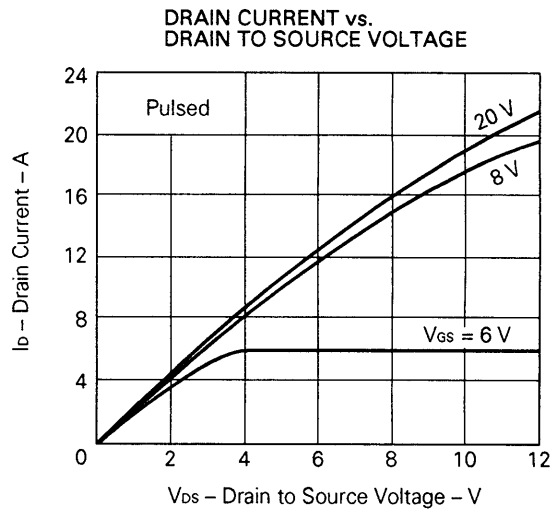
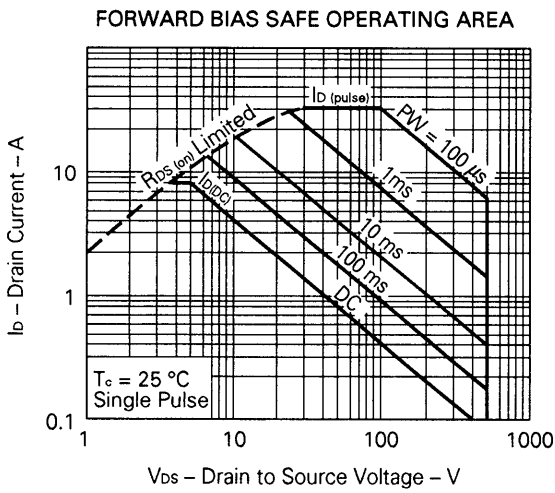
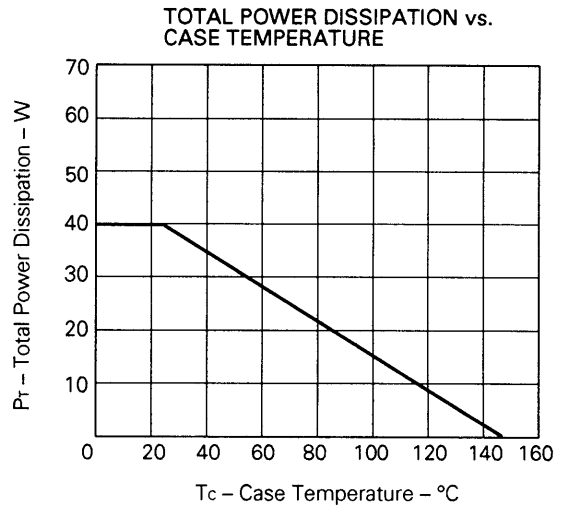
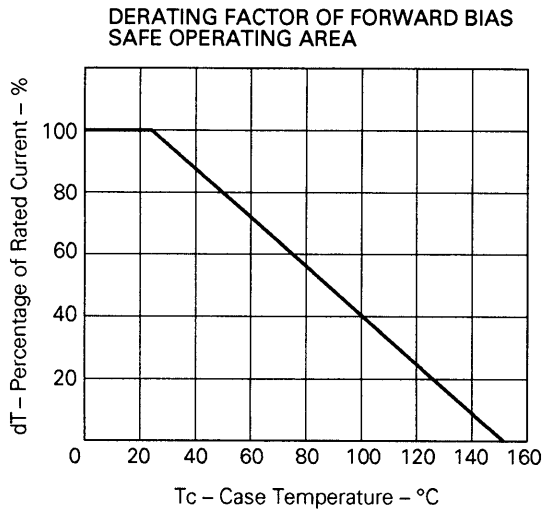
**Test Circuit 2: Switching Time**



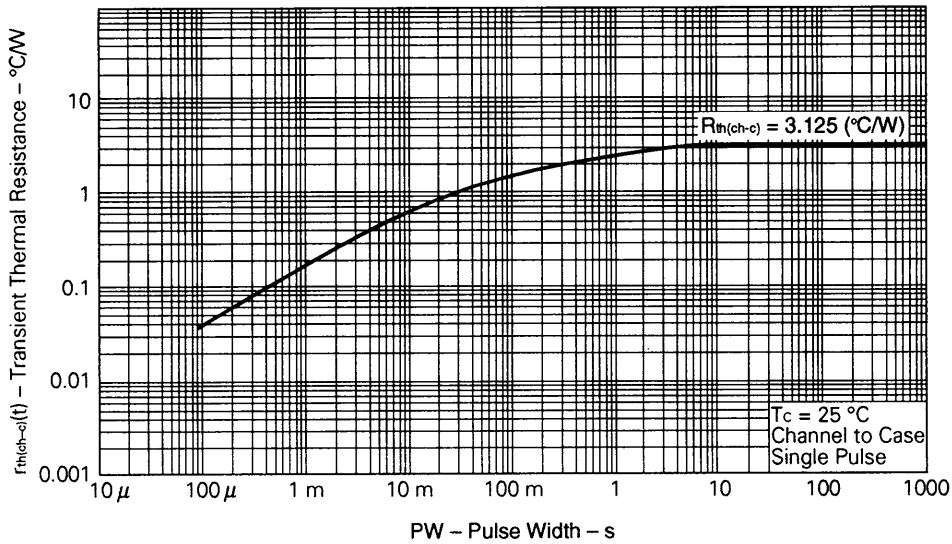
**Test Circuit 3: Gate Charge**



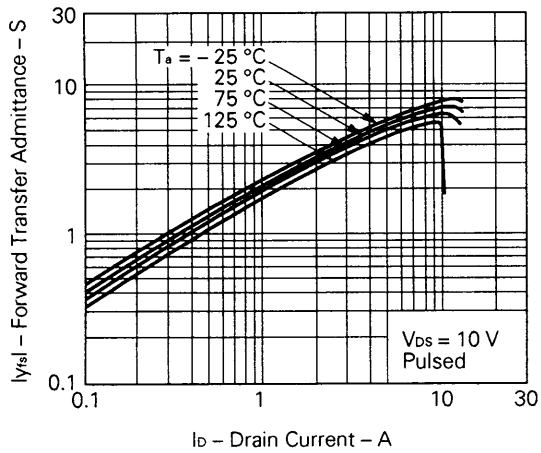
TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )



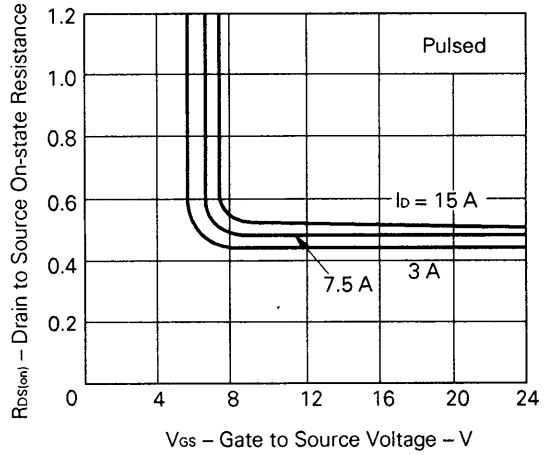
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



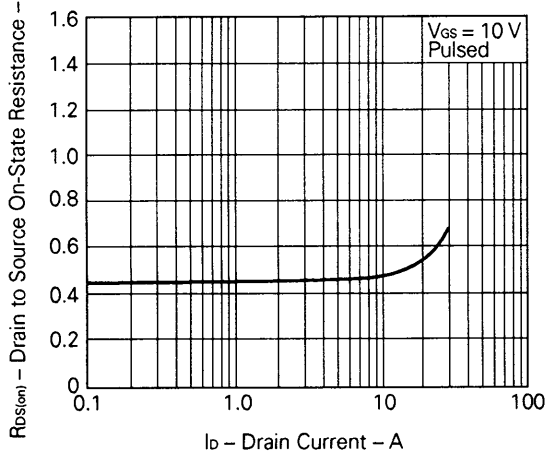
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



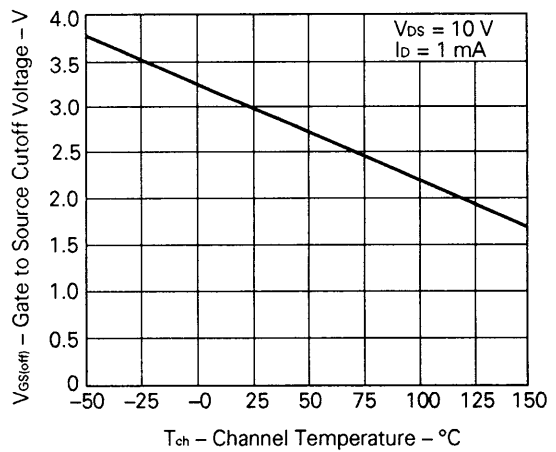
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



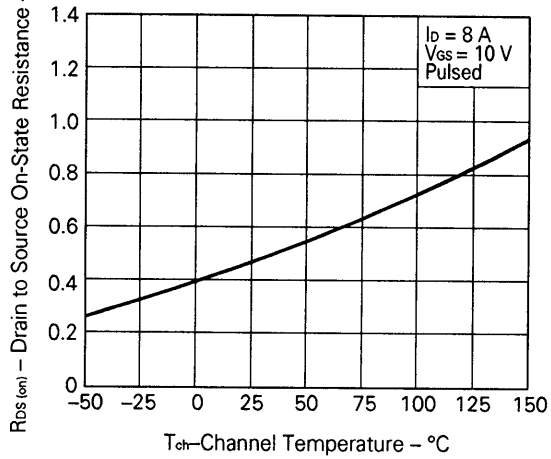
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



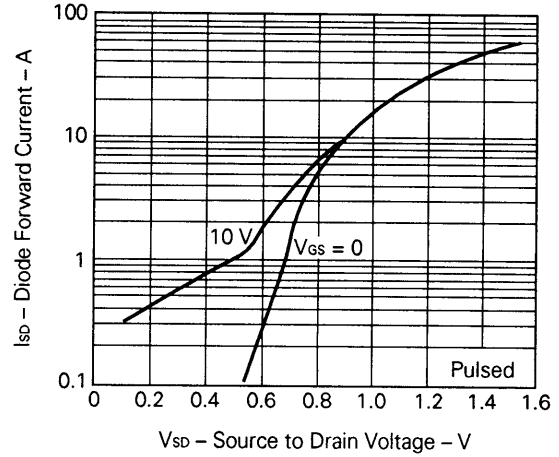
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



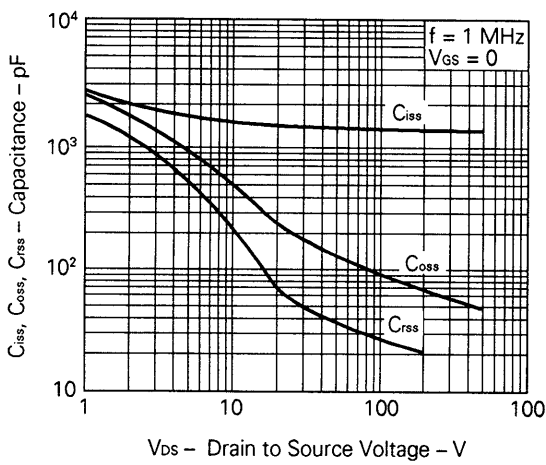
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE**



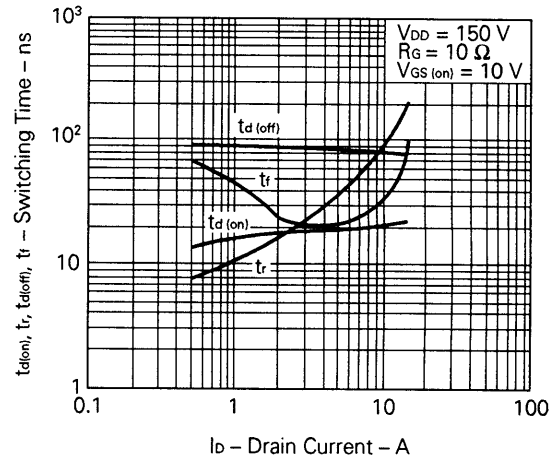
**SOURCE TO DRAIN DIODE FORWARD VOLTAGE**



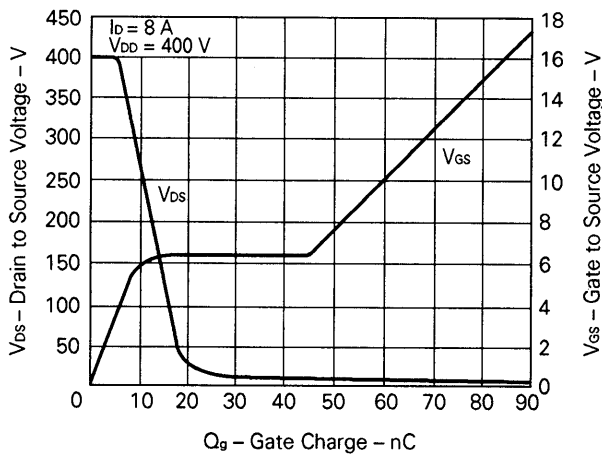
**CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE**



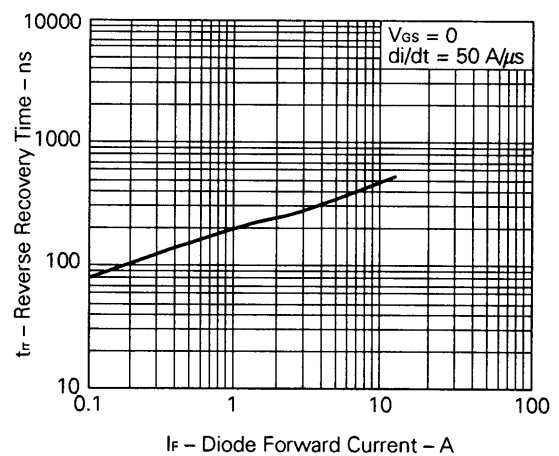
**SWITCHING CHARACTERISTICS**

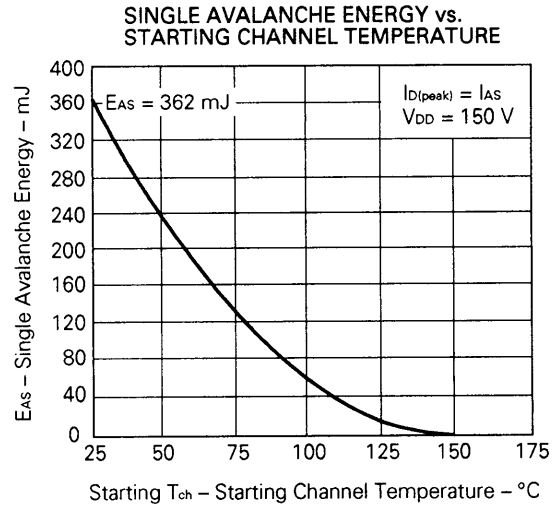
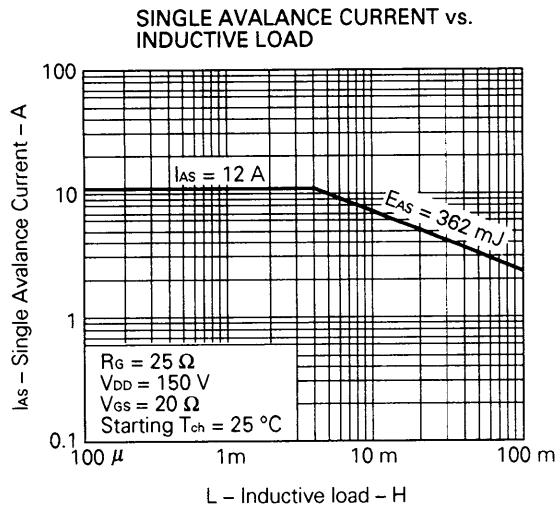


**DYNAMIC INPUT CHARACTERISTICS**



**REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT**





**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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