# HD153119

## Color Palette with Triple 6-bit DA Converter

The HD153119FS/CP is a color palette with triple 6-bit DA converter. Manufactured with Hitachi's Hi-BiCMOS process, this LSI realizes high speed, high density, low power consumption and minimizes the need for externally connected parts. Also, in addition to applications for existing CRTs, the provision of digital R, G and B outputs for color LCD ensure that the HD153119 can easily accomodate future systems using full-color LCD. With color palette, advanced functions, small size and low cost, the HD153119 is an essential component for advanced graphics systems.

### Features

- Displays 256 colors simultaneously from a total of 262,144 possible colors
- Three 6-bit DA converters for RGB video output on a single chip
- Pixel mask function for display control
- Compatible with personal system/2*
- For each pixel, dynamic switching between 262,144-color simultaneous display mode and normal mode.
- In addition to existing CRT applications, direct digital RGB outputs from the color lookup table(CLT) are provided for color LCD applications.
- Variable BLACK level (0 or 7.5 IRE)
- Selectable composite or non-composite SYNC signal (composite is RGB three-channel)
- Dot rate maximum of 50/65 MHz
- Synchronous timing for pipeline control selectable between rise or fall of DOTCK.
- TTL compatible I/O levels

Note: Personal System/2 is a registered trademark of IBM corporation.

### Ordering Information

| Type No. | Max. Operating Freq. | Package |
|---|---|---|
| HD153119FS | 50 MHz | 80 pin plastic QFP (FP-80B) |
| HD153119FS-65 | 65 MHz | |
| HD153119CP | 50 MHz | 68 pin plastic QFJ (CP-68) |
| HD153119CP-65 | 65 MHz | |

### Pin Arrangement

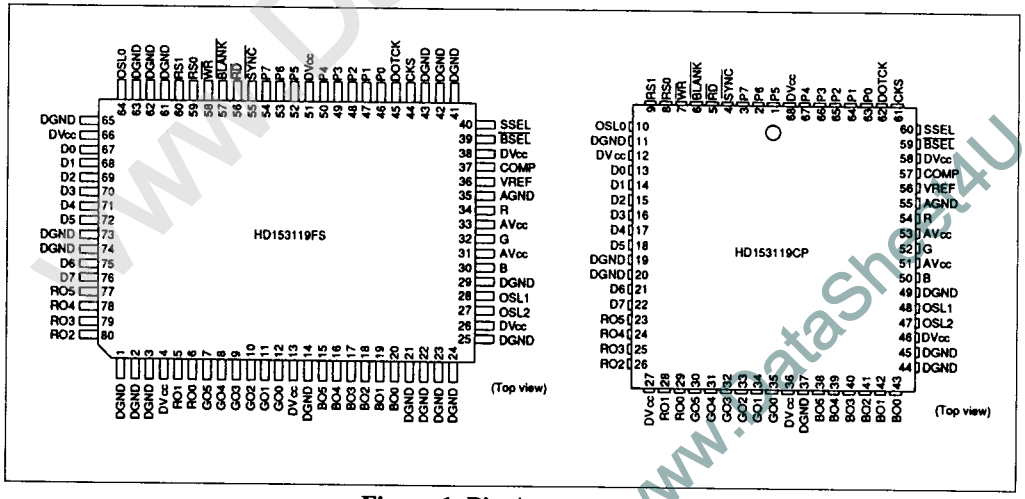
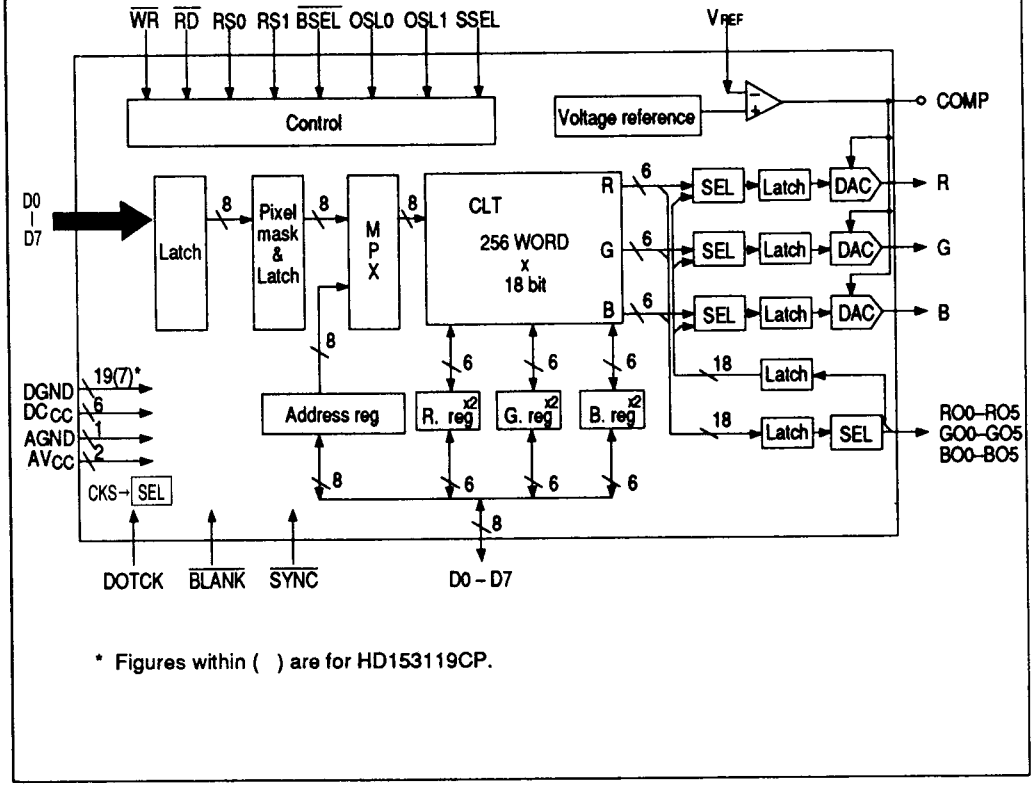



Figure 1 Pin Arrangement

## Block Diagram




* Figures within ( ) are for HD153119CP.

**Figure 2 Block Diagram**

**Table 1 Pin Description**

| Pin name | Pin number * | Description |
|---|---|---|
| P0 – P7 | 46 – 50<br>52 – 54<br>(63 – 67, 1 – 3) | CLT address inputs. P7 is MSB. P0 is LSB. |
| D0 – D7 | 67 – 72, 75, 76<br>(13 – 18, 21, 22) | Data port for reading/writing CLT or address, pixel mask, R, G and B registers. D7 is MSB, D0 is LSB. |
| $\overline{RD}$ | 56<br>(5) | Read clock input. Strobes data from CLT or address, pixel mask, R, G or B registers during read operation. |
| $\overline{WR}$ | 58<br>(7) | Write clock input. Strobes data to CLT or address, pixel mask, R, G or B registers during write operation. |
| RS0, RS1 | 59, 60<br>(8, 9) | Select input for CLT, address register or pixel mask register. |
| RO0 – RO5<br>GO0 – GO5<br>BO0 – BO5 | 6, 5, 80 – 77<br>(29, 28, 26 – 23)<br>12 – 7<br>(35 – 30)<br>20 – 15<br>(43 – 38) | Palette (CLT) digital signal outputs. RO5, GO5 and BO5 are the MSBs and RO0, GO0, and BO0 are the LSBs. |
| VREF | 36<br>(56) | Terminal for connecting reference resistor to set DAC analog output level. |
| COMP | 37<br>(57) | Terminal for connecting a phase-compensation capacitor |
| OSL0, OSL1, OSL2 | 64, 28, 27<br>(10, 48, 47) | Select inputs for digital signal outputs. |
| R, G, B | 34, 32, 30<br>(54, 52, 50) | DAC analog signal outputs. |
| $\overline{BLANK}$ | 57<br>(6) | Video blank input for activating blank signal levels at DAC analog outputs. |
| $\overline{BSEL}$ | 39<br>(59) | Input for selecting DAC BLANK level (0 or 7.5 IRE) |
| DOTCK | 45<br>(62) | Reference clock input for digital and analog sections. On the rise of this signal, CLT, BLANK and SYNC operations are processed and analog signal outputs become active. |
| CKS | 44<br>(61) | Input for selecting active polarity of DOTCK. When CKS = 'L' operations occur on DOTCK rise. When CKS = 'H' operations occur on DOTCK fall. |

* Upper pin numbers are for HD153119FS. Lower pin numbers within ( ) are for HD153119CP.

**Pin Description (cont)**

| Pin name | Pin number * | Description |
|---|---|---|
| SSEL | 40<br>(60) | Input for selecting composite or non-composite SYNC signal. Composite when SSEL = 'H' and non-composite when SSEL = 'L'. For composite, the SYNC level is 0 IRE, blank level is 40 IRE and the WHITE level is 140 IRE. |
| DVCC | 4, 13, 26, 38, 51, 66<br>(12, 27, 36, 46,<br>58, 68) | Digital power supply |
| DGND | 1 – 3, 14, 21 – 25<br>29, 41 – 43,<br>61 – 63, 65, 73, 74<br>(11, 19, 20, 37,<br>44, 45, 49) | Digital GND |
| $AV_{CC}$ | 31, 33<br>(51, 53) | Analog power supply |
| AGND | 35<br>(55) | Analog GND |

* Upper pin numbers are for HD153119FS. Lower pin numbers within ( ) are for HD153119CP.



## Functions

### Accessing the CLT and Registers

The CLT and registers are selected with inputs RS0 and RS1 (see table 2).

**Table 2 Register Selection**

| RS1 | RS0 | Selection |
|---|---|---|
| 0 | 0 | Address register (write mode) |
| 1 | 1 | Address register (read mode) |
| 0 | 1 | CLT |
| 1 | 0 | Pixel mask register |

### Registers

**Address register:** To set up the address register for a CLT write operation, write the CLT address via D7 – D0 with RS0 = '0' and RS1 = '0' (in order to select the address register, write mode).
For a CLT read operation, write the CLT address via D7 – D0 with RS0 = '1' and RS1 = '1' (in order to select the address register, read mode).
Also, the address register contents can be read as shown in figure 10 and figure 11.

**Pixel mask register:** The pixel mask register is used when displayed colors to be modified (by altering the value input from video memory and the contents of the CLT). The pixel mask register is set by writing a pixel mask value to D7 (MSB) – D0 (LSB) with RS0 = '0' and RS1 = '1' (in order to select the pixel mask register for a data write) as shown in figure 13. During color palette operations, the value input from video memory at P7 (MSB) – P0 (LSB) is ANDed with the pixel mask register value, and the resulting value is applied as an address to the CLT. Consequently, pixel mask '0' bits will cancel corresponding video memory value '1' bits. Table 3 shows the CLT address that is generated for a particular pixel mask register value and video memory value.

**Table 3 Pixel Mask Example**

| Pixel mask register | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|
| Address input | Pd7 | Pd6 | Pd5 | Pd4 | Pd3 | Pd2 | Pd1 | Pd0 |
| CLT address value | Pd7 | 0 | Pd5 | 0 | Pd3 | Pd2 | 0 | Pd0 |

**RGB Registers:** There are two RGB register types: one for writing color information to the CLT and one for reading color information from the CLT. Each register type is organized as an 18-bit word. To read or write data to the CLT, set RS0 = '1' and RS1 = '0' to select the appropriate RGB register while performing the read or write via data port D0 (LSB) – D5 (MSB). Bits D6 and D7 may be either '0' or '1' at this time. Write or read the data in the order of R, G, B as shown in figure 7 and figure 8.

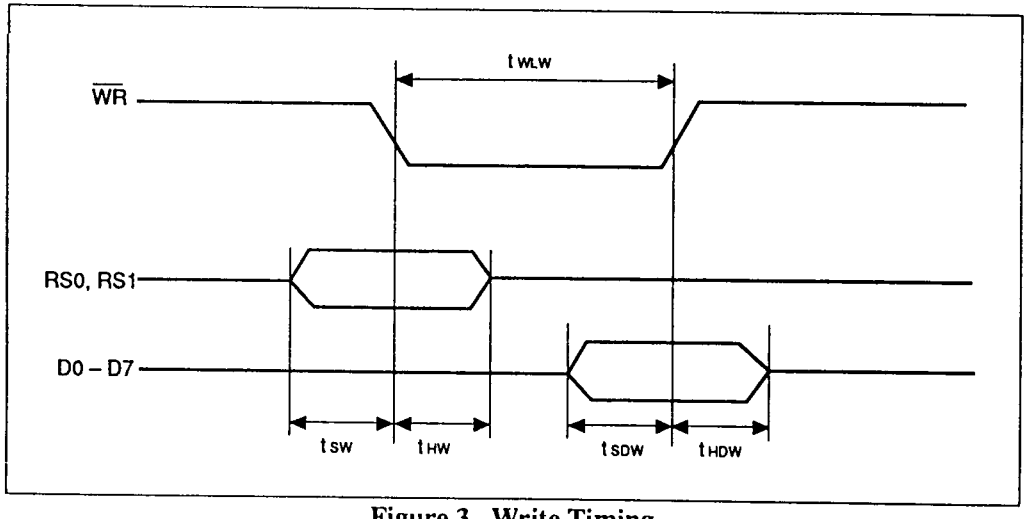



Figure 3 Write Timing

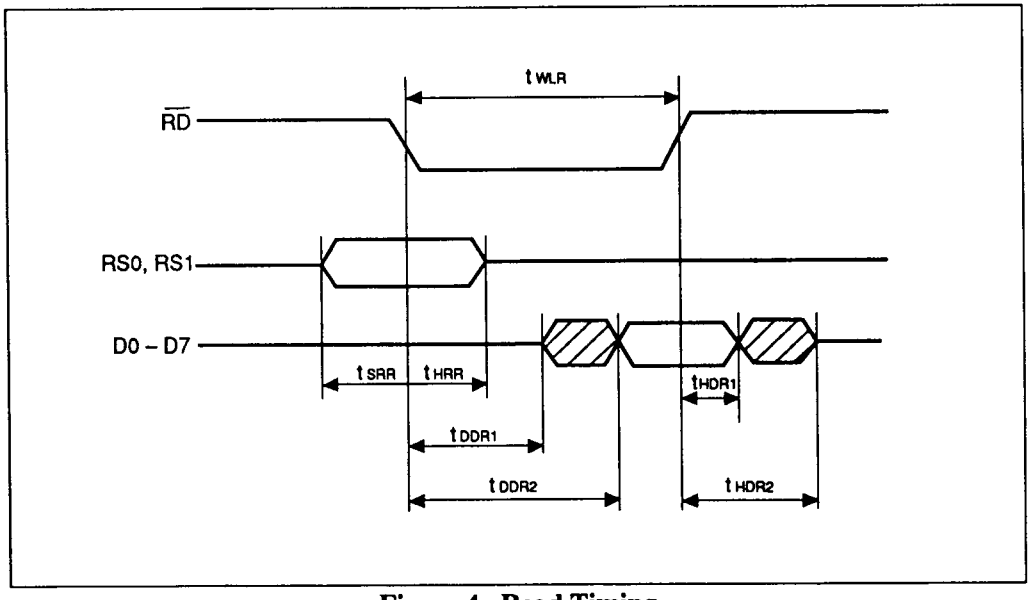
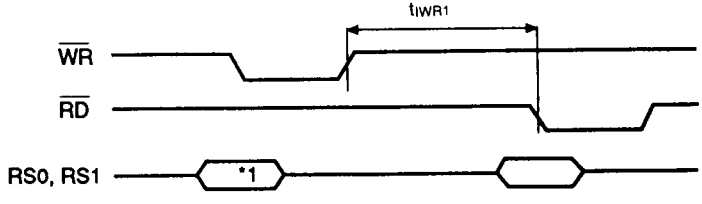


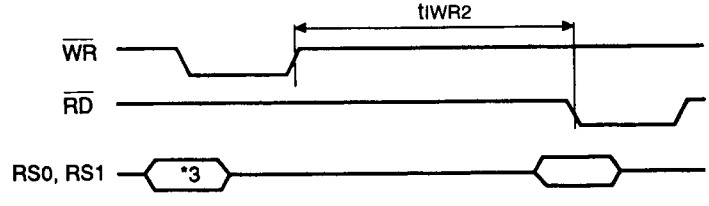

**Figure 4 Read Timing**

Applies to all read-after-write operations except when the write operation is placing a read address in the address register.




*1:
This timing not valid when RS0 = 'H' and RS1 = 'H'.

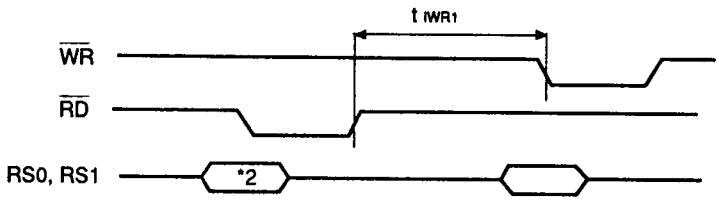
Applies to the case when the write operation is placing a read address in the address register.




*3:
This timing is valid when RS0 = 'H' and RS1 = 'H'.

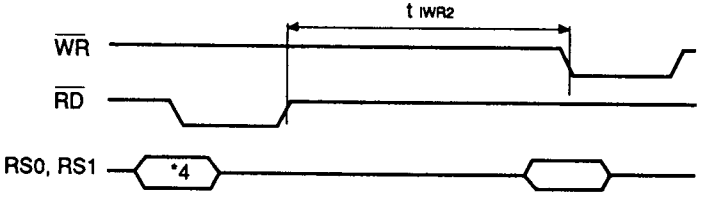
**Figure 5 Read after Write**

Applies to all cases except when the read operation is for CLT blue data.



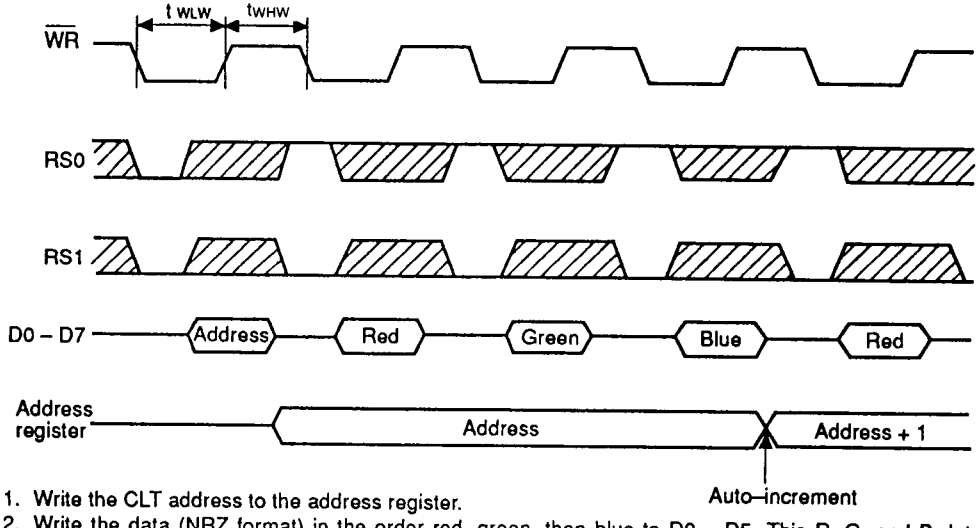

*2:
This timing not valid for reading CLT blue data or when RS0 = 'H' and RS1 = 'L'.

Applies to the case where the read operation is for CLT blue data.



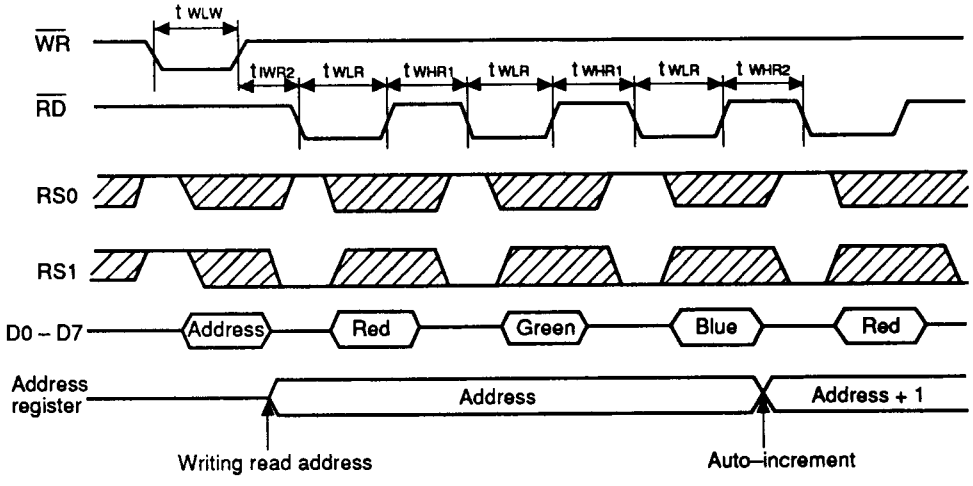

*4:
This timing is valid for reading CLT blue data or when RS0 = 'H' and RS1 = 'L'.

**Figure 6 Write after Read**



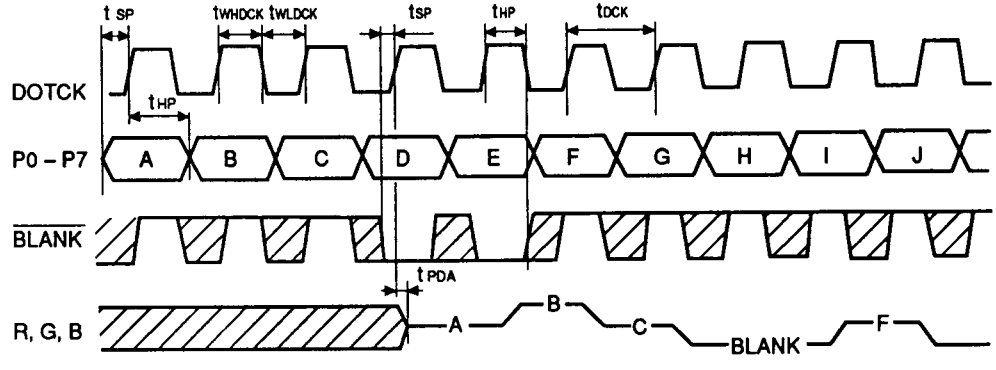

1. Write the CLT address to the address register.
2. Write the data (NRZ format) in the order red, green, then blue to D0 – D5. This R, G, and B data forms an 18-bit word that is written to the CLT.
3. When the R, G and B data writes are completed, the address is automatically incremented by +1 and the next data set can be applied again in RGB order. All subsequent CLT data writes should continue in this manner.

**Figure 7 CLT Write**




1. Write CLT address to the address register.
2. With each strobe of the $\overline{RD}$ line, CLT data can be read in the order red, green and blue at D0 – D5.
3. When the blue data read is completed, the address is automatically incremented and the CLT data for that address can then be read in the order of R, G and B.

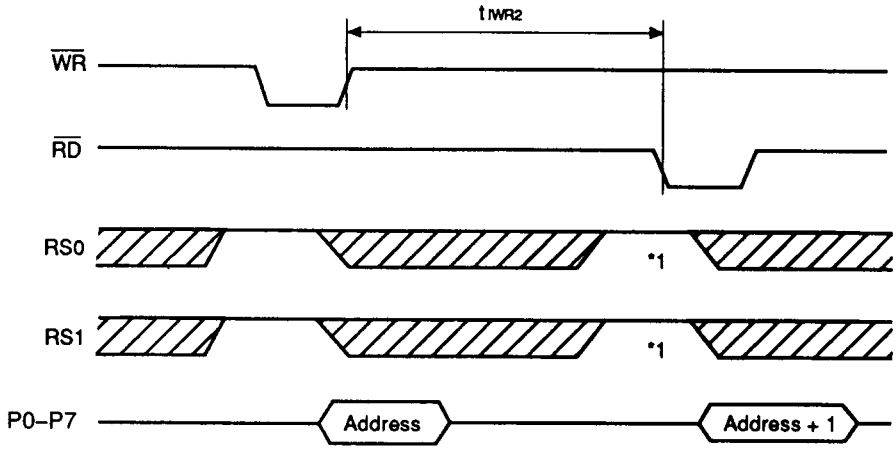
**Figure 8 CLT Read**




Video output is generated when a CLT adta location is selected by the address input at P7 – P0 and subsequently output as analog R, G, and B signals. The video output lags behind the PCLK strobe of its corresponding address at P7 – P0 by three PCLK clock periods.

Note: Digital and video signals are output in unison. During a blanking period, all outputs go to the 'L' level.

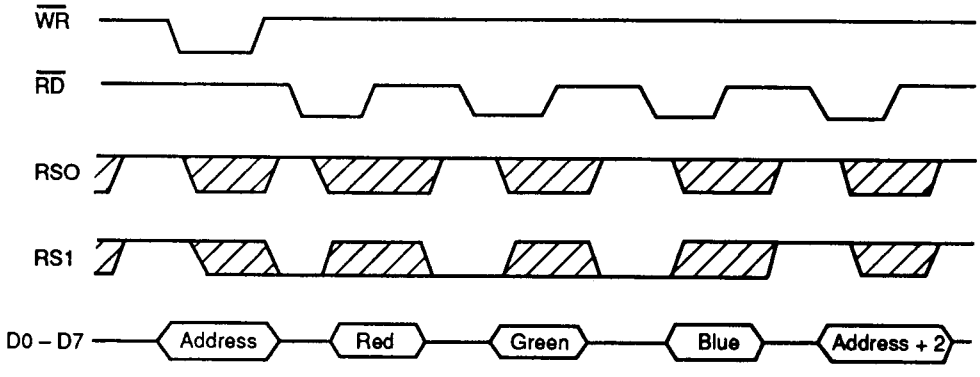
**Figure 9 Video Output**




1. Use $\overline{WR}$ to select the address register and to write the CLT read address.
2. Use $\overline{RD}$ to read the contents of the address register. At this time, the contents of the address register is incremented by +1.

*1: The address register can also be read when RS0 and Rs1 are both set to 'L'.

**Figure 10 Address Register Read (1)**




1. Use $\overline{WR}$ to select the address register and to write the CLT write address.
2. Use $\overline{RD}$ three times in succesion to read CLT data in the order red, green and blue.
3. Using $\overline{RD}$ again will read the contents of the address register. This read of the address register plus the previous read of red, blue and green data will increment the contents of the address register by +2.

*1: The address register can also be read when Rs0 and RS1 are both set to 'L'.

**Figure 11 Address Register Read (2)**

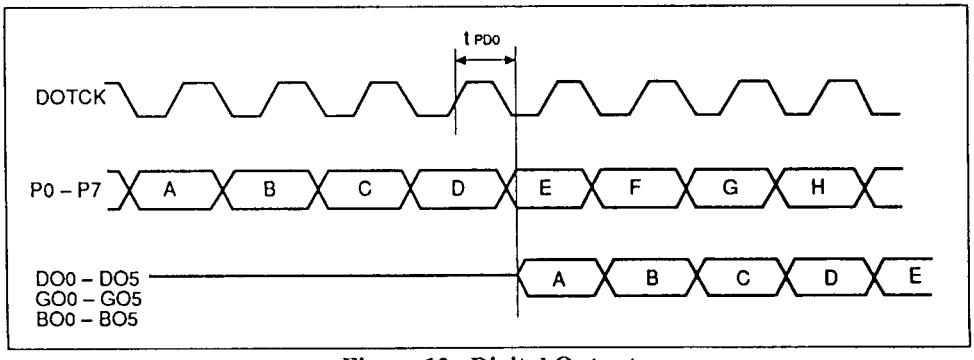



Figure 12 Digital Output

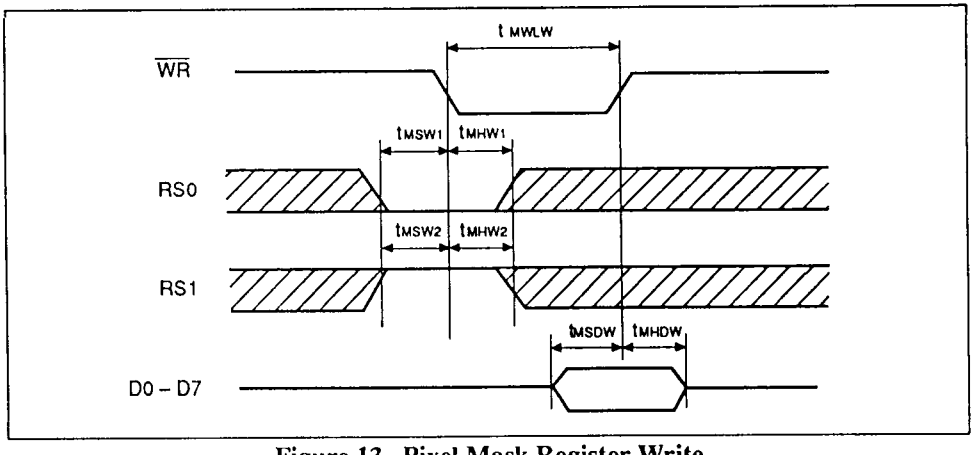



Figure 13 Pixel Mask Register Write

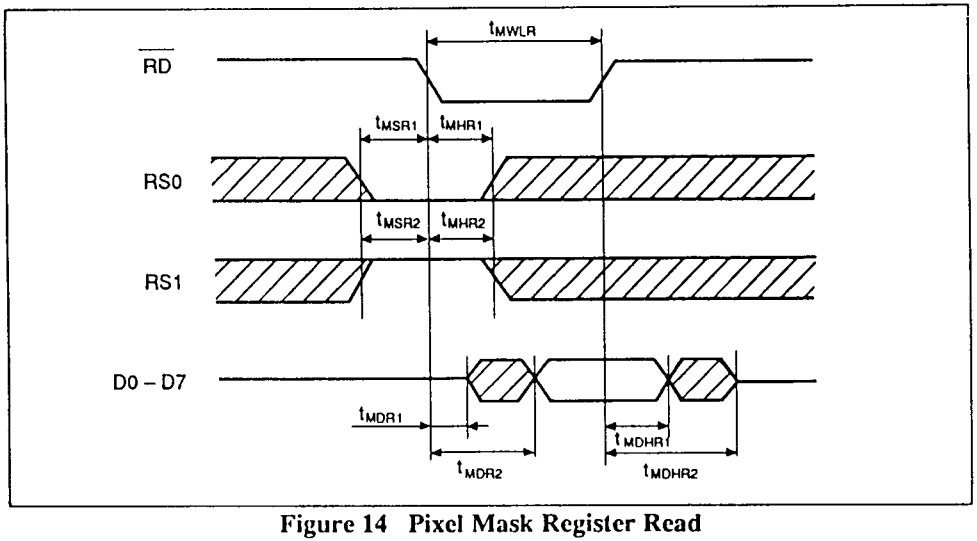
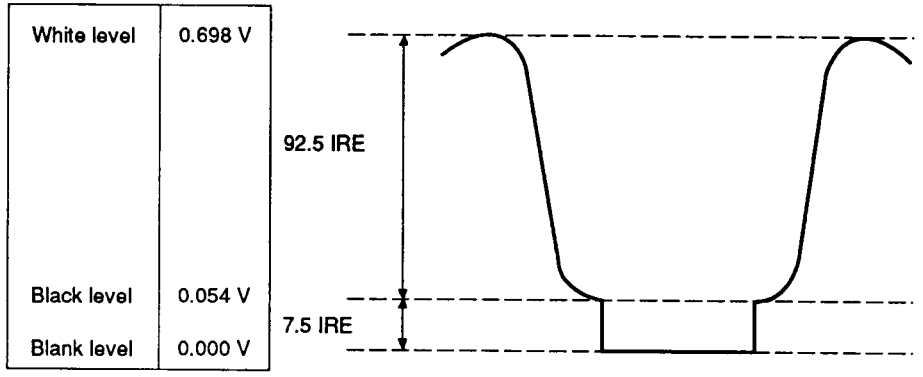
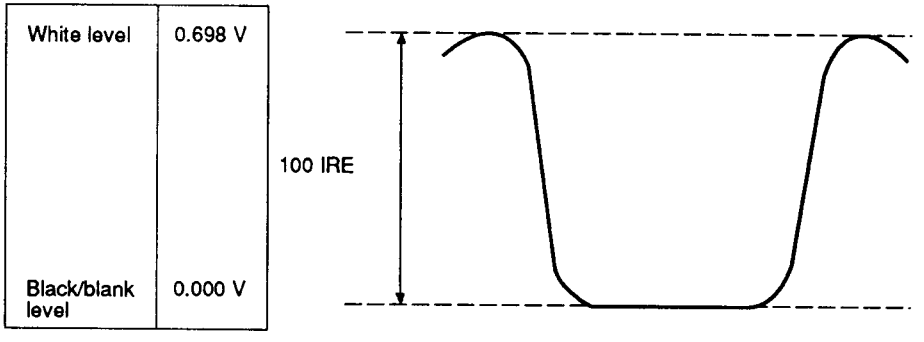



Figure 14 Pixel Mask Register Read

## Video Output Waveforms



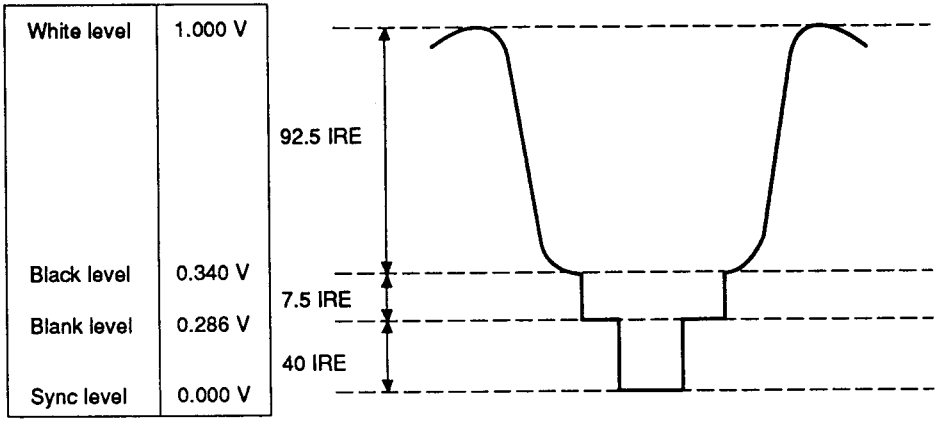

(SSEL = 'L', $\overline{BSEL}$ = 'L', $R_{VREF}$ = 13 kΩ)



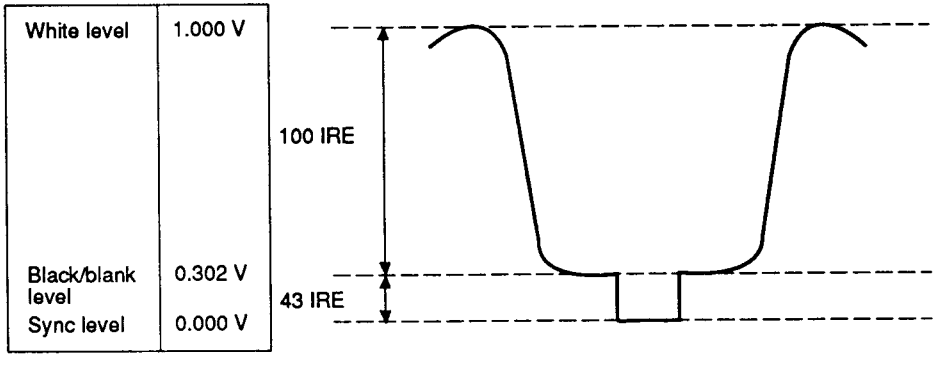

(SSEL = 'L', $\overline{BSEL}$ = 'H', $R_{VREF}$ = 12 kΩ)

**Figure 15 Video Output Waveforms**

## Video Output Waveforms (for composite $\overline{\text{SYNC}}$ signal)




(SSEL = 'H', $\overline{\text{BSEL}}$ = 'L', $R_{VREF}$ = 13 kΩ)




(SSEL = 'H', $\overline{\text{BSEL}}$ = 'H', $R_{VREF}$ = 12 kΩ)

**Figure 16 Video Output Waveforms (for composite SYNC signal)**

## Mode Switching

HD153110 operating mode is switched as shown table 3.

**Table 3 Mode Switching**

| OSL2 | OSL1 | OSL0 | Operating mode | Note |
|---|---|---|---|---|
| L | L | L | DAC output mode | 1 |
| L | L | H | DAC direct input (262,144-color simultaneous display mode) | 1 |
| L | H | L | Digital output 12-bit mode (R, G and B are output on upper 4 bits) | 2 |
| L | H | H | Prohibited (Digital output 18-bit mode) | 3 |
| H | L | L | Digital output 6-bit mode (Green output only) | 2 |
| H | L | H | Prohibited | |
| H | H | L | Digital output 18-bit mode | 2 |
| H | H | h | Prohibited | |

Notes: 1. Digital output is Hi-Z.
2. DAC outputs are off.
3. Both digital and DAC outputs are active.

## Resister Correspondence with CLT

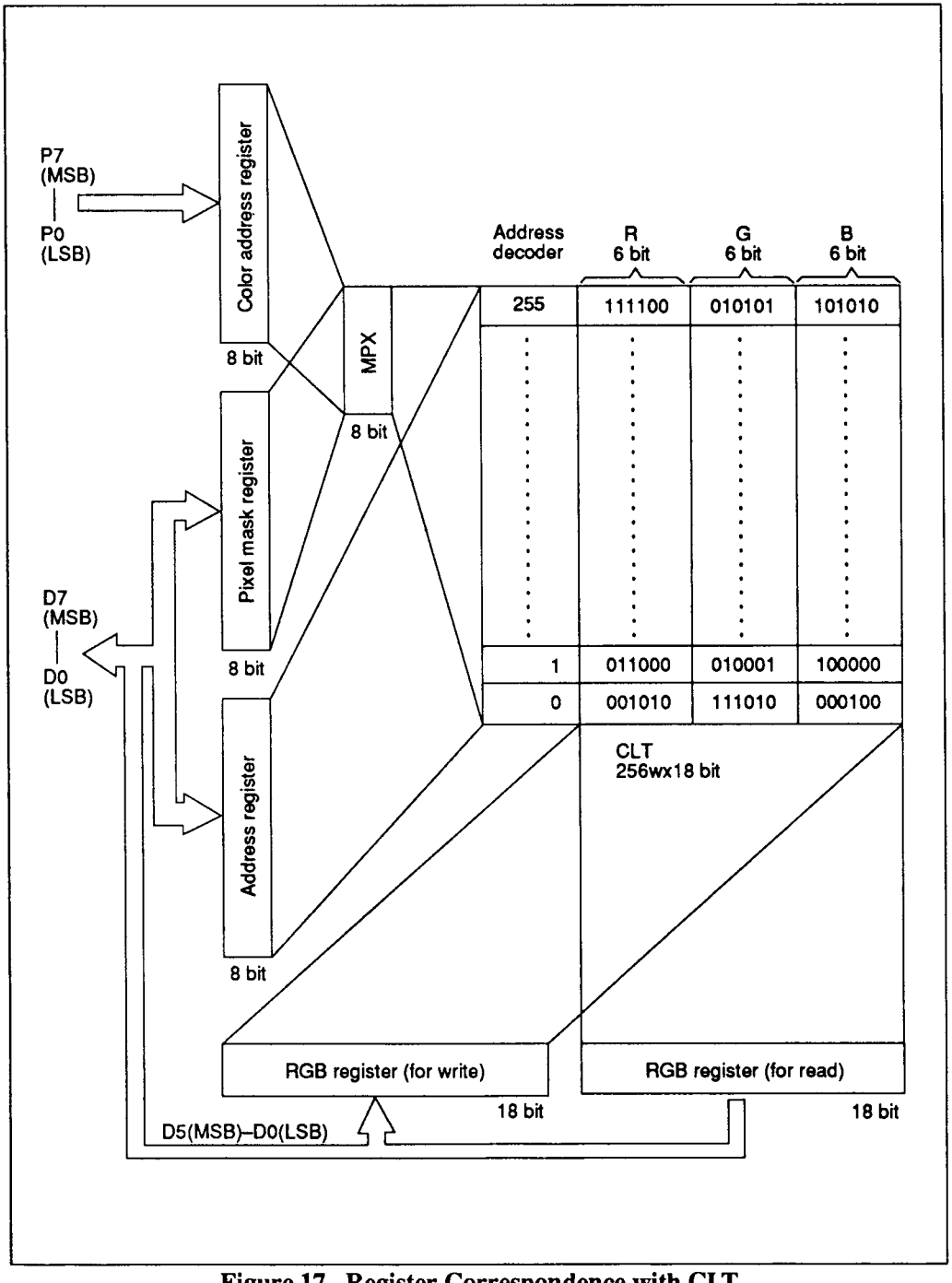



**Figure 17 Register Correspondence with CLT**

## System Configuration Example

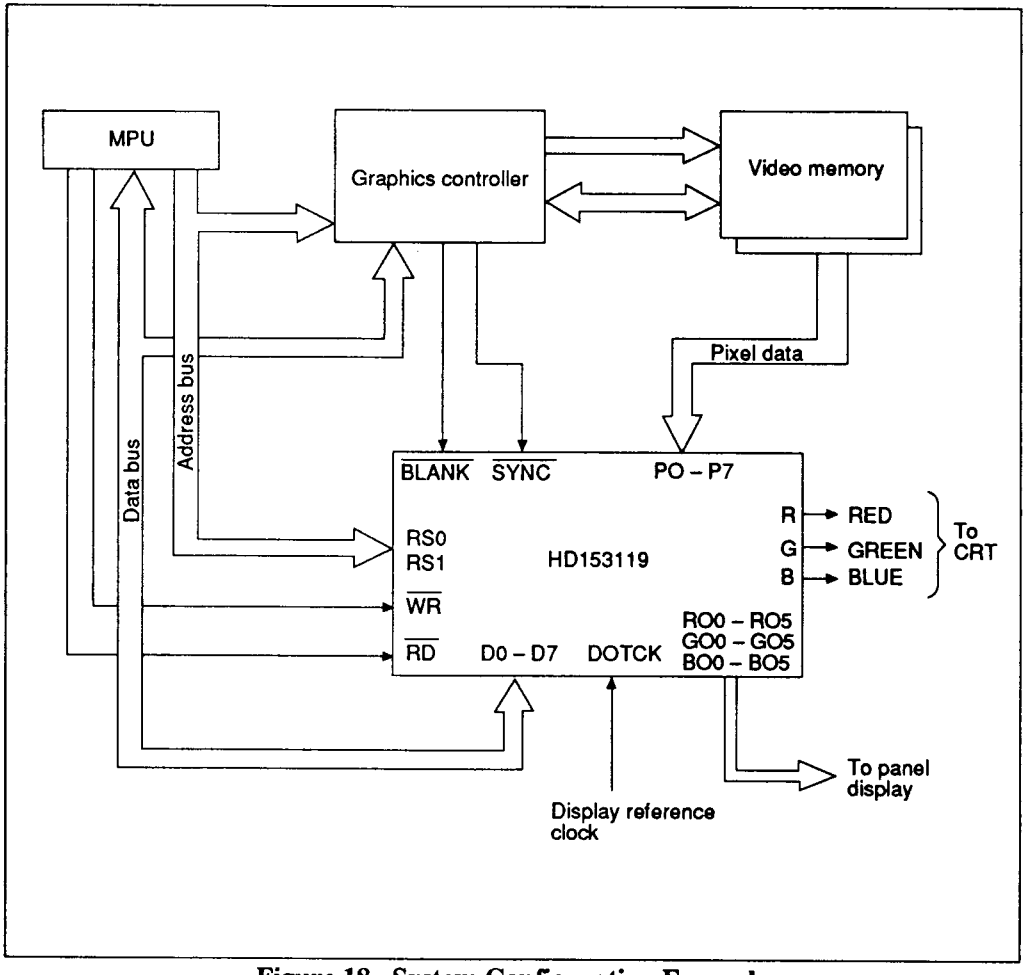



**Figure 18 System Configuration Example**

**Table 4 Absolute Maximum Ratings**

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 7.0 | V |
| Input voltage | $V_{in}$ | 0 to VCC | V |
| Operating temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage temperature | $T_{stg}$ | –55 to +150 | °C |

## Electrical Characteristics

**Table 5 DAC Section Electrical Characteristics ($V_{CC}$ = 5 V, Ta = 25 °C)**

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Resolution | | 6 | 6 | 6 | bits | |
| Maximum operating frequency | $f_{CLK}$ | — | — | 50/65 | MHz | |
| Analog output voltage | $V_A$ (Full) | –15 | — | 15 | % of FSR | |
| ($R_{VREF}$ = 12 kΩ) | $V_A$ (Zero) | –2 | — | 2 | % of FSR | |
| Differential linearity | DLE | –1 | — | +1 | LSB | |
| Integral linearity | ILE | –1 | — | +1 | LSB | |
| Output rise time (20 to 80 %) | tr | — | — | 10 | ns | $C_L$ = 15 pF |
| Output fall time (80 to 20 %) | tf | — | — | 10 | ns | $C_L$ = 15 pF |
| Settling time | ts | — | — | 30 | ns | $C_L$ = 15 pF |
| Glitch energy | $E_G$ | — | 90 | — | PVS | |

**Table 6 Digital section DC Characteristics (unless otherwise specified $V_{cc}$ = 5 V ± 5%, Ta = 0 ~ 70°C)**

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input "High" level voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ | V | |
| Input "Low" level voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | |
| Input clamp voltage | $V_I$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V<br>$I_{IN}$ = –18 mA |
| Output "High" level voltage | $V_{OH}$ | 2.7 | — | — | V | $V_{CC}$ = 4.75 V<br>$I_{OH}$ = –400 µA |
| Output "Low" level voltage | $V_{OL}$ | — | — | 0.5 | V | $V_{CC}$ = 4.75 V<br>$I_{OL}$ = 8 mA |
| Input current | $I_I$ | — | — | 1 | mA | $V_{CC}$ = 5.25 V<br>$V_I$ = 5.5 V |
| "High" level input current | $I_{IH}$ | — | — | 20 | µA | $V_{CC}$ = 5.25 V<br>$V_I$ = 2.7 V |
| "Low" level input current | $I_{IL}$ | — | — | –400 | µA | $V_{CC}$ = 5.25 V<br>$V_I$ = 0.4 V |
| Supply current (1) *1 | $I_{CC}$ (1) | — | 130 | 190 | mA | $V_{CC}$ = 5.25 V |
| Supply current (2) *2 | $I_{CC}$ (2) | — | 110 | 160 | mA | $V_{CC}$ = 5.25 V |

Notes: 1. OSL0 = 'L', OSL1 = 'L', OSL2 = 'L'
2. OSL0 = 'L', OSL1 = 'H', OSL2 = 'H'

**Table 7 Digital Section AC Characteristics ($V_{CC}$ = 5 V, Ta = 25 °C)**

| Item | Symbol | 50 MHz Min | 50 MHz Max | 65 MHz Min | 65 MHz Max | Unit | Test conditions | Reference figure |
|---|---|---|---|---|---|---|---|---|
| DOTCK cycle time | $t_{DCK}$ | 20 | — | 15.3 | — | ns | | 9 |
| DOTCK low level time | $t_{WLDCK}$ | 8 | — | 6 | — | ns | | 9 |
| DOTCK high level time | $t_{WHDCK}$ | 8 | — | 6 | — | ns | | 9 |
| Data setup time | $t_{SP}$ | 6 | — | 5 | — | ns | | 9 |
| Data hold time | $t_{HP}$ | 6 | — | 5 | — | ns | | 9 |
| Data output delay time | $t_{PDA}$ | — | 30 | — | 30 | ns | $C_L$ = 15 pF | 9 |
| $\overline{WR}$ low level time | $t_{WLW}$ | 50 | — | 50 | — | ns | | 3, 7, 8 |
| $\overline{WR}$ high level time | $t_{WHW}$ | 3 × $t_{DCK}$ | — | 3 × $t_{DCK}$ | — | ns | | 4, 8 |
| $\overline{RD}$ low level time | $t_{WLR}$ | 50 | — | 50 | — | ns | | 8 |
| $\overline{RD}$ high level time (1) | $t_{WHR1}$ | 3 × $t_{DCK}$ | — | 3 × $t_{DCK}$ | — | ns | | 8 |
| $\overline{RD}$ high level time (2) | $t_{WHR2}$ | 6 × $t_{DCK}$ | — | 6 × $t_{DCK}$ | — | ns | | 8 |
| $\overline{WR}$/$\overline{RD}$ interval time (1) | $t_{IWR1}$ | 3 × $t_{DCK}$ | — | 3 × $t_{DCK}$ | — | ns | | 5, 6 |
| $\overline{WR}$/$\overline{RD}$ interval time (2) | $t_{IWR2}$ | 6 × $t_{DCK}$ | — | 6 × $t_{DCK}$ | — | ns | | 5, 6, 8, 9 |
| $\overline{WR}$/RS0, RS1 setup time | $t_{SW}$ | 10 | — | 10 | — | ns | | 3 |
| $\overline{WR}$/RS0, RS1 hold time | $t_{HW}$ | 10 | — | 10 | — | ns | | 3 |
| $\overline{RD}$/RS0, RS1 setup time | $t_{SRR}$ | 10 | — | 10 | — | ns | | 4 |
| $\overline{RD}$/RS0, RS1 hold time | $t_{HRR}$ | 10 | — | 10 | — | ns | | 4 |
| $\overline{WR}$ data setup time | $t_{SDW}$ | 10 | — | 10 | — | ns | | 3 |
| $\overline{WR}$ data hold time | $t_{HDW}$ | 10 | — | 10 | — | ns | | 3 |
| $\overline{RD}$ data output delay time (1) | $t_{DDR1}$ | 5 | — | 5 | — | ns | $C_L$ = 15 pF | 4 |
| $\overline{RD}$ data output delay time (2) | $t_{DDR2}$ | — | 40 | — | 40 | ns | $C_L$ = 15 pF | 4 |
| $\overline{RD}$ data output hold time (1) | $t_{HDR1}$ | 5 | — | 5 | — | ns | $C_L$ = 15 pF | 4 |
| $\overline{RD}$ data output hold time (2) | $t_{HDR2}$ | — | 20 | — | 20 | ns | $C_L$ = 15 pF | 4 |
| Digital output delay time | $t_{PDO}$ | — | 19 | — | 19 | ns | $C_L$ = 15 pF | 12 |
| $\overline{WR}$ low level time | $t_{MWLW}$ | 50 | — | 50 | — | ns | | 13 |
| $\overline{RD}$ low level time | $t_{MWLR}$ | 50 | — | 50 | — | ns | | 14 |

**Digital Section AC Characteristics ($V_{CC}$ = 5 V, Ta = 25 °C) (cont)**

| Item | Symbol | 50 MHz Min | 50 MHz Max | 65 MHz Min | 65 MHz Max | Unit | Test conditions | Reference figure |
|---|---|---|---|---|---|---|---|---|
| $\overline{WR}$/RS0, RS1 setup time | $t_{MSW1}$ | 10 | — | 10 | — | ns | | 13 |
| | $t_{MSW2}$ | 10 | — | 10 | — | ns | | 13 |
| $\overline{WR}$/RS0, RS1 hold time | $t_{MHW1}$ | 10 | — | 10 | — | ns | | 13 |
| | $t_{MHW2}$ | 10 | — | 10 | — | ns | | 13 |
| $\overline{RD}$/RS0, RS1 setup time | $t_{MSR1}$ | 10 | — | 10 | — | ns | | 14 |
| | $t_{MSR2}$ | 10 | — | 10 | — | ns | | 14 |
| $\overline{RD}$/RS0, RS1 hold time | $t_{MHR1}$ | 10 | — | 10 | — | ns | | 14 |
| | $t_{MHR2}$ | 10 | — | 10 | — | ns | | 14 |
| $\overline{WR}$ data setup time | $t_{MSDW}$ | 10 | — | 10 | — | ns | | 13 |
| $\overline{WR}$ data hold time | $t_{MHDW}$ | 10 | — | 10 | — | ns | | 13 |
| $\overline{RD}$ data output delay time | $t_{MDR1}$ | 5 | — | 5 | — | ns | $C_L$ = 15 pF | 14 |
| | $t_{MDR2}$ | — | 40 | — | 40 | ns | $C_L$ = 15 pF | 14 |
| RD data output hold time | $t_{MDHR1}$ | 5 | — | 5 | — | ns | $C_L$ = 15 pF | 14 |
| | $t_{MDHR2}$ | — | 20 | — | 20 | ns | $C_L$ = 15 pF | 14 |

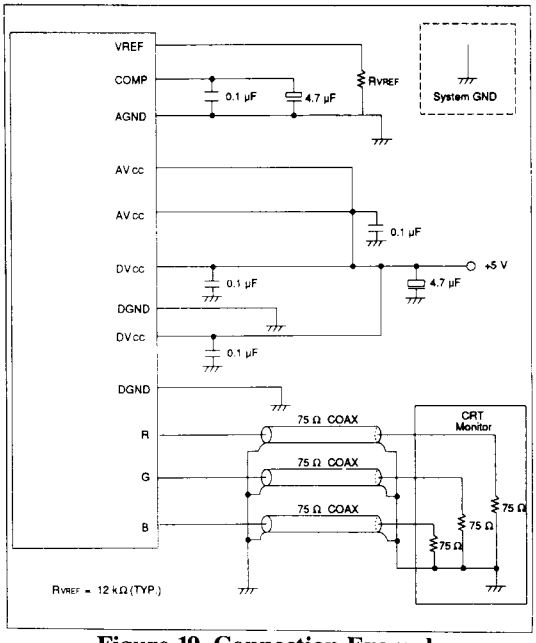



**Figure 19 Connection Example**