# HD14517B

#### Dual 64-bit Static Shift Register

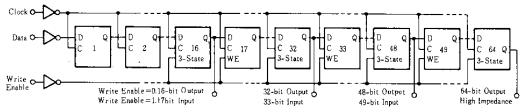
The HD14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48 and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

#### FEATURES

- Quiescent Current = 10nA/pkg typ. @5V
- Noise Immunity of  $V_{DD}$  typ.
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7MHz Operation @10V

BLOCK DIAGRAM(1/2)

- Exceedingly Slow Input Transition Rates May Be Apolied to the Clock Input
- 3-state Output at 64th-bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

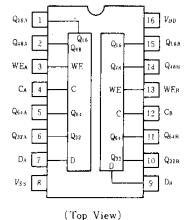


#### TRUTH TABLE

Clock	Write Enable	Data	16-bit Tap	32-bit Tap	48-bit Tap	64-bit Tap	
0	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed	
0	1	×	High Impedance	High Impedance	High Impedance	High Impedance	
1	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed	
1	1	×	High Impedance	High Impedance	High Impedance	High Impedance	
	0	Data entered into 1st Bit	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed	
_	1	Data entered into 1st Bit	Data at tap entered into 17-bit	Data at tap entered into 33-bit	Data at tap entered into 49-bit	High Impedance	
	0	×	Content of 16-bit Displayed	Content of 32-bit Displayed	Content of 48-bit Displayed	Content of 64-bit Displayed	
	1	× .	High Impedance	High Impedance	High Impedance	High Impedance	

x=Don't Care





Characteristic	Symbo	Test Conditions	-4	-40°C		25°C			85°C			
Characteristic		$V_{DD}(\mathbf{V})$	)	min	max	min	typ	max	min	max	Uni	
		5.0	$V_{in} = V_{DD}$ or 0	-	0.05		0	0.05	—	0.05	v	
	VOL	10		·	0.05	_	0	0.05		0.05		
Output Voltage		15			0.05		0	0.05		0.05		
compare transfer		5.0		4.95		4.95	5.0	_	4.95		v	
	V <sub>OH</sub>	10	$V_{in} = 0$ or $V_{DD}$	9.95		9.95	10		9.95	_		
		15		14.95		14.95	15		14.95			
		5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{ V}$	-	1.5	_	2.25	1.5	i —	1.5	v	
	VIL	10	$V_{out} = 9.0 \text{ or } 1.0 \text{ V}$		3.0	_	4.50	3.0		3.0		
Input Voltage		15	$V_{out} = 13.5$ or $1.5 \mathrm{V}$	i –	4.0		6.75	4.0		4.0		
input fortuge		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{ V}$	3.5	-	3.5	2.75	·	3.5		v	
	ViH	10	$V_{out} = 1.0 \text{ or } 9.0 \text{ V}$	7.0	_	7.0	5.50		7.0	_		
		15	$V_{out} = 1.5 \text{ or } 13.5 \text{ V}$	11.0	—	11.0	8.25	<u> </u>	11.0	-		
		5.0	$V_{OH} = 2.5 \mathrm{V}$	-1.0		-0.8	-1.7		~-0.6		mA	
	Іан	5.0	$V_{OH} = 4.6 \mathrm{V}$	-0.2		-0.16	-0.36	—	-0.12	—		
	10H	10	$V_{0H} = 9.5 \mathrm{V}$	-0.5	-	-0.4	0.9		-0.3	—		
Output Drive Current		15	$V_{0H} = 13.5 \mathrm{V}$	-1.4	<u> </u>	-1.2	-3.5		-1.0	-		
		5.0	$V_{0L} = 0.4 \mathrm{V}$	0.52		0.44	0.88		0.36	— .	mA	
	Iol	10	$V_{o_{\perp}} = 0.5 \mathrm{V}$	1.3	_	1,1	2.25		0.9	_		
		15	$V_{0L} = 1.5 \mathrm{V}$	3.6		3.0	8.8		2.4	—		
Input Current	Iin	15			±0.3		±0.00001	±0.3		±1.0	μA	
Input Capacitance	C		$V_{in} = 0$		-		5.0	7.5	-		pF	
		5.0	Zero Signal. per Package	—	50	—	0.010	50		375	μA	
Quiescent Current	Inn	10		_	100		0.020	100		750		
		15			200	_	0.030	200	_	1500		
		5.0	$Dynamic + I_{DD}$ ,		-	_	4.2	-	_	_	μA	
Total Supply Current*	Ir	10	per Gate	_	i —		8.8	-	-	_		
		15	$C_L = 50 \mathrm{pF}, \ f = 1 \mathrm{kHz}$		_		13.7		_	_	1	
Three-State Output Leakage Current	Ιτι	15			±1.0	_	±0.00001	±1.0		±7.5	μA	

#### **ELECTRICAL CHARACTERISTICS**

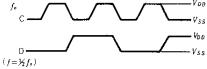
\* To calculate total supply current at frequency other than 1kHz.

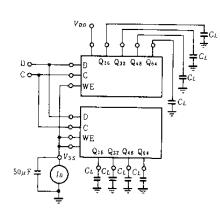
 $( W_{00} = 5.0 \text{ V } I_T - (4.2 \,\mu\text{A/kHz}) f + I_{0D}, \quad ( W_{00} = 10 \text{ V } I_T - (8.8 \,\mu\text{A/kHz}) f + I_{DD}, \quad ( W_{00} = 15 \text{ V } I_T - (13.7 \,\mu\text{A/kHz}) f + I_{0D}) f + I_{0D} f + I_{0D}$ 

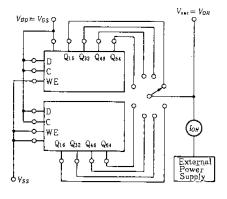
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### DC CHARACTERISTIC TEST CIRCUIT

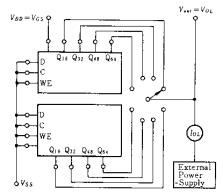














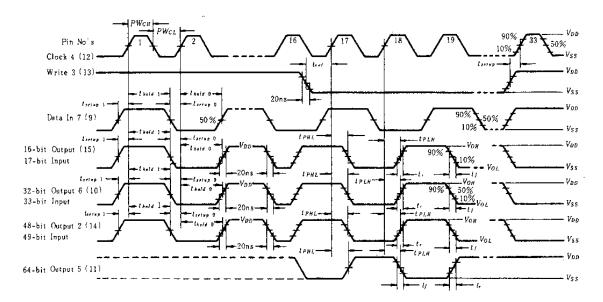
HD145178-

# **E**SWITCHING CHARACTERISTICS ( $C_L = 50 \text{pF}, Ta = 25^{\circ}\text{C}$ )

Characteristic	Symbol	$V_{DD}(\mathbf{V})$	min	typ	max	Unit
		5.0	<u> </u>	180	400	
Output Rise Time	t.,	10		90	200	ns
		15		65	160	
		5.0		100	200	
Dutput Fall Time	t,	10		50	100	ns
		15	_	37	80	1
	z	5.0		475	770	ns
Propagation Delay Time	ţ₽LH,	10		210	300	
	t <sub>PHL</sub>	15	_	140	215	]
		5.0	330	170	_	ns
Clock Pulse Width	$PW_{c}$	10	125	- 75		
		15	100	60		
	PRF	5.0	<u> </u>	3.0	1.5	MHz
Clock Frequency		10	_	6.7	4.0	
		15		8.3	5.3	1
	t., t <sub>j</sub>	5.0	*			
Clock Pulse Rise and Fall Time		10				
		15				
		5.0	0	-40	—	ns
Setup Time	taetup	10	10	-15		
		15	15	0	_	
		5.0	150	75		ns
Hold Time	troid	10	75	25	_	
		15	35	10	_	
		5.0	400	170		
Write Enable to Clock Setup Time	t se tup	10	200	65		ns
		15	110	50	-	1
		5.0	380	160		1
Write Enable to Clock Release Time	t +e t	10	180	55		ns
		15	100	40	_	1

\* When shift register sections are cascaded, the maxmum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

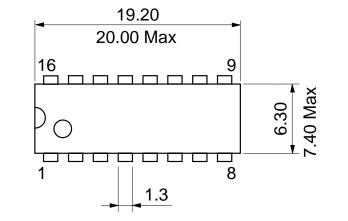
#### •DYNAMIC SIGNAL WAVEFORMS



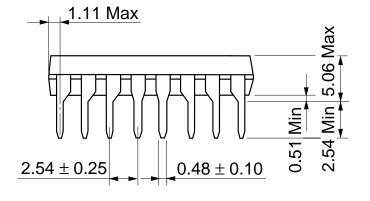


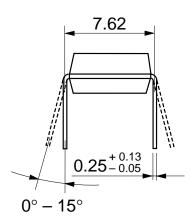


Unit: mm





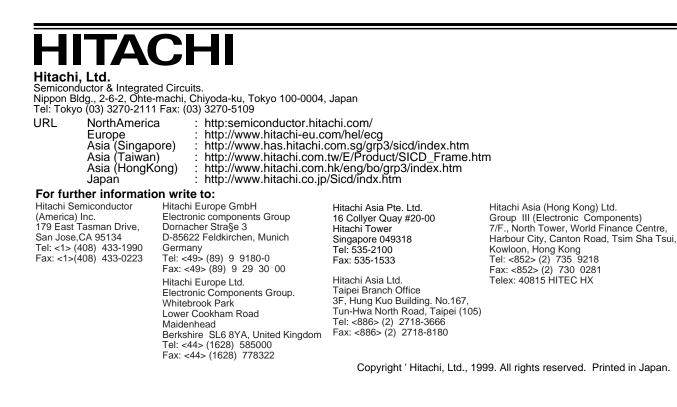




Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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