HD14516B

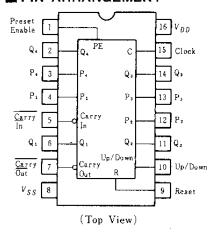
Binary Up/Down Counter

The HD14516B finds primary use where low power dissipation and/or high noise immunity is desired. This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

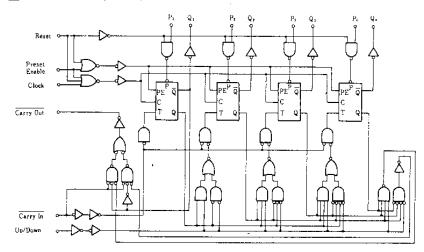
FEATURES

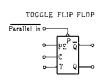
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V Internally Synchronous for High Speed
- Logic Edge-clocked Design ... Count Occurs on Positive Going Edge of Clock
- 6MHz Counting Rate (@10V)
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ PIN ARRANGEMENT



LOGIC DIAGRAM





Flip-flop Functional Truth Table

Preset Enable	Clock	Toggle Enable	Q,1		
1	×	×	Parallel in		
0		0	Q,		
0		1	Q,		
0		×	Q.		
x = Don't (Care		•		

TRUTH TABLE

Carry In	Up/Down	Preset Enable	Reset	Action
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	O	Count Down
X	Х	1	0	Preset
×	Х	×	1	Reset

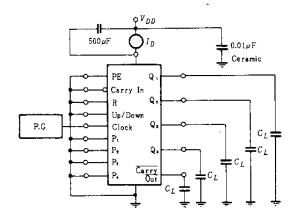
x=Don't Care

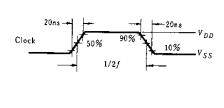
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions		-40°C		25 °C			85°C		Unit	
Character istic	Symbol	VDD(V)	Test Conditions	min	max	min	typ	max	min	max] Omt	
		5.0	$V_{in} = V_{DD}$ or 0	_	0.05	_	0	0.05	_	0.05	v	
	Vol	10		_	0.05	_	0	0.05	_	0.05		
Output Voltage		15			0.05	_	0	0.05	_	0.05		
output vollage		5.0		4.95	_	4.95	5.0		4.95	-		
	Voн	10	$V_{in}=0$ or V_{DD}	9.95		9.95	10		9.95	_	V	
		15		14.95	_	14.95	15		14.95	. –		
		5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$	_	1.5	_	2.25	1.5	_	1.5	v	
15	VIL	10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$	-	3.0	_	4.50	3.0	. –	3.0		
Input Voltage		15	$V_{out} = 13.5 \text{ or } 1.5 \text{V}$	_	4.0		6.75	4.0	_	4.0		
mput vortage		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$	3.5	_	3.5	2.75	_	3.5	-	V	
	V_{IH}	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0	_	7.0	5.50		7.0	_		
	ļ	15	$V_{\text{out}} = 1.5 \text{ or } 13.5 \text{V}$	11.0	-	11.0	8.25	_	11.0	_		
		5.0	$V_{OH} = 2.5 \mathrm{V}$	-1.0		-0.8	-1.7	_	-0.6	_	m A	
	Ţ	5.0	$V_{OH} = 4.6 \mathrm{V}$	-0.2		-0.16	-0.36	-	-0.12			
	Іон	10	$V_{OH} = 9.5 \mathrm{V}$	-0.5	_	-0.4	-0.9		-0.3			
Output Drive Current		15	$V_{OH} = 13.5 \text{ V}$	-1.4	-	-1.2	-3.5	_	-1.0	-		
		5.0	$V_{OL} = 0.4 \text{ V}$	0.52	_	0.44	0.88	_	0.36	_	m A	
	IoL	10	$V_{OL} = 0.5 \mathrm{V}$	1.3	_ '	1.1	2.25		0.9			
		15	$V_{0L} = 1.5 \text{ V}$	3.6	_	3.0	8.8	_	2.4	_		
Input Current	Iin.	15		-	±0.3	-	±0.00001	±0.3	_	±1.0	μA	
Input Capacitance	Cin	· –	$V_{in} = 0$	-	-	_	5.0	7.5	_	_	pF	
Quiescent Current		5.0	Zero Signal,	- '	20		0.005	20		150	μA	
	I_{DD}	10			40		0.010	40	_	300		
		15	per Package		80		0.015	80		600		
		5.0	Dynamic + I_{DD} , C_L = 50pF	_	_		0.58	_	_	-	<u> </u>	
Total Supply Current*	Iτ	10	f = 1 kHz,		_	_	1.2	_		_	μA	
		15	per Gate		_		1.7			-		

f * To calculate total supply current at frequency other than 1kHz.

■POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



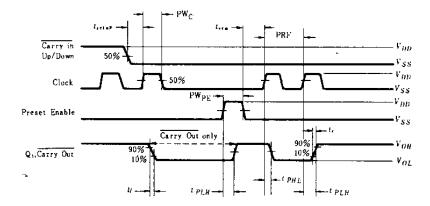


ESWITCHING CHARACTERISTICS ($C_L = 50 \text{pF}$, $Ta = 25 ^{\circ}\text{C}$)

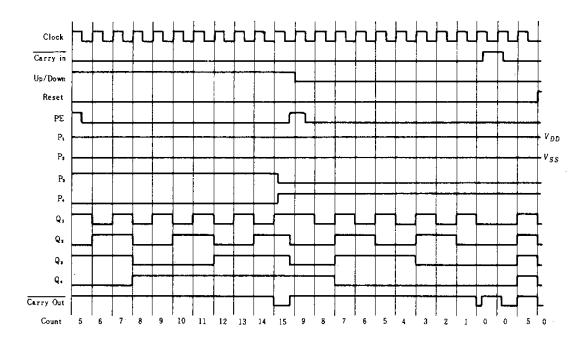
Chamata		Symbol	V _{DD} (V)	min	typ	max	Unit
Characteristic		Бунгоот	5.0	124111	180	360	Onit
Output Rise Time			10	_	90	180	
		t r	15	_	65	130	ns
			5.0	_	100	200	!
Out-of E-11 Wes-				-			
Output Fall Time		t_f	10		50	100	ns
			15		40	80	
			5.0		315	630	4
	Clock-to-Q		10	_	130	260	j
			15	_	100	200	
	Clock-to-		5.0	-	315	630	
	Carry Out		10	_	130	260	
			15	_	100	200]
	Carry In-	t PLH	5.0	-	180	360	
Propagation Delay	to-Carry	t PHL	10	-	80	160	ns
Time	Out		15		60	120	·
	Preset or		5.0	-	315	630	
	Reset -		10	<u> </u>	130	360	
	to-Q		15		100	300	1
	Preset or		5.0	_	550	1100	
	Reset-to-		10	_	225	450	
	Carry Out		15	_	150	300	
			5.0	400	200		
Clock Pulse Width		PW_C	10	200	100		ns
			15	150	75		
			5.0	_	3.0	1.5	
Clock Frequency		PRF	10	i	6.0	3.0	MHz
			15		8.0	4.0	
			5.0	650	325	_	
Preset or Reset Res	moval Time*	trem	10	230	115	-	ns
			15	180	90	_	
			5.0	_		15	
Clock Pulse Rise and	d Fall Time	t_{τ}, t_f	10		_	15	μs
			15		-	15	
			5.0	260	130		
Carry In Setup Time	e		10	120	60	<u> </u>	1
ourly in Setup Time			15	100	50	-	1
Up/Down Setup Time		t setup	5.0	500	250	 	ns
			10	200	100	 	†
			15	150	75	 	†
			5.0	200	100		
Preset Enable Pulse	Width	PW_{PE}	10	100	50		ns
2 - 2005 Emanic I diac it idill		- 775.6	15	80	40		113

^{*}The Preset or Reset Signal must be low prior to a positive-going transition of the clock.

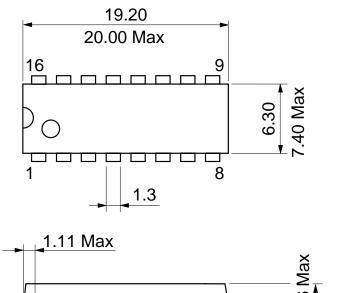
■ DYNAMIC SIGNAL WAVEFORMS



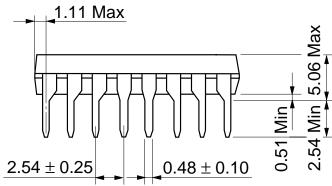
TIMING DIAGRAM

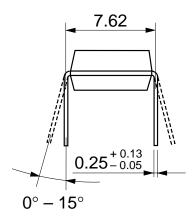


Unit: mm



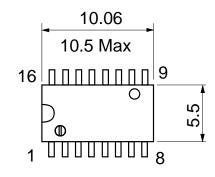


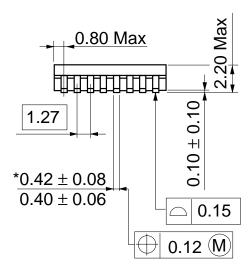




Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

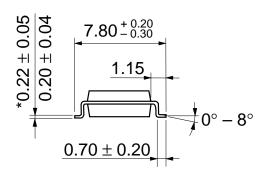
Unit: mm





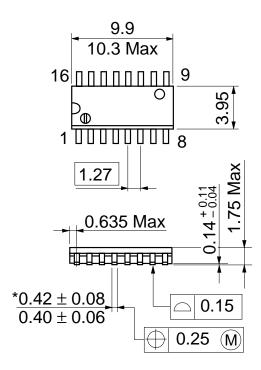
*Dimension including the plating thickness
Base material dimension



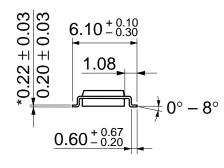


Hitachi Code	FP-16DA
JEDEC	
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose,CA 95134 Tel: <1> (408) 433-1990 Fax: <1>(408) 433-0223 Hitachi Europe GmbH Electronic components Group Dornacher Stra§e 3 D-85622 Feldkirchen, Munich Germany

Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd. Electronic Components Group Whitebrook Park Lower Cookham Road Maidenhead

Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533

Hitachi Asia Ltd. Taipei Branch Office

3F, Hung Kuo Building. No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281

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