

# HD14175B

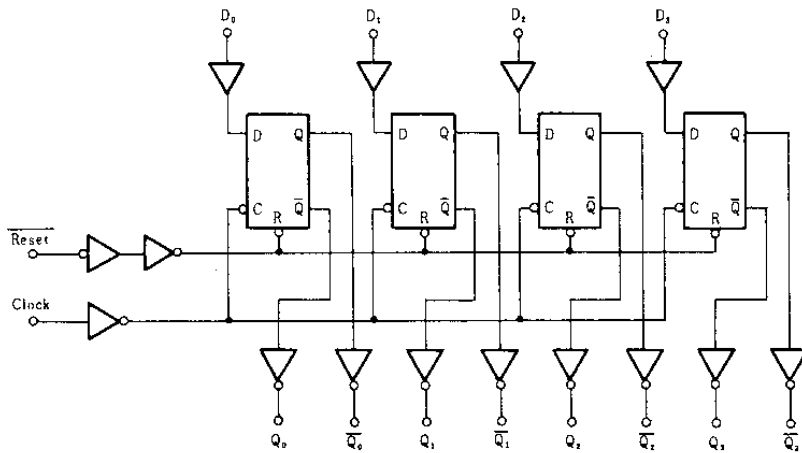
## Quadruple D-type Flip Flop

The HD14175B is quad type D flip-flop. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input (R) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and  $\bar{Q}$ ). This device may be used as shift register elements or as type T flip-flops for counter and toggle applications.

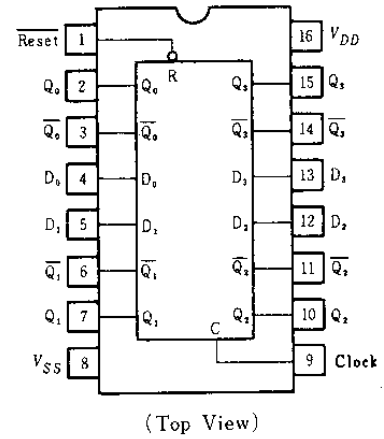
### FEATURES

- Supply Voltage Range = 3 to 18V
- Output Compatible with One Low-power Schottky TTL Load
- Functional Equivalent to TTL74175

### BLOCK DIAGRAM



### PIN ARRANGEMENT

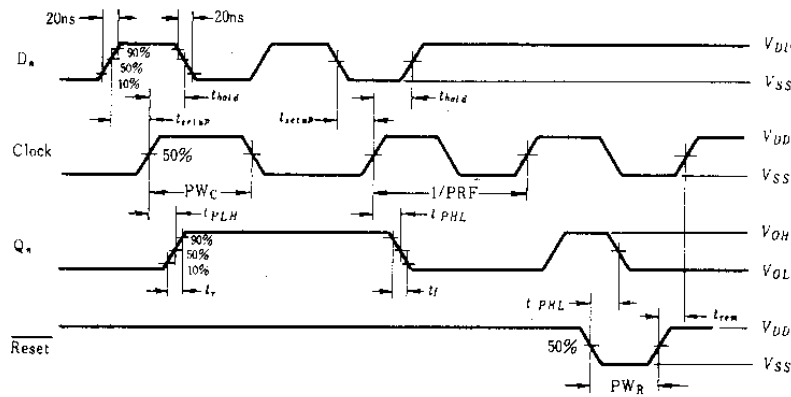


### TRUTH TABLE

Inputs			Output	
Clock	Data	Reset	Q	$\bar{Q}$
	0	1	0	1
	1	1	1	0
	x	1	Q	$\bar{Q}$
x	x	0	0	1

x = Don't Care

### DYNAMIC SIGNAL WAVEFORMS



## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	$V_{DD}$ (V)	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	$V_{OL}$	5.0	$V_{in} = V_{DD}$ or 0	-	0.05	-	0	0.05	-	0.05	V
		10		-	0.05	-	0	0.05	-	0.05	
		15		-	0.05	-	0	0.05	-	0.05	
	$V_{OH}$	5.0	$V_{in} = 0$ or $V_{DD}$	4.95	-	4.95	5.0	-	4.95	-	V
		10		9.95	-	9.95	10	-	9.95	-	
		15		14.95	-	14.95	15	-	14.95	-	
Input Voltage	$V_{IL}$	5.0	$V_{out} = 4.5$ or $0.5V$	-	1.5	-	2.25	1.5	-	1.5	V
		10	$V_{out} = 9.0$ or $1.0V$	-	3.0	-	4.50	3.0	-	3.0	
		15	$V_{out} = 13.5$ or $1.5V$	-	4.0	-	6.75	4.0	-	4.0	
	$V_{IH}$	5.0	$V_{out} = 0.5$ or $4.5V$	3.5	-	3.5	2.75	-	3.5	-	V
		10	$V_{out} = 1.0$ or $9.0V$	7.0	-	7.0	5.50	-	7.0	-	
		15	$V_{out} = 1.5$ or $13.5V$	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current	$I_{OH}$	5.0	$V_{OH} = 2.5V$	-2.5	-	-2.1	-4.2	-	-1.7	-	mA
		5.0	$V_{OH} = 4.6V$	-0.52	-	-0.44	-0.88	-	-0.36	-	
		10	$V_{OH} = 9.5V$	-1.3	-	-1.1	-2.25	-	-0.9	-	
		15	$V_{OH} = 13.5V$	-3.6	-	-3.0	-8.8	-	-2.4	-	
	$I_{OL}$	5.0	$V_{OL} = 0.4V$	0.52	-	0.44	0.88	-	0.36	-	mA
		10	$V_{OL} = 0.5V$	1.3	-	1.1	2.25	-	0.9	-	
15		$V_{OL} = 1.5V$	3.6	-	3.0	8.8	-	2.4	-		
Input Current	$I_{in}$	15		-	$\pm 0.3$	-	$\pm 0.00001$	$\pm 0.3$	-	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{in}$	-	$V_{in} = 0$	-	-	-	5.0	7.5	-	-	pF
Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	-	20	-	0.0005	20	-	150	$\mu A$
		10		-	40	-	0.0010	40	-	300	
		15		-	80	-	0.0015	80	-	600	
Total Supply Current*	$I_T$	5.0	Dynamic $+I_{DD}$ , $C_L = 50pF$	-	-	-	1.7	-	-	-	$\mu A$
		10	$f = 1kHz$	-	-	-	3.4	-	-	-	
		15	per Gate	-	-	-	5.0	-	-	-	

\* To calculate total supply current at frequency other than 1kHz.

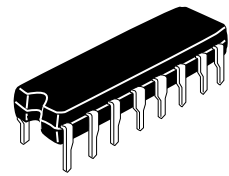
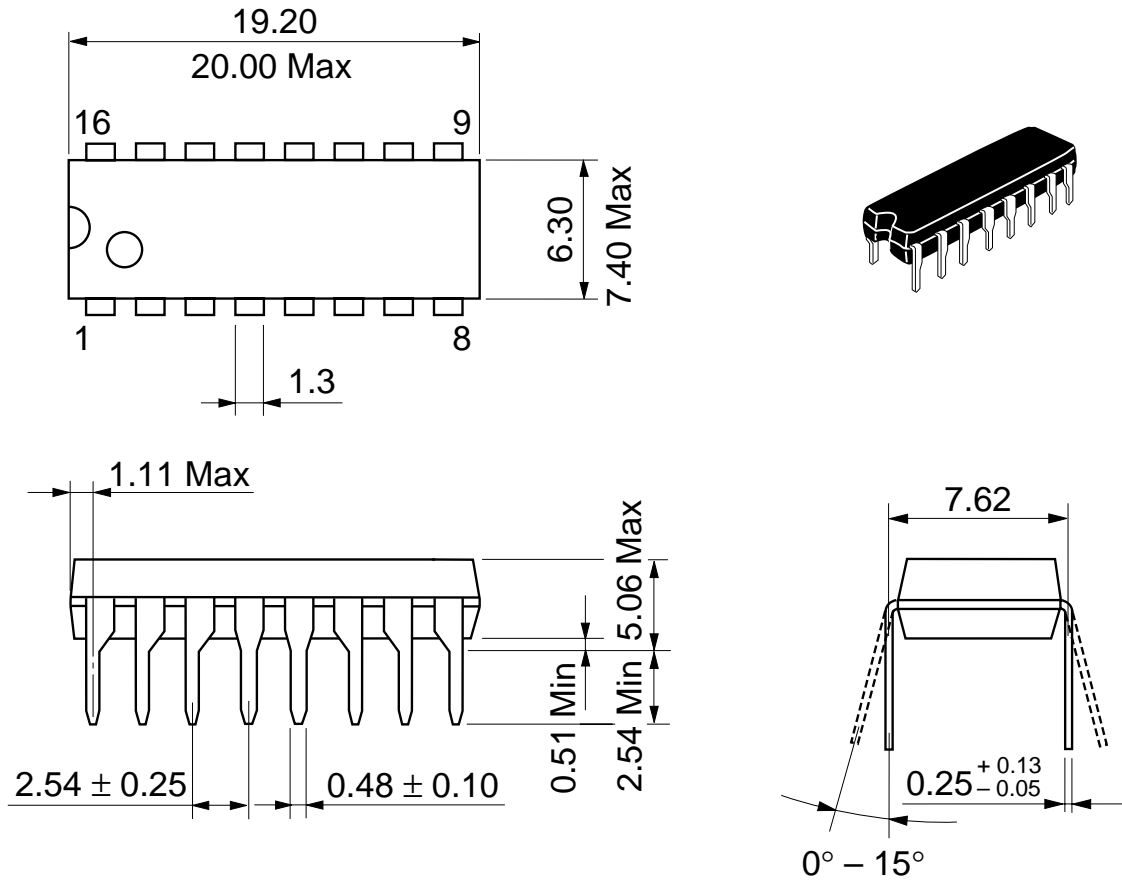
@  $V_{DD} = 5.0V$   $I_T = (1.7 \mu A/kHz) f + I_{DD}$  @  $V_{DD} = 10V$   $I_T = (3.4 \mu A/kHz) f + I_{DD}$  @  $V_{DD} = 15V$   $I_T = (5.0 \mu A/kHz) f + I_{DD}$

**SWITCHING CHARACTERISTICS** ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise and Fall Time		$t_r, t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Clock	$t_{PLH}$ $t_{PHL}$	5.0	—	220	420	ns
			10	—	90	170	
			15	—	70	130	
	Reset	$t_{PHL}$	5.0	—	325	650	ns
			10	—	130	260	
			15	—	100	200	
Clock Pulse Width	$PW_C$	5.0	250	110	—	ns	
		10	100	45	—		
		15	75	35	—		
Reset Pulse Width	$PW_R$	5.0	200	100	—	ns	
		10	80	40	—		
		15	60	30	—		
Clock Frequency	$PRF$	5.0	—	4.5	2.0	MHz	
		10	—	11	5.0		
		15	—	14	6.5		
Clock Pulse Rise and Fall Time	$t_r, t_f$	5.0	—	—	15	$\mu\text{s}$	
		10	—	—	15		
		15	—	—	15		
Setup Time	$t_{setup}$	5.0	120	60	—	ns	
		10	50	25	—		
		15	40	20	—		
Hold Time	$t_{hold}$	5.0	80	40	—	ns	
		10	40	20	—		
		15	30	15	—		
Reset Removal Time	$t_{rem}$	5.0	250	125	—	ns	
		10	100	50	—		
		15	80	40	—		

\* The reset signal must be high prior to a positive-going transition of the clock.

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
                 Europe                     : <http://www.hitachi-eu.com/hel/ecg>  
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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher StraÙe 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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