HD14160B, HD14161B HD14162B, HD14163B

HD14160B......Decade Counter with Asynchronous Clear

HD14161B 4-bit Binary Counter with Asynchronous Clear

HD14162B..... Decade Counter with Synchronous Clear

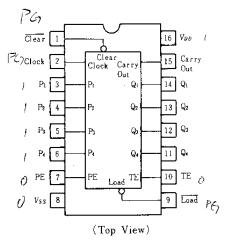
HD14163B 4-bit Binary Counter with Synchronous Clear

The HD14160B to HD14163B are synchronous programmable counters and functionally equivalent to the 74160 to 74163 TTL counters. Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (HD14160B, HD14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (HD14161B, HD14163B).

■ FEATURES

- Internal Look-Ahead for Fast Counting
- Carry Output for N-bit Cascading
- Synchronously Programmable
- Synchronous Counting
- · Load Control Line
- Synchronous or Asynchronous Clear Positive Edge Clocked

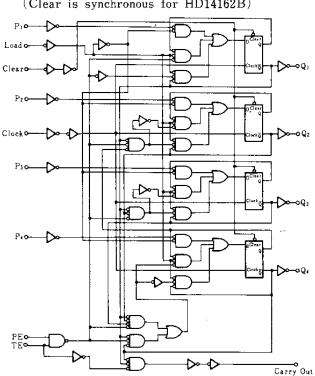
■ PIN ARRANGEMENT



■ LOGIC DIAGRAM

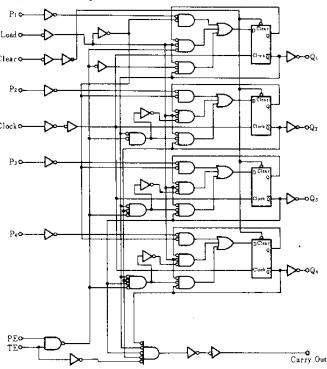
HD14160B, HD14162B

(Clear is synchronous for HD14162B)



HD14161B, HD14163B

(Clear is Synchronous for HD14163B)



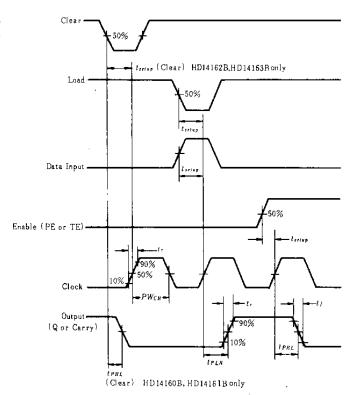
■ ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	−40 °C		25°C			85°C			
		$V_{DD}(V)$	V _{DD} (V)	min	max	min	typ	max	min	max	Unit
Output Voltage		5.0	$V_{i\pi} = V_{DD}$ or 0	_	0.05	_	0	0.05		0.05	v
	Vol	10			0.05		0	0.05		0.05	
		15		_	0.05	_	0	0.05		0.05	
	V_{OH}	5.0	$V_{in}{=}0$ or V_{DD}	4.95	_	4.95	5.0		4.95		
		10		9.95		9.95	10	_	9.95	_] v
		15		14.95		14.95	15	_	14.95	_	
Input Voltage	V_{tL}	5.0	$V_{out} = 4.5 \text{ or } 0.5\text{V}$	_	1.5		2.25	1.5	_	1.5	v
		10	$V_{out} = 9.0 \text{ or } 1.0 \text{V}$	-	3.0	_	4.50	3.0		3.0	
		15	$V_{out} = 13.5 \text{ or } 1.5 \text{V}$	-	4.0	_	6.75	4.0		4.0	
		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$	3.5		3.5	2.75	_	3.5	-	v
	V_{IH}	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0	_	7.0	5.50		7.0]	
		15	$V_{out} = 1.5 \text{ or } 13.5 \text{V}$	11.0	_	11.0	8.25	_	11.0	_	
		5.0	$V_{OH}=2.5V$	-2.5	-	-2.1	-4.2	_	-1.7	_	- mA
Output Drive Current	Іон	5.0	$V_{OH}=4.6V$	-0.52	. —	-0.44	-0.88		-0.36	_]	
		10	$V_{OH} = 9.5 \text{V}$	-1.3		-1.1	-2.25	. —	-0.9		
		15	$V_{OH}=13.5V$	-3.6		-3.0	-8.8		-2.4	_]	
	Ior	5.0	$V_{oL}=0.4V$	0.52		0.44	0.88	_	0.36	_	mA
		10	$V_{OL} = 0.5 \text{V}$	1.3		1.1	2.25	_	0.9	_	
		15	$V_{OL}=1.5V$	3.6	_	3.0	8.8		2.4		
Input Current	I.	15		_	±0.3	_	±0.00001	±0.3	_	±1.0	μΑ
Input Capacitance	Cin		$V_{in} = 0$	_	_	_	5.0	7.5			pF
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	_	20		0.005	20		150	
		10		_	40	_	0.010	40		300	μA
		15		_	80		0.015	80	_	600	
Total Supply Current*	I_{T}	5.0	Dynamic $+I_{DD}$,] —	_		0.56		_	_	μA
		10	per Gate, $C_L = 50 \mathrm{pF}$	-			1.1	. —	_		
		15	f=1kHz			_	1.9				

 $[\]bigstar$ To calculate total supply current at frequency other than $1k\mathrm{Hz},$

@ V_{DD} =5.0V I_{7} =(0.56 μ A/kHz) $f+I_{DD}$, @ V_{DD} =10V I_{7} =(1.1 μ A/kHz) $f+I_{DD}$, @ V_{DD} =15V I_{7} =(1.9 μ A/kHz) $f+I_{DD}$

■ DYNAMIC SIGNAL WAVEFORMS



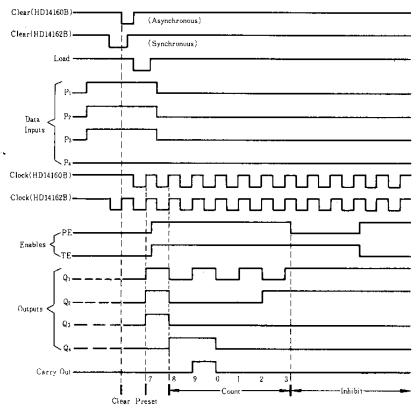


■ SWITCHING CHARACTERICS ($C_L = 50 \,\mathrm{pF}, T_a = 25 \,^{\circ}\mathrm{C}$)

Characteristic		$V_{DD}(V)$	min	typ	max	Unit
	t,	5.0	-	100	200	
		10	_	50	100	ns
			-	40	80	1
Output Fall Time		5.0		100	200	ns
		10	-	50	100	
			_	40	80	ĺ
		5.0	_	350	700	ns
Clock to Q		10	_	150	300	
		15	_	100	200	
Clock to Carry Out		5.0		440	880	
		10	_	185	370	
	tplH,	15	_	125	250	
	t_{PHL}	5.0	_	300	600	
TE to Carry Out		10		130	260	
		15	_	90	180	
Clear to Q (HD14160B, HD14161Bonly)		5.0	-	155	310	
		10	_	55	110	
		15	_	35	70	
		5.0	320	160	-	ns
Data to Clock	t setup	10	130	65	<u> </u>	
		15	90	45		
Load to Clock		5.0	600	300		
			<u> </u>			
		15	180		_	
Enable to Clock (PE or TE)						
		10	170			
		15	120	60		
Clear to Clock (HD14162B, HD14163B only)						
		10	110			
		15				
Clock Pulse Width		+	250			ns
		-				
						
Clock Rise Time				_	 	μs
					 	
		-				
Clock Frequency					 	MHz
		10		5.0	2.5	
on a regional				LI A LI	. 4.1	171114
	Clock to Q Clock to Carry Out TE to Carry Out Clear to Q (HD14160B, HD14161Bonly) Data to Clock Load to Clock Enable to Clock (PE or TE) Clear to Clock (HD14162B, HD14163Bonly)	Clock to Q Clock to Carry Out tplh, tphL TE to Carry Out Clear to Q (HD14160B, HD14161Bonly) Data to Clock Load to Clock (PE or TE) Clear to Clock (HD14162B, HD14163Bonly)	t. 10 15 5.0 t 10 15 5.0 t 10 15 5.0 10 15 15 5.0 10 15 15 5.0 10 15 15 15 15 15 15 1	t. 10 15 10 15 10 15	1. 10	t, 10 100 200

■ TIMING DIAGRAM

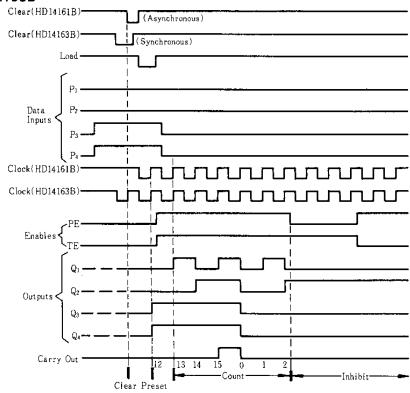
● HD14160B, HD14162B



Sequence illustrated in waveforms:

- 1. Clear outputs to zero. 3. Count to eight, nine, zero, one, two, and three.
- 2. Preset to BCD seven. 4. Inhibit

●HD14161B, HD14163B

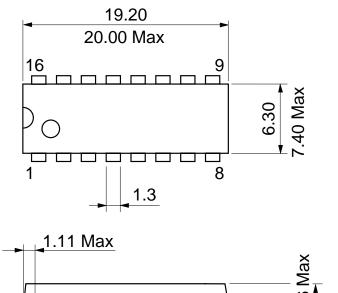


Sequence illustrated in waveforms:

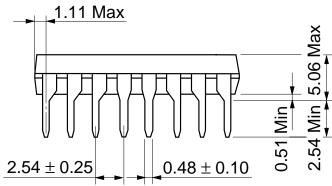
- 1. Clear outputs to zero. 3. Count to thirteen, fourteen, fifteen, zero, one, and two.
- 2. Preset to binary twelve. 4. Inhibit

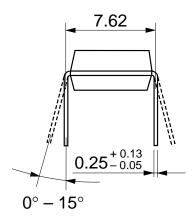


Unit: mm









Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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