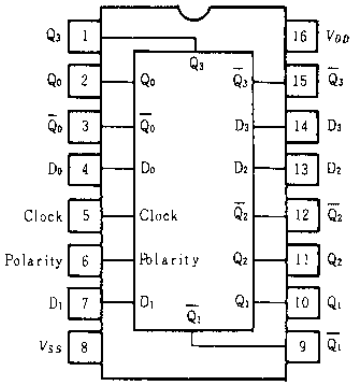
Quadruple Latch

The HD14042B quad latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

■ PIN ARRANGEMENT

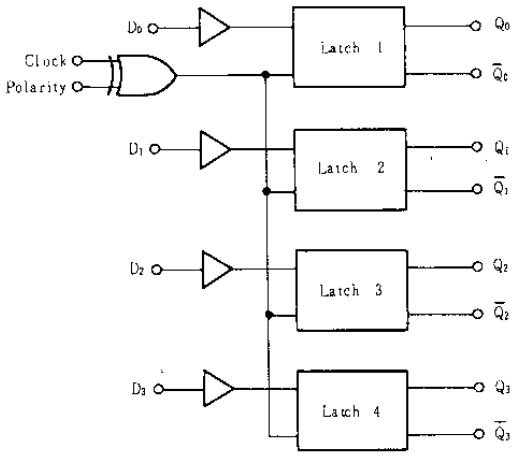


(Top View)

■ FEATURES

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and $\overline{Q}$ Outputs
- Quiescent Current = 2nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range

■ LOGIC DIAGRAM

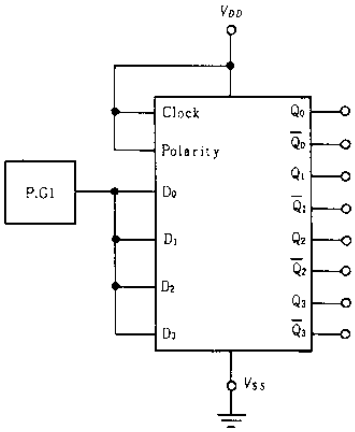


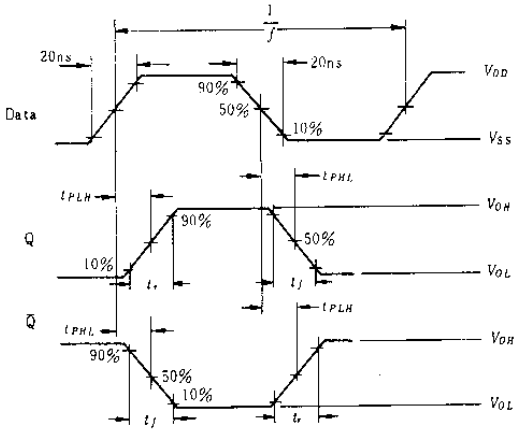
■ TRUTH TABLE

Clock	Polarity	Q
0	0	Data
⌐	0	Latch
1	1	Data
⌙	1	Latch

■ DC CHARACTERISTIC TEST CIRCUIT

(Data to Q, $\overline{Q}$)





For Power Dissipation test, each output is loaded with capacitance C_L.

■ ELECTRICAL CHARACTERISTICS

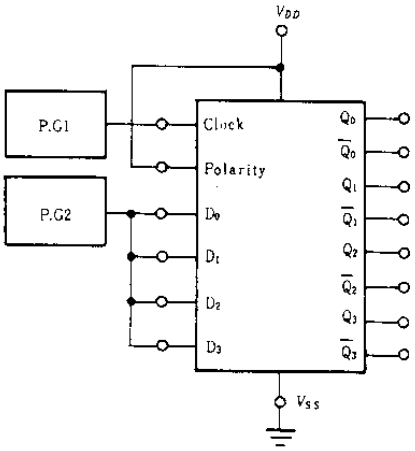
Characteristic		Symbol	V_{DD}(V)	Test Conditions	−40℃ min	−40℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Output Voltage		V_{OL}	5.0	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V
			10		—	0.05	—	0	0.05	—	0.05	
			15		—	0.05	—	0	0.05	—	0.05	
		V_{OH}	5.0	$V_{in}=0$ or V_{DD}	4.95	—	4.95	5.0	—	4.95	—	V
			10		9.95	—	9.95	10	—	9.95	—	
			15		14.95	—	14.95	15	—	14.95	—	
Input Voltage	Data	V_{IL}	5.0	V_{out}= 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	V
			10	V_{out}= 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
			15	V_{out}=13.5 or 1.5V	—	4.0	—	6.75	4.0	—	4.0	
	Clock Polarity		5.0	V_{out}= 4.5 or 0.5V	—	1.5	—	2.25	1.5	—	1.5	
			10	V_{out}= 9.0 or 1.0V	—	3.0	—	4.50	3.0	—	3.0	
			15	V_{out}=13.5 or 1.5V	—	3.75	—	6.75	3.75	—	3.75	
	Data	V_{IH}	5.0	V_{out}= 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	V
			10	V_{out}= 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
			15	V_{out}= 1.5 or 13.5V	11.0	—	11.0	8.25	—	11.0	—	
	Clock Polarity		5.0	V_{out}= 0.5 or 4.5V	3.5	—	3.5	2.75	—	3.5	—	
			10	V_{out}= 1.0 or 9.0V	7.0	—	7.0	5.50	—	7.0	—	
			15	V_{out}= 1.5 or 13.5V	11.25	—	11.25	8.25	—	11.25	—	
Output Drive Current		I_{OH}	5.0	V_{OH}= 2.5V	−1.0	—	−0.8	−1.7	—	−0.6	—	mA
			5.0	V_{OH}= 4.6V	−0.2	—	−0.16	−0.36	—	−0.12	—	
			10	V_{OH}= 9.5V	−0.5	—	−0.4	−0.9	—	−0.3	—	
			15	V_{OH}=13.5V	−1.4	—	−1.2	−3.5	—	−1.0	—	
		I_{OL}	5.0	V_{OL}= 0.4V	0.52	—	0.44	0.88	—	0.36	—	
			10	V_{OL}= 0.5V	1.3	—	1.1	2.25	—	0.9	—	
			15	V_{OL}= 1.5V	3.6	—	3.0	8.8	—	2.4	—	
Input Current		I_{in}	15		—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance		C_{in}	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current		I_{DD}	5.0	Zero Signal, per Package	—	4.0	—	0.002	4.0	—	30	μA
			10		—	8.0	—	0.004	8.0	—	60	
			15		—	16	—	0.006	16	—	120	
Total Supply Current*		I_T	5.0	Dynamic + I_{DD}, per Gate C_L=50pF, f=1kHz	—	—	—	1.0	—	—	—	μA
			10		—	—	—	2.0	—	—	—	
			15		—	—	—	3.0	—	—	—	

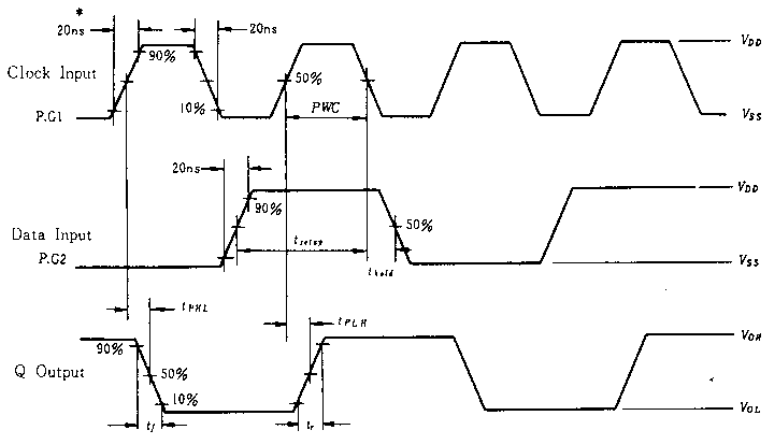
* To calculate total supply current at frequency other than 1kHz.
@V_{DD}=5.0V $I_T=(1.0\,\mu A/kHz)f+I_{DD}$, @$V_{DD}$=10V $I_T=(2.0\,\mu A/kHz)f+I_{DD}$, @$V_{DD}$=15V $I_T=(3.0\,\mu A/kHz)f+I_{DD}$

■SWITCHING CHARACTERISTICS (C_L=50pF, Ta=25℃)

Characteristic		Symbol	V_{DD} (V)	min	typ	max	Unit
Output Rise Time		t_r	5.0	—	180	360	ns
			10	—	90	180	
			15	—	65	130	
Output Fall Time		t_f	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Data to Q, $\overline{Q}$	t_{PLH}, t_{PHL}	5.0	—	220	440	ns
			10	—	90	180	
			15	—	60	120	
	Clock to Q, $\overline{Q}$		5.0	—	220	440	
			10	—	90	180	
			15	—	60	120	
Clock Pulse Width		PW_C	5.0	300	150	—	ns
			10	100	50	—	
			15	80	40	—	
Clock Rise Time		t_r	5.0	No Limit			
			10				
			15				
Hold Time		t_{hold}	5.0	100	50	—	ns
			10	50	25	—	
			15	40	20	—	
Setup Time		t_{setup}	5.0	50	0	—	ns
			10	30	0	—	
			15	25	0	—	

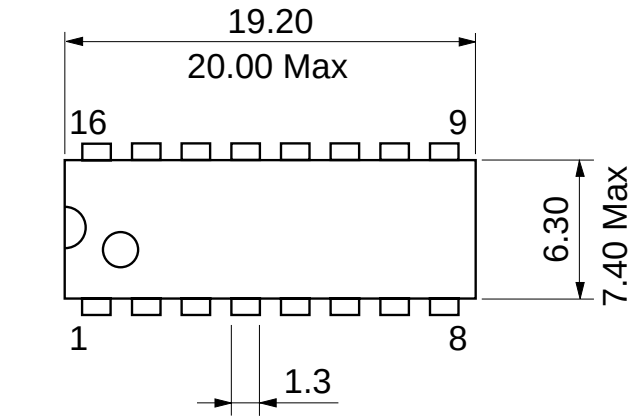
■AC TEST CIRCUIT (Clock to Q)

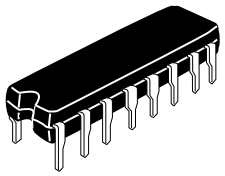


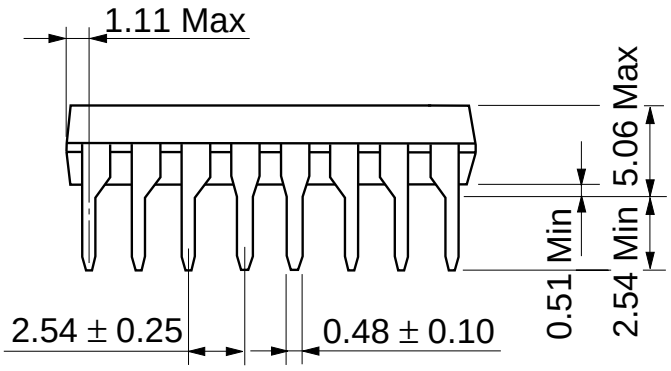


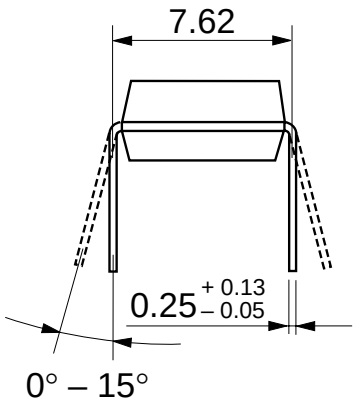
* Input clock rise time is 20ns except for maximum

Unit: mm



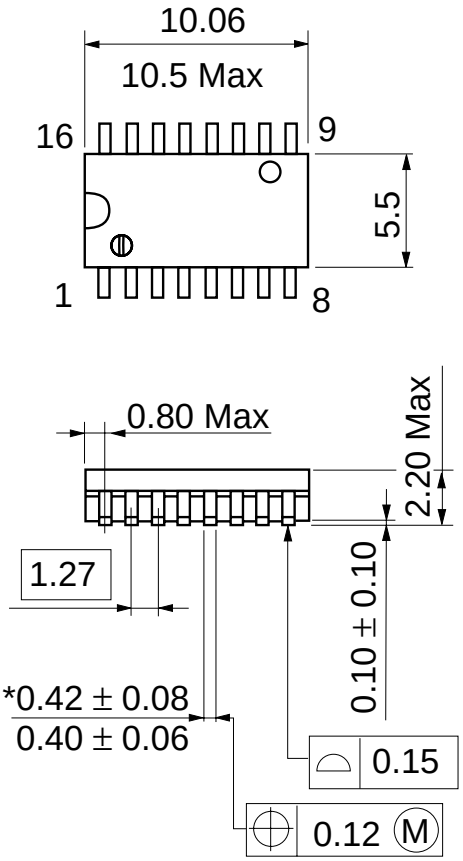


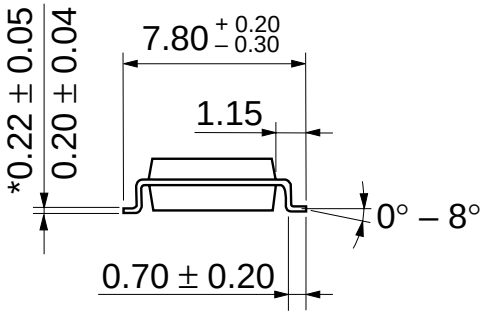


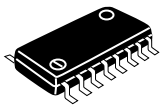


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm



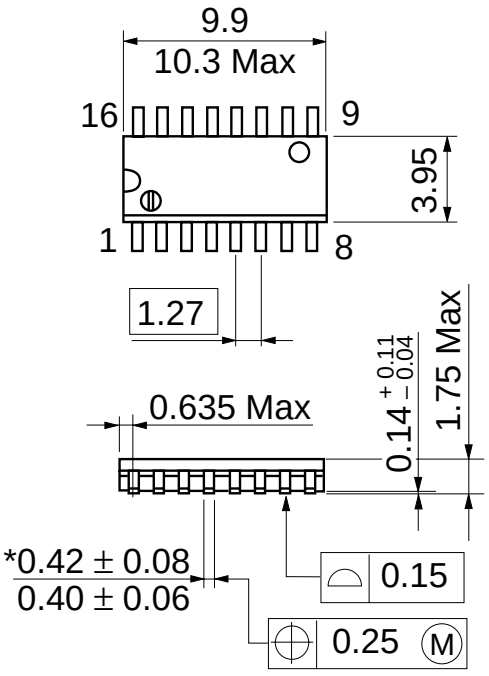


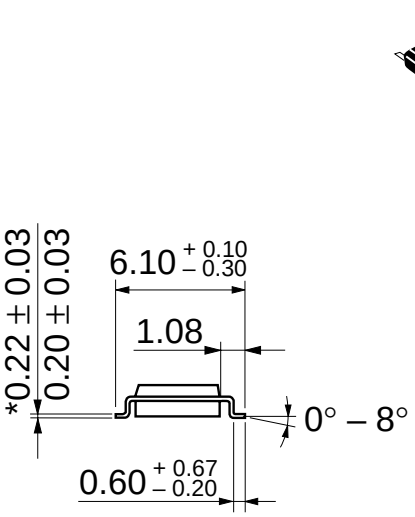


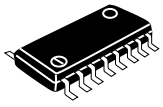
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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