### Silicon P-Channel MOS FET

# HITACHI

#### Application

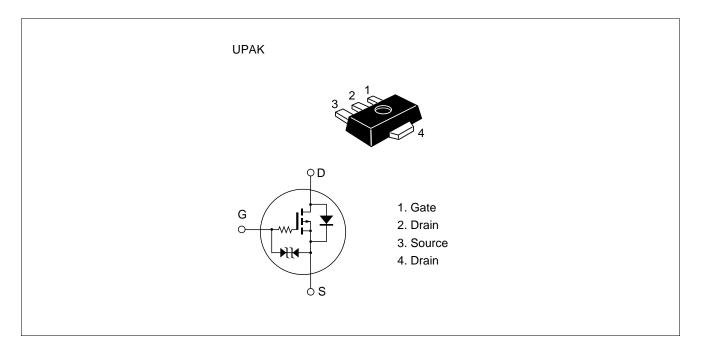
High speed power switching

Low voltage operation

#### Features

- Very low on-resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

#### Outline





#### **Absolute Maximum Ratings** ( $Ta = 25^{\circ}C$ )

| Item                                      | Symbol           | Ratings     | Unit |  |
|---|------------------|-------------|------|--|
| Drain to source voltage                   | V <sub>DSS</sub> | -12         | V    |  |
| Gate to source voltage                    | V <sub>GSS</sub> | -7          | V    |  |
| Drain current                             | I <sub>D</sub>   | ±2          | А    |  |
| Drain peak current                        | l★1<br>D(pulse)  | ±4          | А    |  |
| Body to drain diode reverse drain current | I <sub>DR</sub>  | 2           | А    |  |
| Channel dissipation                       | Pch*2            | 1           | W    |  |
| Channel temperature                       | Tch              | 150         | °C   |  |
| Storage temperature                       | Tstg             | -55 to +150 | °C   |  |

Notes: 1.  $PW \le 100 \ \mu s$ , duty cycle  $\le 10\%$ 

2. Value on the alumina ceramic board (12.5×20×0.7 mm).

3. Marking is "NY".

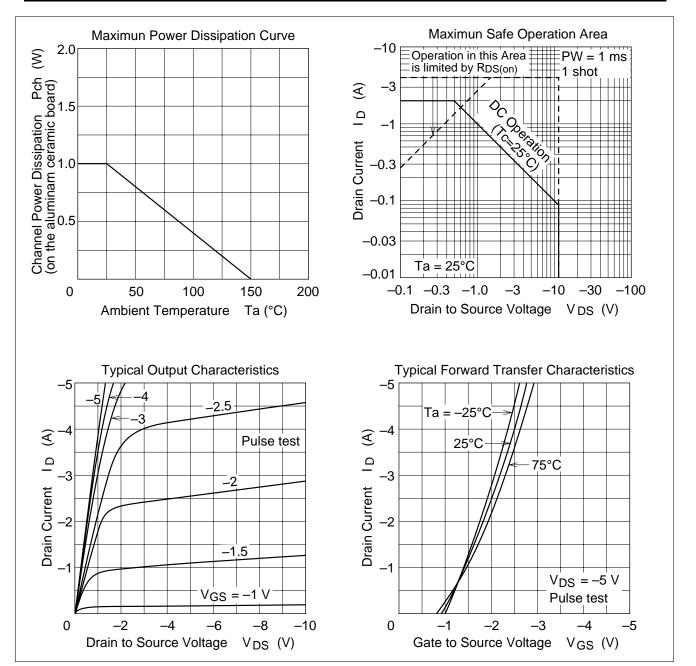
#### **Electrical Characteristics** (Ta = 25°C)

| Item                              | Symbol                      | Min  | Тур  | Max  | Unit | Test conditions  |
|-----------------------------------|-----------------------------|------|------|------|------|--|
| Drain to source breakdown voltage | $V_{(\text{BR})\text{DSS}}$ | -12  | _    | _    | V    | $I_{\rm D} = -1 \text{ mA}, V_{\rm GS} = 0$                        |
| Gate to source breakdown voltage  | $V_{(BR)GSS}$               | ±7   | _    | _    | V    | $I_{g} = \pm 10 \ \mu A, \ V_{DS} = 0$                             |
| Gate to source cutoff current     | I <sub>GSS</sub>            |      |      | ±5   | μΑ   | $V_{GS} = \pm 6.5 \text{ V}, V_{DS} = 0$                           |
| Zero gate voltage drain current   | I <sub>DSS</sub>            | —    | _    | -1   | μΑ   | $V_{\rm DS} = -8 \ V, \ V_{\rm GS} = 0$                            |
| Gate to source cutoff voltage     | $V_{\text{GS(off)}}$        | -0.4 |      | -1.4 | V    | $I_{\rm D} = -100 \ \mu A, \ V_{\rm DS} = -5 \ V$                  |
| Static drain to source on state   | $R_{DS(on)1}$               | _    | 0.4  | 0.7  | Ω    | $I_{\rm D} = -0.5 \ {\rm A^{*1}}, \ V_{\rm GS} = -2.2 \ {\rm V}$   |
| resistance                        | R <sub>DS(on)2</sub>        | —    | 0.28 | 0.35 | Ω    | $I_{\rm D} = -1 \ {\rm A}^{*1}, \ {\rm V}_{\rm GS} = -4 \ {\rm V}$ |
| Forward transfer admittance       | y <sub>fs</sub>             | 1.0  | 2.3  | _    | S    | $I_{\rm D} = -1 \ {\rm A}^{*1}, \ {\rm V}_{\rm DS} = -5 \ {\rm V}$ |
| Input capacitance                 | Ciss                        | _    | 63   | _    | pF   | $V_{\rm DS} = -5 \ V, \ V_{\rm GS} = 0,$                           |
| Output capacitance                | Coss                        | _    | 180  |      | pF   | f = 1 MHz  |
| Reverse transfer capacitance      | Crss                        | _    | 23   | _    | pF   |  |
| Turn-on time                      | t <sub>on</sub>             | _    | 500  | _    | ns   | $I_{\rm D} = -0.2 \ {\rm A^{*1}}, \ {\rm Vin} = -4 \ {\rm V},$     |
| Turn-off time                     | t <sub>off</sub>            | —    | 2860 | _    | ns   | $R_{L} = 51 \Omega$  |

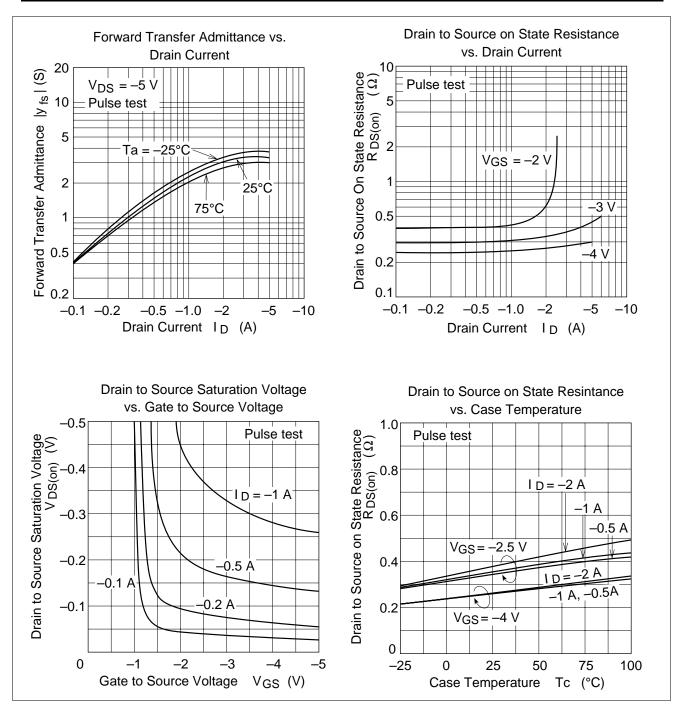
Note: 1. Pulse test

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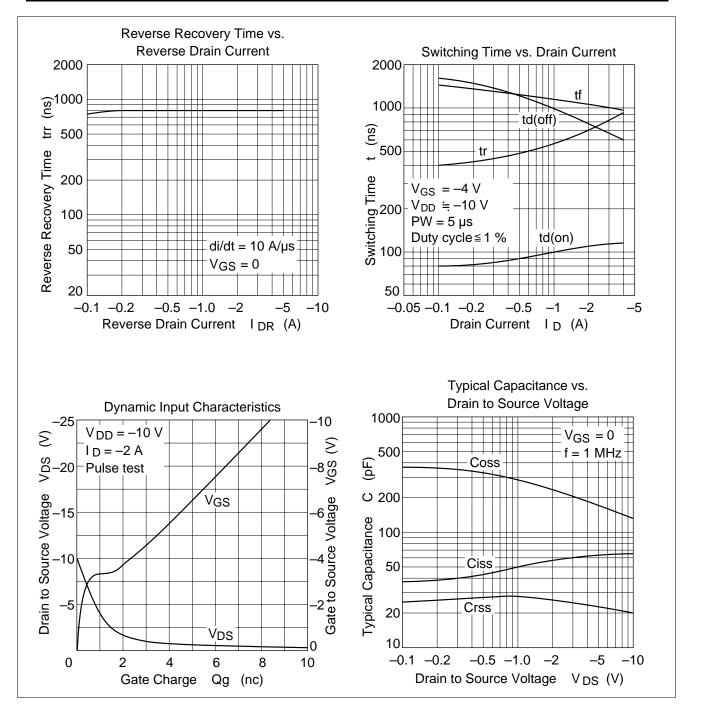


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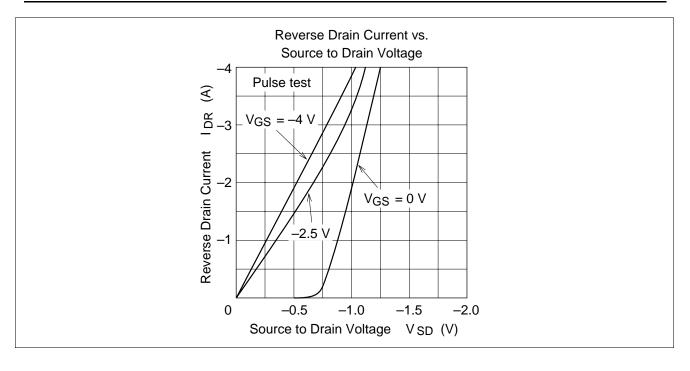


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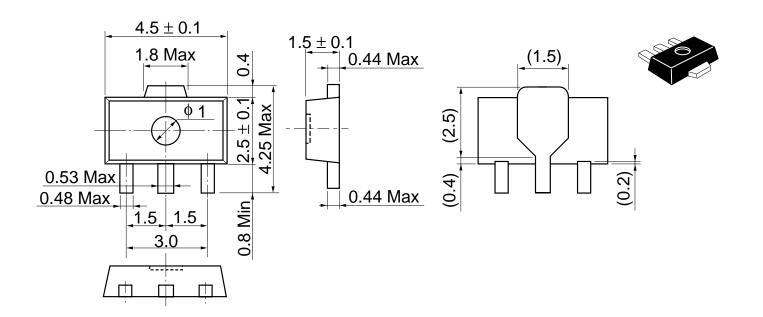
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Unit: mm



| Hitachi Code             | UPAK     |
|--------------------------|----------|
| JEDEC                    |          |
| EIAJ                     | Conforms |
| Weight (reference value) | 0.050 g  |

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