The RF MOSFET Line

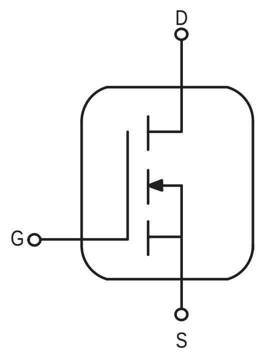
RF Power Field Effect Transistor

N–Channel Enhancement–Mode Lateral MOSFET

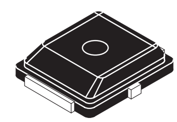
MRF1518T1

The MRF1518T1 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  Output Power — 8 Watts
  Power Gain — 11 dB
  Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- RF Power Plastic Surface Mount Package
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



**520 MHz, 8 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET**



**CASE 466–02, STYLE 1
(PLD–1.5)**

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	62.5 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

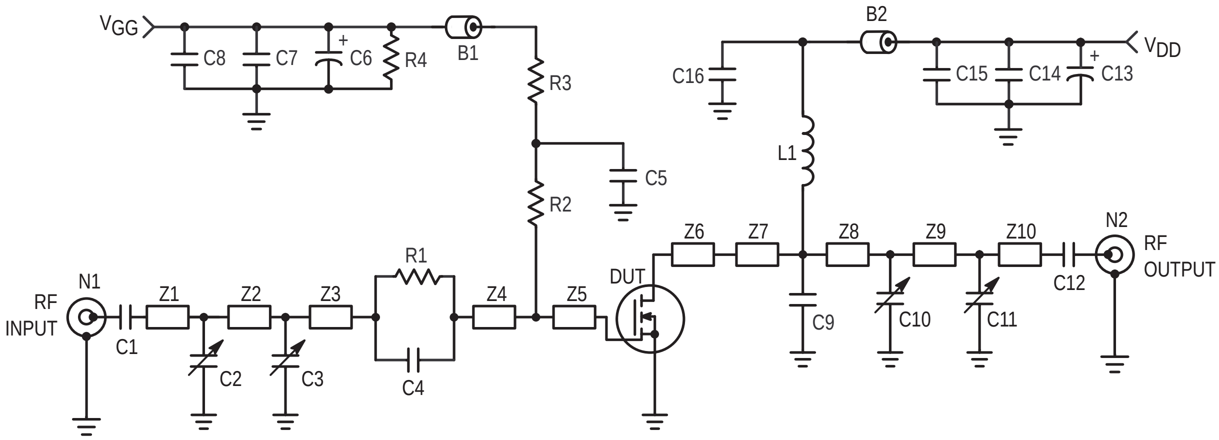
(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 40 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 100 μA)	$V_{GS(th)}$	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.4	—	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	66	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	33	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.5	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)	R4	33 kΩ, 1/8 W Resistor
C1, C14	240 pF, 100 mil Chip Capacitor	Z1	0.451″ x 0.080″ Microstrip
C2, C3, C10, C11	0 to 20 pF, Trimmer Capacitor	Z2	1.005″ x 0.080″ Microstrip
C4	82 pF, 100 mil Chip Capacitor	Z3	0.020″ x 0.080″ Microstrip
C5, C16	120 pF, 100 mil Chip Capacitor	Z4	0.155″ x 0.080″ Microstrip
C6, C13	10 μF, 50 V Electrolytic Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitor	Z7	0.065″ x 0.080″ Microstrip
C8, C15	0.1 μF, 100 mil Chip Capacitor	Z8	0.266″ x 0.080″ Microstrip
C9	30 pF, 100 mil Chip Capacitor	Z9	1.113″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z10	0.433″ x 0.080″ Microstrip
N1, N2	Type N Flange Mount	Board	Glass Teflon®, 31 mils, 2 oz. Copper
R1	15 Ω, 0805 Chip Resistor		
R2	51 Ω, 1/2 W Resistor		
R3	10 Ω, 0805 Chip Resistor		

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

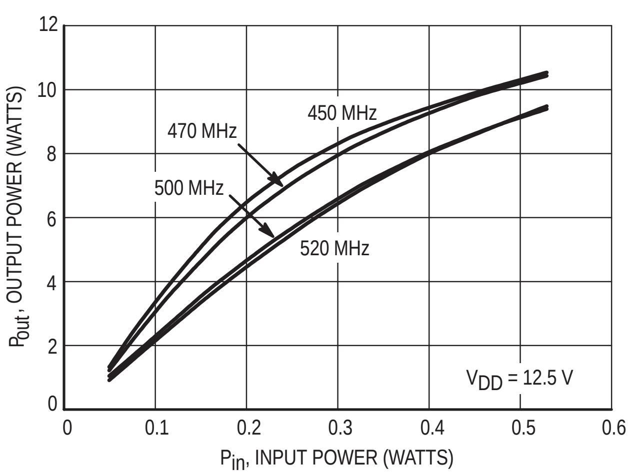


Figure 2. Output Power versus Input Power

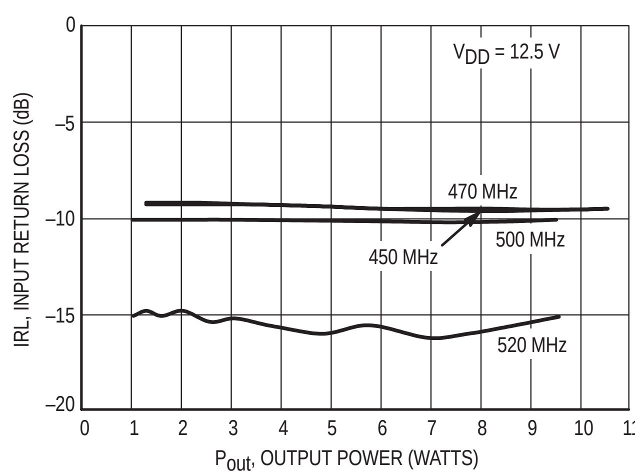


Figure 3. Input Return Loss versus Output Power

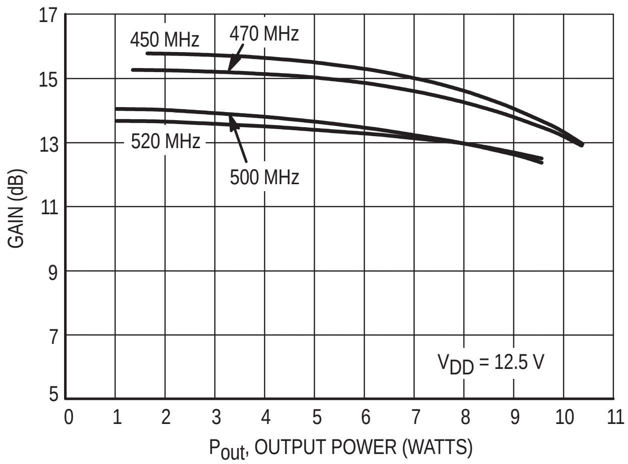


Figure 4. Gain versus Output Power

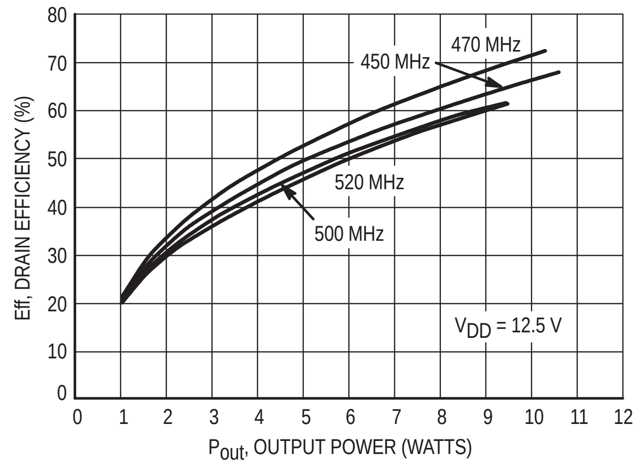


Figure 5. Drain Efficiency versus Output Power

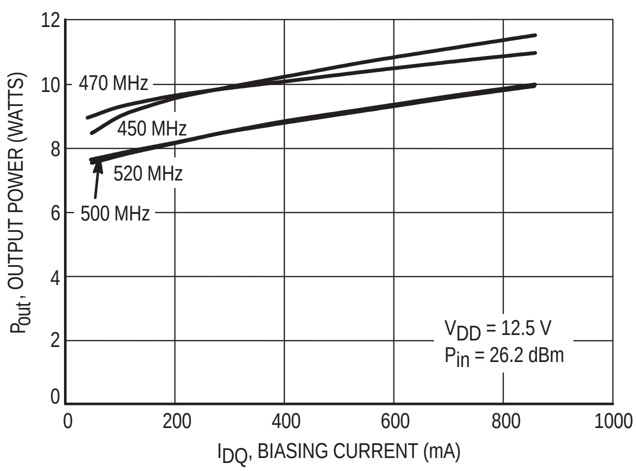


Figure 6. Output Power versus Biasing Current

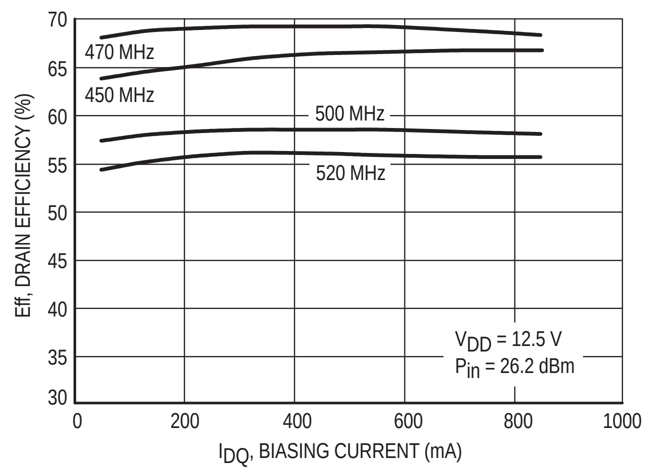


Figure 7. Drain Efficiency versus Biasing Current

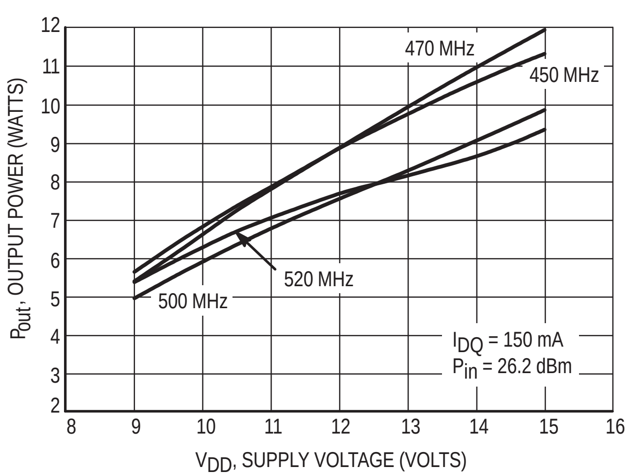


Figure 8. Output Power versus Supply Voltage

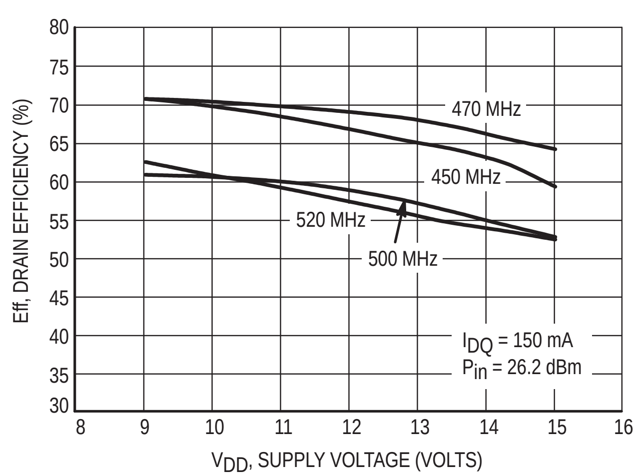
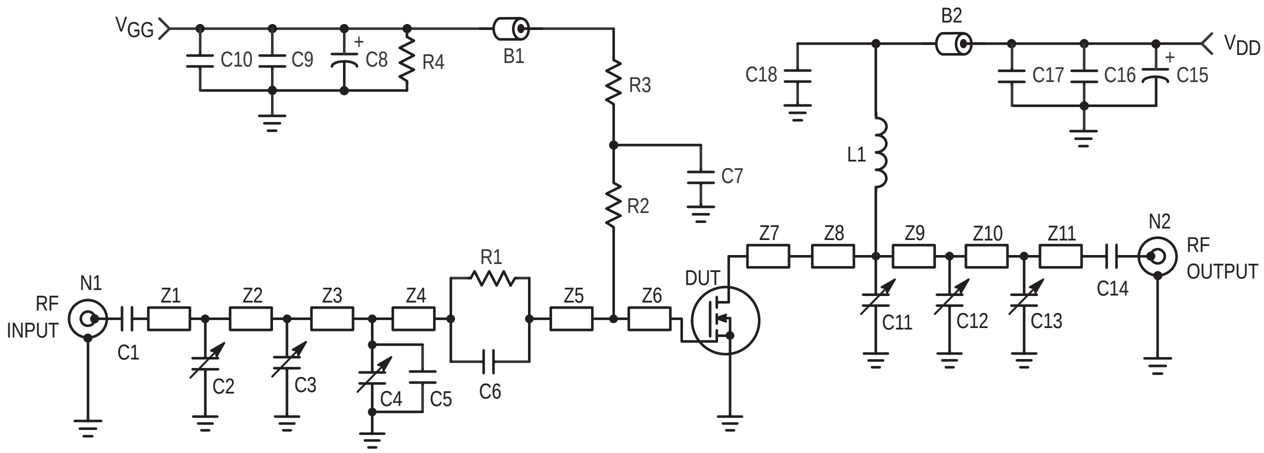


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)
C1, C14	240 pF, 100 mil Chip Capacitor
C2, C3, C4, C11, C12, C13	0 to 20 pF, Trimmer Capacitor
C5	30 pF, 100 mil Chip Capacitor
C6	47 pF, 100 mil Chip Capacitor
C7, C18	120 pF, 100 mil Chip Capacitor
C8, C15	10 μF, 50 V Electrolytic Capacitor
C9, C16	1,200 pF, 100 mil Chip Capacitor
C10, C17	0.1 μF, 100 mil Chip Capacitor
L1	55.5 nH, 5 Turn, Coilcraft
N1, N2	Type N Flange Mount
R1	15 Ω, 0805 Chip Resistor
R2	51 Ω, 1/2 W Resistor

R3	10 Ω, 0805 Chip Resistor
R4	33 kΩ, 1/8 W Resistor
Z1	0.476″ x 0.080″ Microstrip
Z2	0.724″ x 0.080″ Microstrip
Z3	0.348″ x 0.080″ Microstrip
Z4	0.048″ x 0.080″ Microstrip
Z5	0.175″ x 0.080″ Microstrip
Z6, Z7	0.260″ x 0.223″ Microstrip
Z8	0.239″ x 0.080″ Microstrip
Z9	0.286″ x 0.080″ Microstrip
Z10	0.806″ x 0.080″ Microstrip
Z11	0.553″ x 0.080″ Microstrip
Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

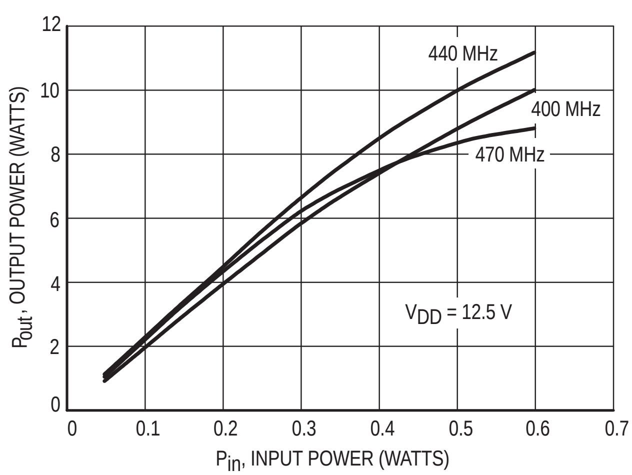


Figure 11. Output Power versus Input Power

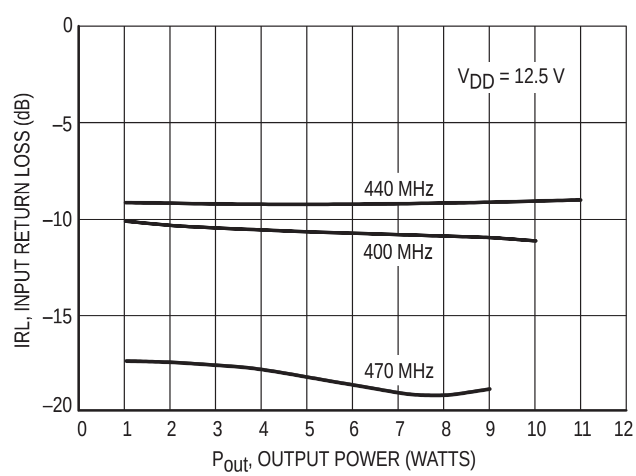


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 470 MHz

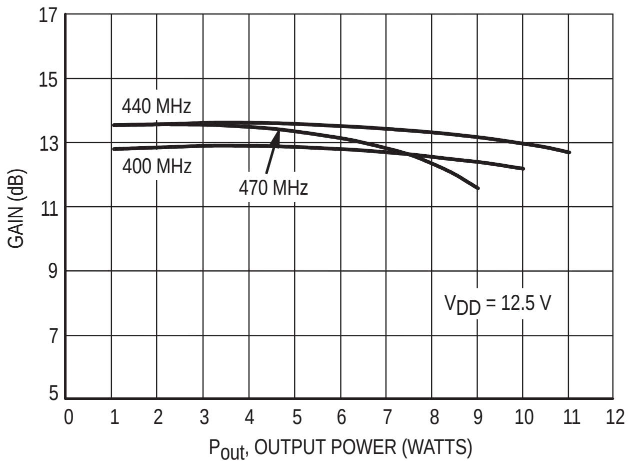


Figure 13. Gain versus Output Power

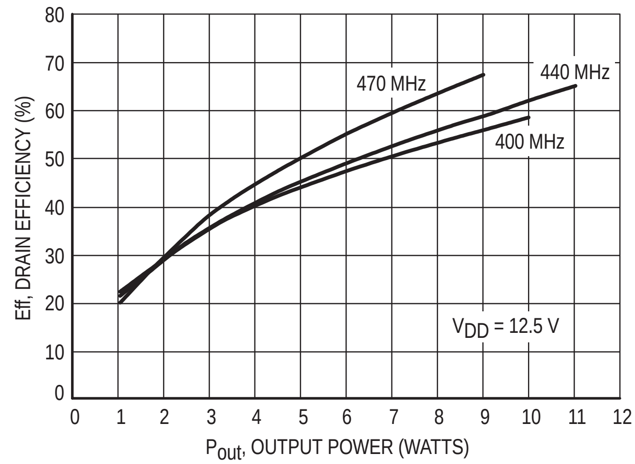


Figure 14. Drain Efficiency versus Output Power

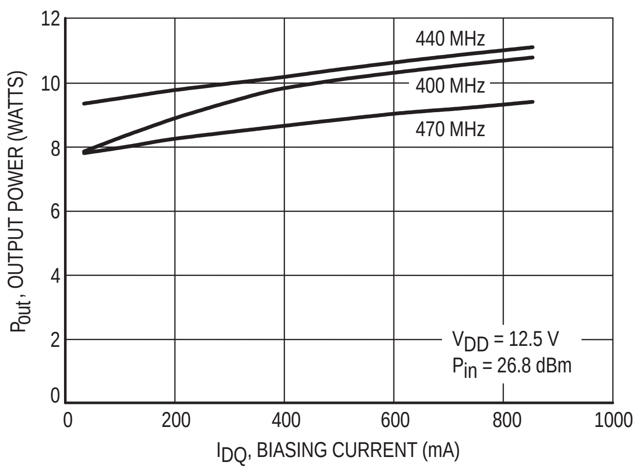


Figure 15. Output Power versus Biasing Current

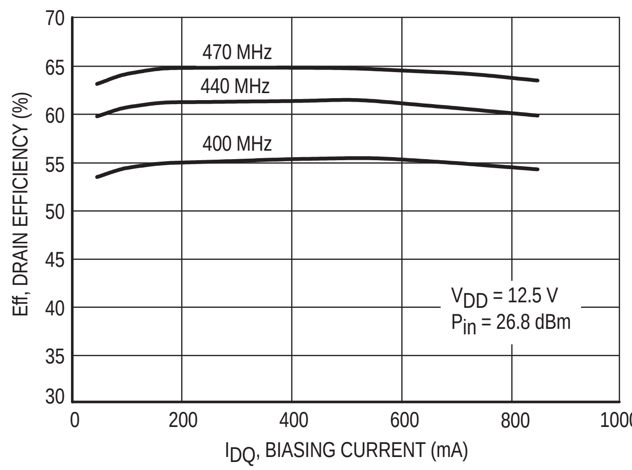


Figure 16. Drain Efficiency versus Biasing Current

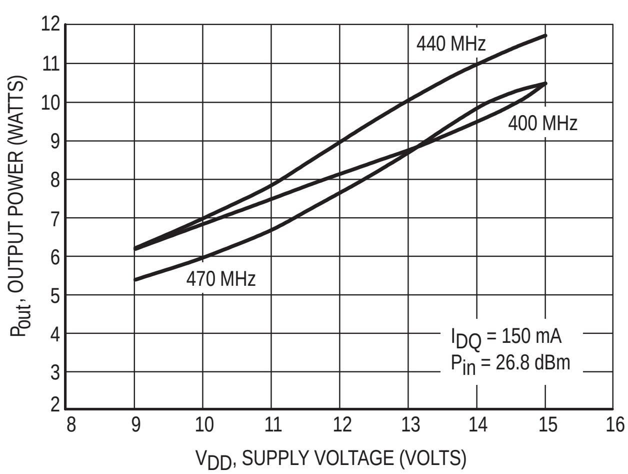


Figure 17. Output Power versus Supply Voltage

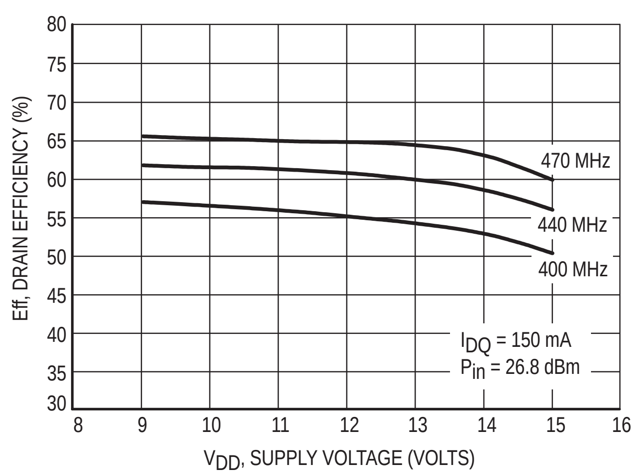
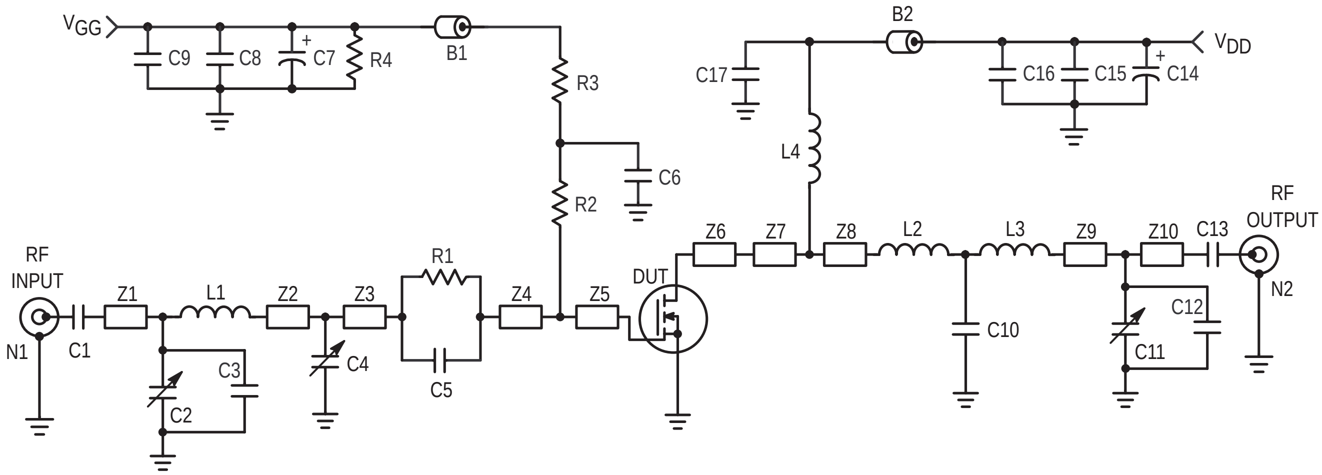


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Bead, Fair Rite Products (2743021446)
C1, C13	330 pF, 100 mil Chip Capacitor
C2, C4, C11	0 to 20 pF, Trimmer Capacitor
C3	12 pF, 100 mil Chip Capacitor
C5	43 pF, 100 mil Chip Capacitor
C6, C17	75 pF, 100 mil Chip Capacitor
C7, C14	10 μF, 50 V Electrolytic Capacitor
C8, C15	1,200 pF, 100 mil Chip Capacitor
C9, C16	0.1 μF, 100 mil Chip Capacitor
C10	75 pF, 100 mil Chip Capacitor
C12	13 pF, 100 mil Chip Capacitor
L1	26 nH, 4 Turn, Coilcraft
L2	5 nH, 2 Turn, Coilcraft
L3	33 nH, 5 Turn, Coilcraft
L4	55.5 nH, 5 Turn, Coilcraft
N1, N2	Type N Flange Mount
R1	15 Ω, 0805 Chip Resistor
R2	56 Ω, 1/4 W Carbon Resistor
R3	100 Ω, 0805 Chip Resistor
R4	33 kΩ, 1/8 W Carbon Resistor
Z1	0.115″ x 0.080″ Microstrip
Z2	0.255″ x 0.080″ Microstrip
Z3	1.037″ x 0.080″ Microstrip
Z4	0.192″ x 0.080″ Microstrip
Z5, Z6	0.260″ x 0.223″ Microstrip
Z7	0.125″ x 0.080″ Microstrip
Z8	0.962″ x 0.080″ Microstrip
Z9	0.305″ x 0.080″ Microstrip
Z10	0.155″ x 0.080″ Microstrip
Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

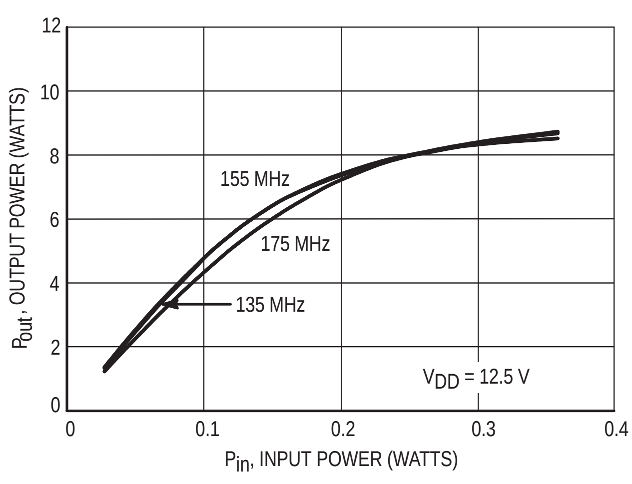


Figure 20. Output Power versus Input Power

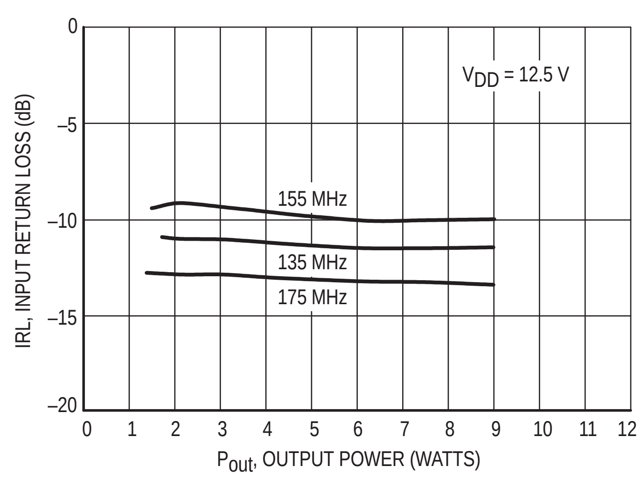


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

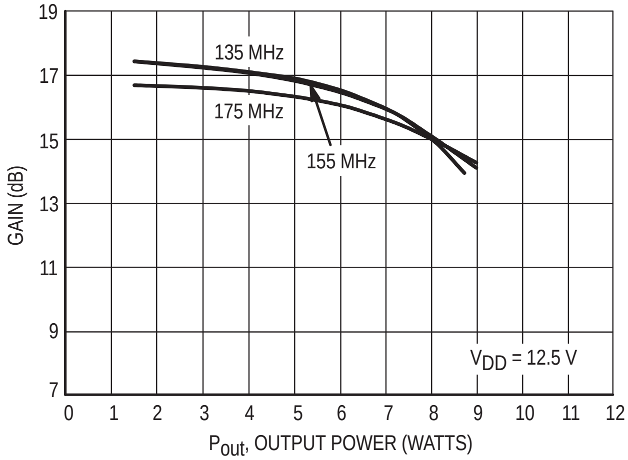


Figure 22. Gain versus Output Power

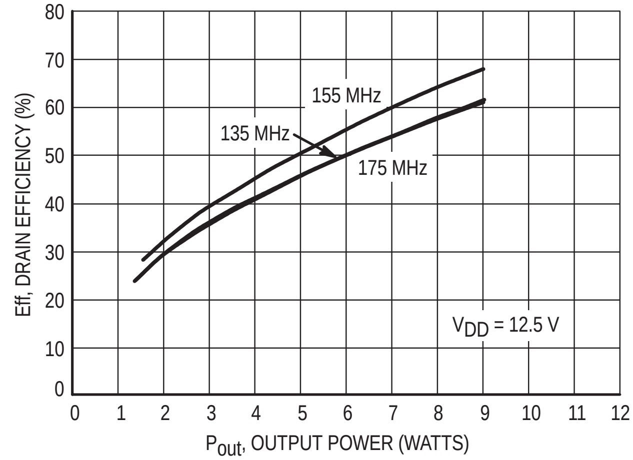


Figure 23. Drain Efficiency versus Output Power

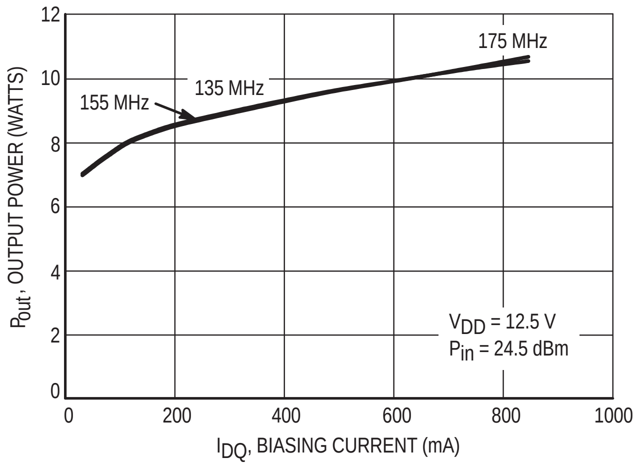


Figure 24. Output Power versus Biasing Current

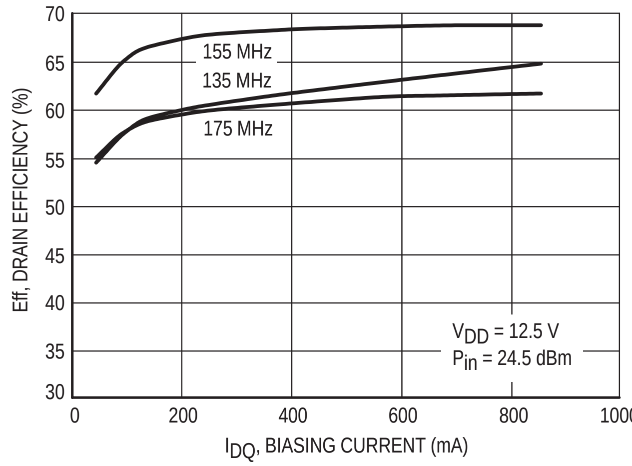


Figure 25. Drain Efficiency versus Biasing Current

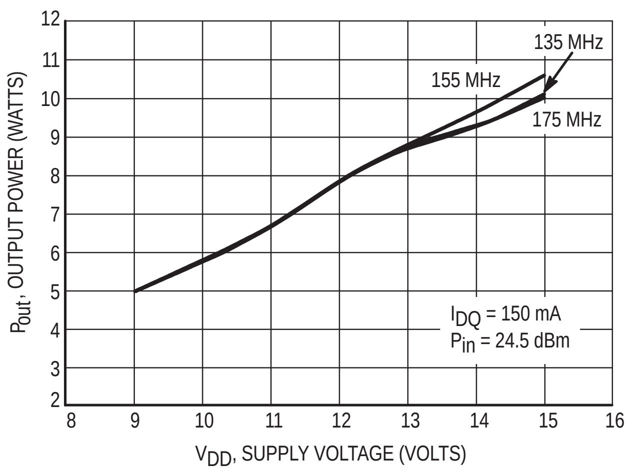


Figure 26. Output Power versus Supply Voltage

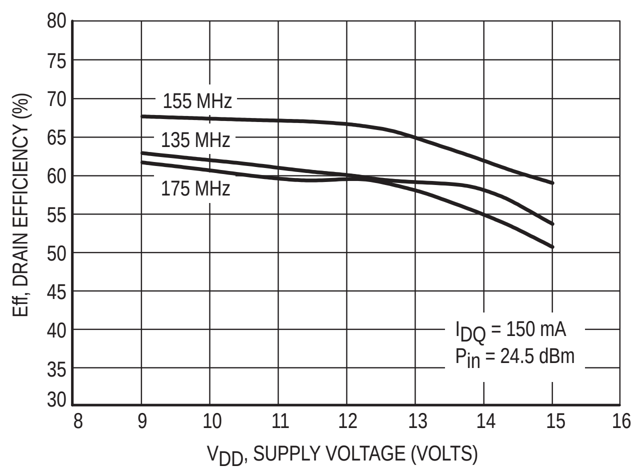
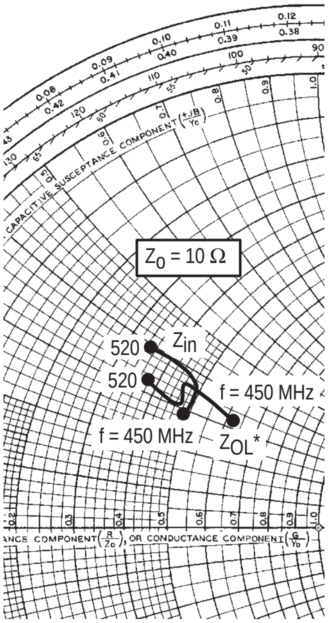
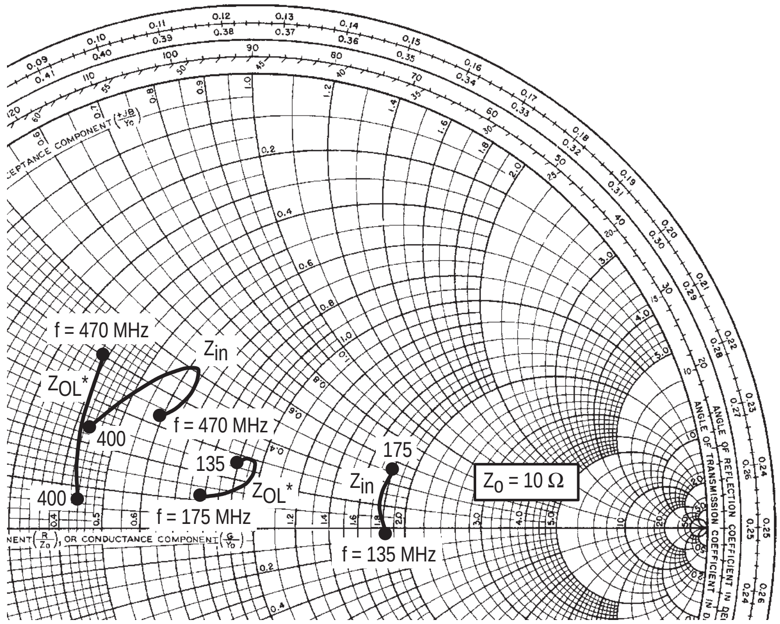


Figure 27. Drain Efficiency versus Supply Voltage





V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	4.9 +j2.85	6.42 +j3.23
470	4.85 +j3.71	4.59 +j3.61
500	4.63 +j3.84	4.72 +j3.12
520	3.52 +j3.92	3.81 +j3.27

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 82 pF capacitor in series with gate. (See Figure 1).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	4.28 +j2.36	4.41 +j0.67
440	6.45 +j5.13	4.14 +j2.53
470	5.91 +j3.34	3.92 +j4.02

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 47 pF capacitor in series with gate. (See Figure 10).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	18.31 –j0.76	8.97 +j2.62
155	17.72 +j1.85	9.69 +j2.81
175	18.06 +j5.23	7.94 +j1.14

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 43 pF capacitor in series with gate. (See Figure 19).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

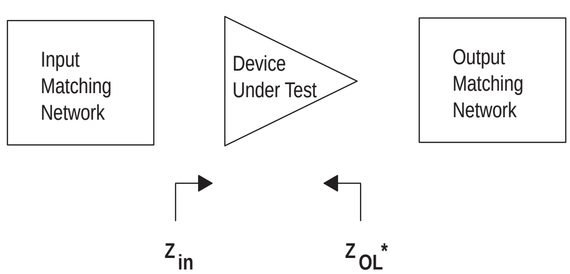


Figure 28. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 150 mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
50	0.88	–148	18.91	99	0.033	11	0.67	–144
100	0.85	–163	9.40	86	0.033	–6	0.66	–158
200	0.85	–170	4.47	73	0.026	–17	0.69	–162
300	0.87	–171	2.72	64	0.025	–28	0.74	–163
400	0.88	–172	1.85	56	0.021	–21	0.79	–164
500	0.90	–173	1.35	52	0.019	–30	0.83	–165
600	0.92	–173	1.04	47	0.014	–26	0.85	–167
700	0.93	–174	0.83	44	0.015	–39	0.88	–168
800	0.94	–175	0.68	39	0.014	–31	0.90	–169
900	0.94	–175	0.55	36	0.010	–41	0.91	–170
1000	0.96	–176	0.46	30	0.011	–38	0.95	–170

I_{DQ} = 800 mA

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
50	0.90	–159	20.80	97	0.020	14	0.73	–162
100	0.88	–169	10.35	88	0.018	1	0.74	–169
200	0.88	–174	5.09	79	0.017	–9	0.75	–171
300	0.89	–175	3.23	73	0.015	–18	0.77	–171
400	0.89	–175	2.30	67	0.015	–17	0.80	–171
500	0.90	–176	1.74	63	0.014	–22	0.82	–170
600	0.91	–176	1.39	59	0.014	–19	0.83	–171
700	0.92	–176	1.16	55	0.009	–23	0.85	–171
800	0.93	–176	0.96	50	0.011	–14	0.87	–172
900	0.94	–177	0.80	46	0.007	4	0.88	–173
1000	0.94	–177	0.67	41	0.010	–15	0.89	–173

I_{DQ} = 1.5 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
50	0.91	–159	20.18	97	0.015	11	0.73	–165
100	0.89	–169	10.05	89	0.016	–5	0.74	–171
200	0.88	–174	4.93	80	0.015	–3	0.75	–172
300	0.89	–175	3.14	73	0.014	–14	0.78	–172
400	0.89	–176	2.24	67	0.014	–20	0.80	–171
500	0.90	–176	1.70	64	0.014	–22	0.82	–170
600	0.92	–176	1.36	59	0.010	–16	0.84	–171
700	0.92	–176	1.13	55	0.013	–10	0.85	–171
800	0.93	–177	0.94	50	0.008	–13	0.87	–172
900	0.94	–177	0.78	46	0.013	–26	0.87	–173
1000	0.94	–178	0.65	41	0.007	8	0.87	–172

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

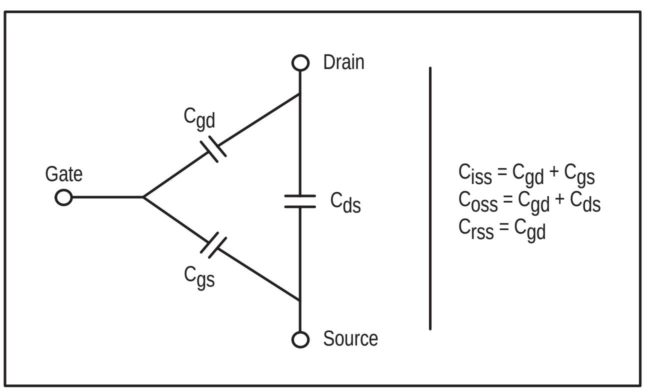
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, “Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package,” and Engineering Bulletin EB209/D, “Mounting Method for RF Power Leadless Surface Mount Transistor” for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with this device’s S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters” for a discussion of two port network theory and stability.

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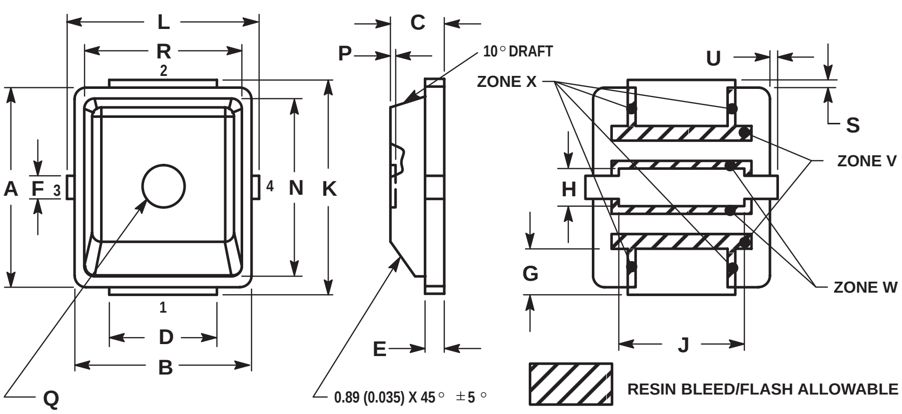
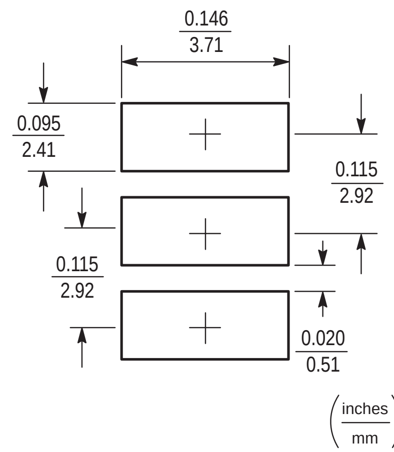
PACKAGE DIMENSIONS





SOLDER FOOTPRINT

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.255	0.265	6.48	6.73
B	0.225	0.235	5.72	5.97
C	0.065	0.072	1.65	1.83
D	0.130	0.150	3.30	3.81
E	0.021	0.026	0.53	0.66
F	0.026	0.044	0.66	1.12
G	0.050	0.070	1.27	1.78
H	0.045	0.063	1.14	1.60
J	0.160	0.180	4.06	4.57
K	0.273	0.285	6.93	7.24
L	0.245	0.255	6.22	6.48
N	0.230	0.240	5.84	6.10
P	0.000	0.008	0.00	0.20
Q	0.055	0.063	1.40	1.60
R	0.200	0.210	5.08	5.33
S	0.006	0.012	0.15	0.31
U	0.006	0.012	0.15	0.31
ZONE V	0.000	0.021	0.00	0.53
ZONE W	0.000	0.010	0.00	0.25
ZONE X	0.000	0.010	0.00	0.25

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. RESIN BLEED/FLASH ALLOWABLE IN ZONE V, W, AND X.

CASE 466–02
ISSUE B

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