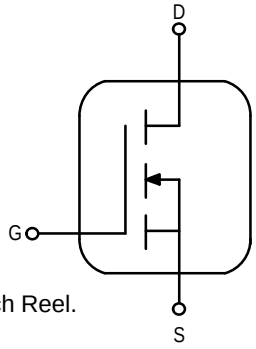
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFETs

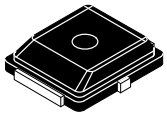
MRF1507
MRF1507T1

8 W, 520 MHz, 7.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

The MRF1507 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 volt portable FM equipment.

- Specified Performance @ 520 MHz, 7.5 Volts
  Output Power — 8 Watts
  Power Gain — 10 dB
  Efficiency — 65%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Excellent Thermal Stability
- Capable of Handling 20:1 VSWR, @ 9.5 Vdc, 520 MHz, 2 dB Overdrive
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- RF Power Plastic Surface Mount Package
- Available in Tape and Reel by Adding T1 Suffix to Part Number. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.





CASE 466–02, STYLE 1
(PLD 1.5)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage (1)	V_{DSS}	25	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	62.5 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_j	150	°C

THERMAL CHARACTERISTICS

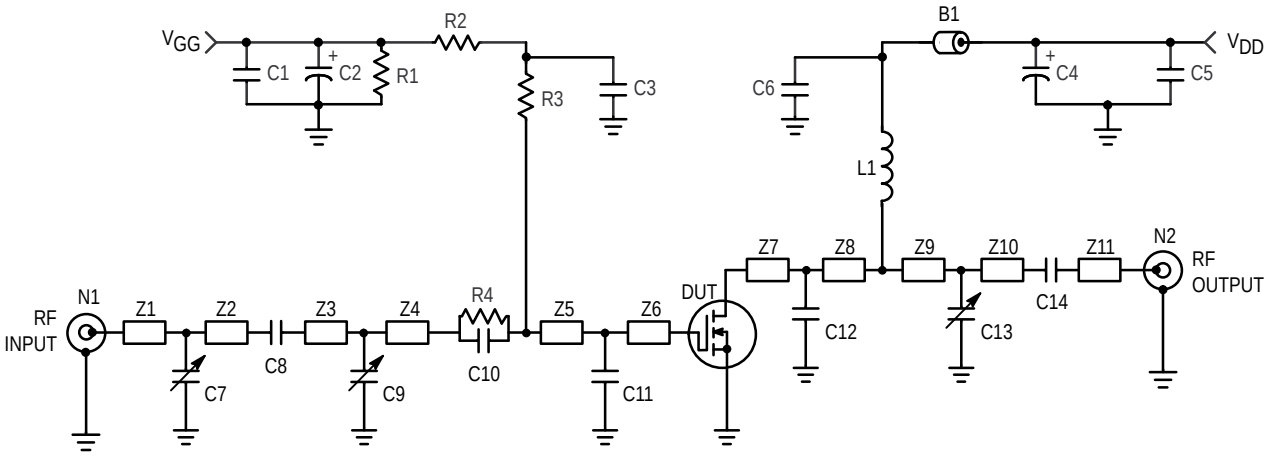
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

(1) Not designed for 12.5 volt applications.

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 25 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2.5	3.4	—	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	0.3	0.44	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	1.30	1.80	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	40.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 7.5 Vdc, P_{in} = 29 dBm, I_{DQ} = 150 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 7.5 Vdc, P_{in} = 29 dBm, I_{DQ} = 150 mA, f = 520 MHz)	η	50	65	—	%
P_{out} (V_{DD} = 7.5 Vdc, P_{in} = 29 dBm, I_{DQ} = 150 mA, f = 520 MHz)	P_{out}	8	9.9	—	W



B1	Fair Rite Products Long Ferrite Bead
C1, C5	0.1 μF, 100 mil Chip Capacitor
C2, C4	10 μF, 50 V Electrolytic Capacitor
C3, C6, C8, C14	130 pF, 100 mil Chip Capacitor
C7, C9, C13	0.3–20 pF Trimmer Capacitor
C10	82 pF, 100 mil Chip Capacitor
C11	39 pF, 100 mil Chip Capacitor
C12	32 pF, 100 mil Chip Capacitor
L1	4 Turns, #20 AWG Enamel, 0.1″ ID
N1, N2	Type N Connectors
R1	1.1 MΩ, 1/4 W Carbon
R2	2 kΩ, 1/2 W Carbon
R3	100 Ω, 1/4 W Carbon
R4	20 Ω, 1/4 W Carbon
Z1	0.459″ x 0.083″ Microstrip
Z2	0.135″ x 0.083″ Microstrip
Z3	1.104″ x 0.083″ Microstrip
Z4	0.114″ x 0.083″ Microstrip
Z5	0.154″ x 0.083″ Microstrip
Z6	0.259″ x 0.213″ Microstrip
Z7	0.217″ x 0.213″ Microstrip
Z8	0.175″ x 0.083″ Microstrip
Z9	0.747″ x 0.083″ Microstrip
Z10	0.608″ x 0.083″ Microstrip
Z11	0.594″ x 0.083″ Microstrip
Board	Glass Teflon, 31 mils

Figure 1. 500 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS

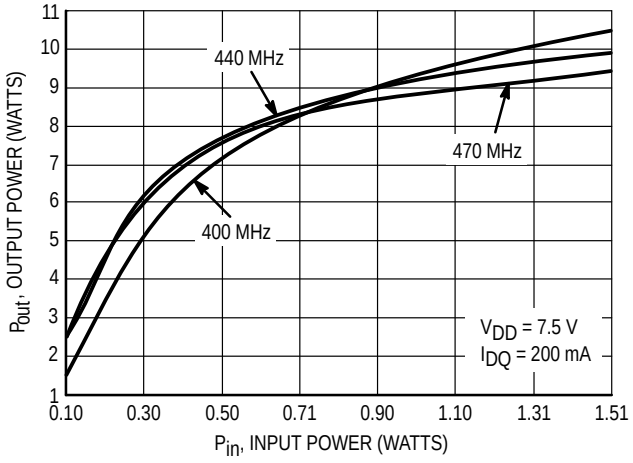


Figure 2. Output Power versus Input Power

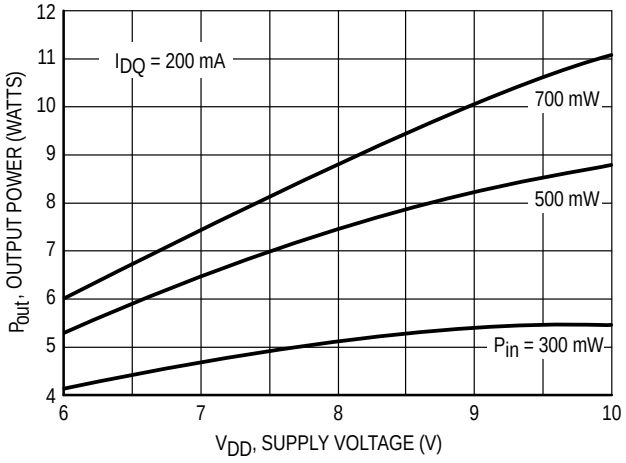


Figure 3. Output Power versus Supply Voltage @ 400 MHz

TYPICAL CHARACTERISTICS

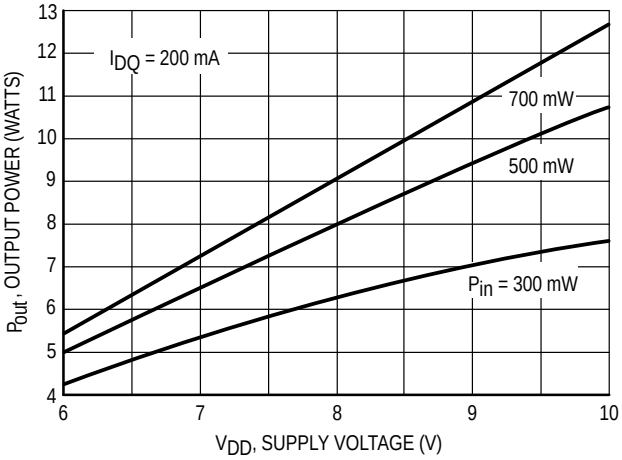


Figure 4. Output Power versus Supply Voltage @ 470 MHz

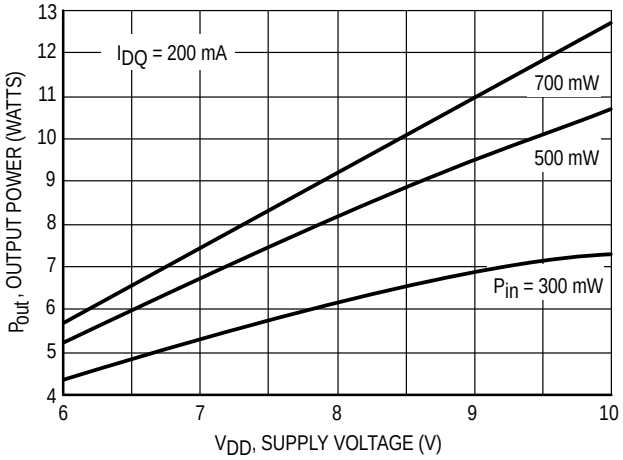


Figure 5. Output Power versus Supply Voltage @ 440 MHz

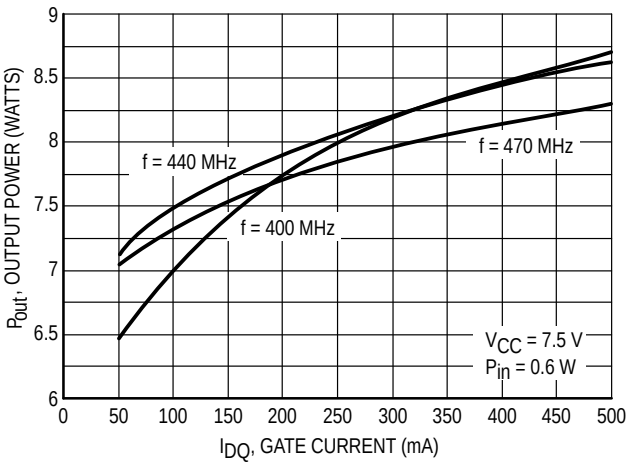


Figure 6. Output Power versus Gate Current

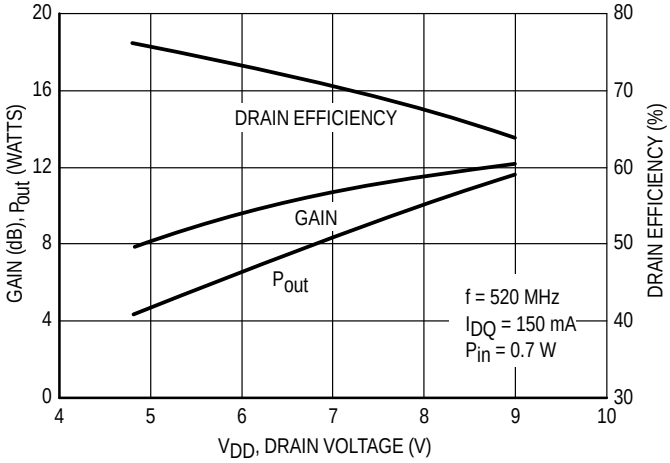


Figure 7. Gain, P_{out}, Efficiency versus Drain Voltage

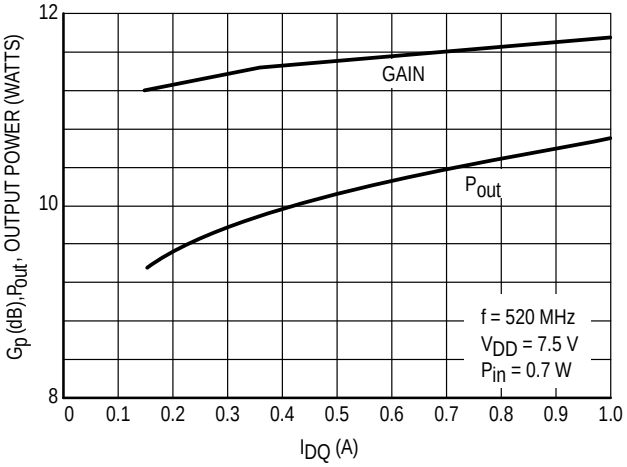


Figure 8. P_{out} versus I_{DQ}

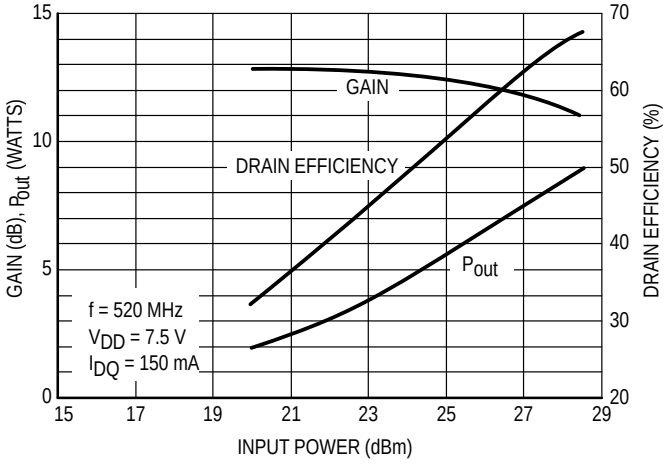


Figure 9. P_{out}, Gain, Drain Efficiency versus P_{in}

TYPICAL CHARACTERISTICS

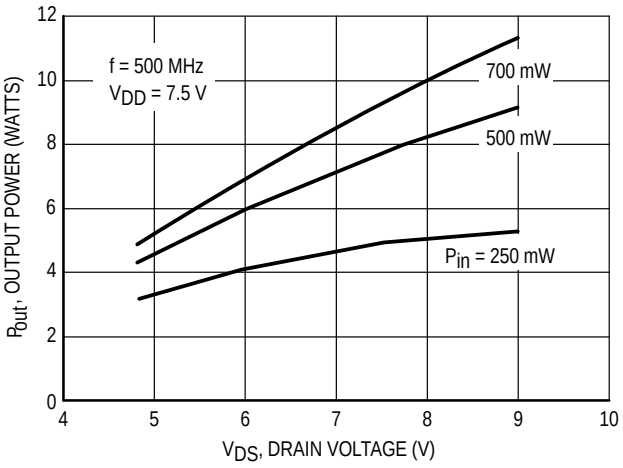


Figure 10. P_{out} versus Drain Voltage

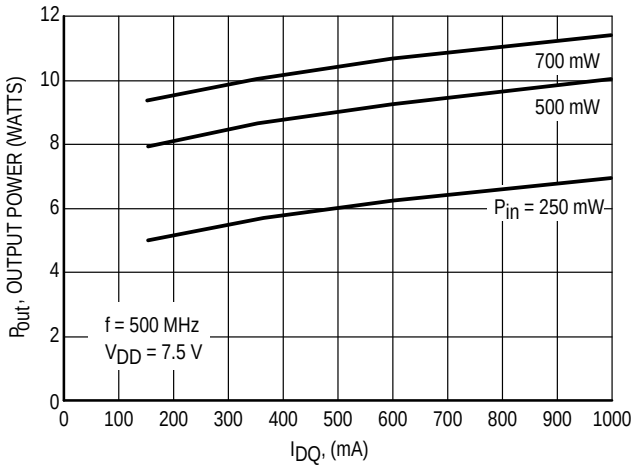


Figure 11. P_{out} versus I_{DQ}

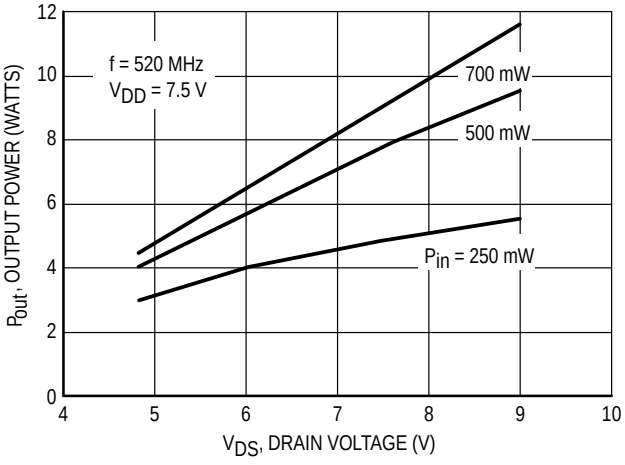


Figure 12. P_{out} versus Drain Voltage

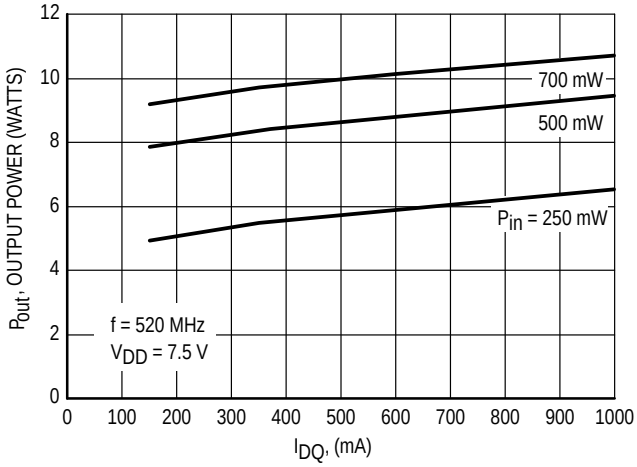


Figure 13. P_{out} versus I_{DQ}

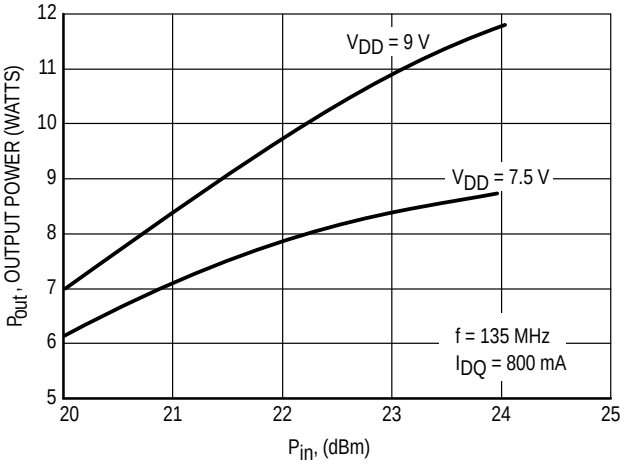


Figure 14. P_{out} versus P_{in}

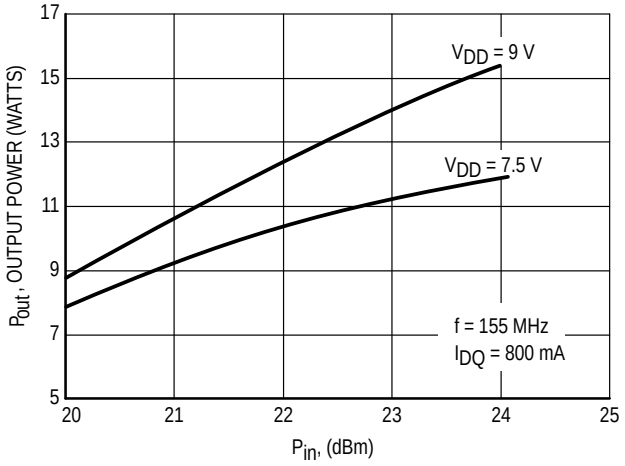


Figure 15. P_{out} versus P_{in}

TYPICAL CHARACTERISTICS

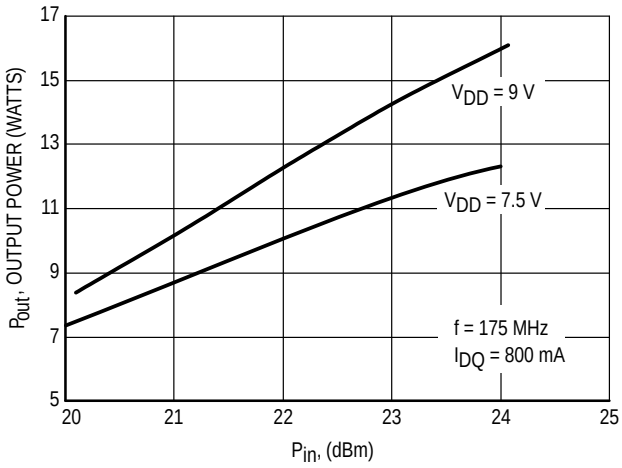


Figure 16. P_{out} versus P_{in}

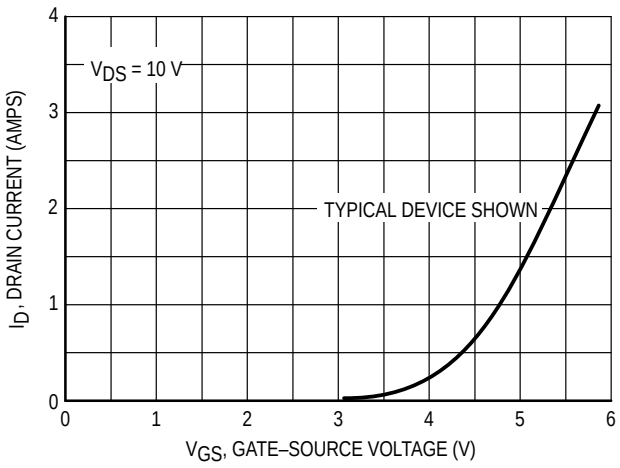


Figure 17. Drain Current versus Gate Voltage (Typical Device Shown)

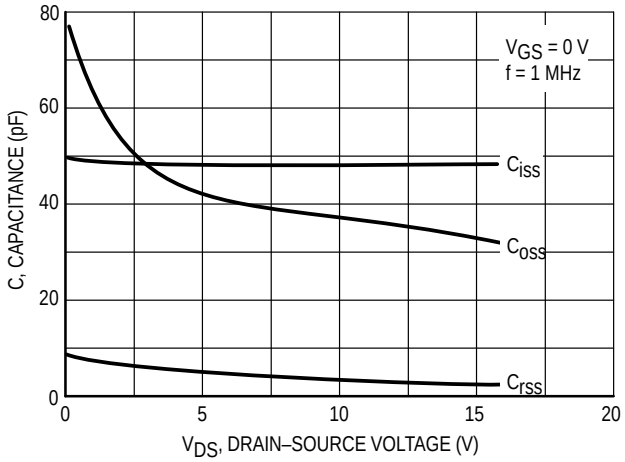


Figure 18. Capacitance versus Voltage

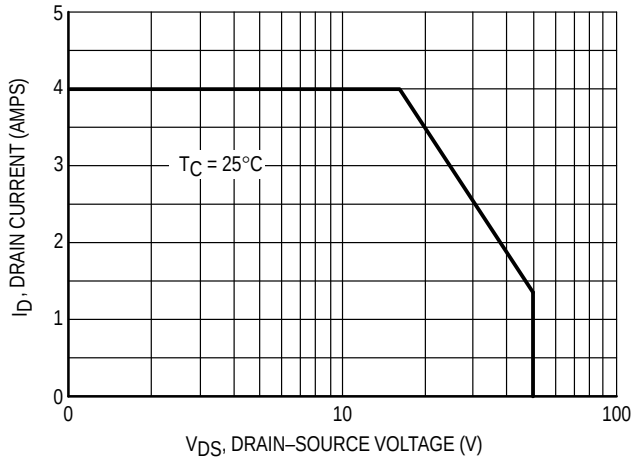
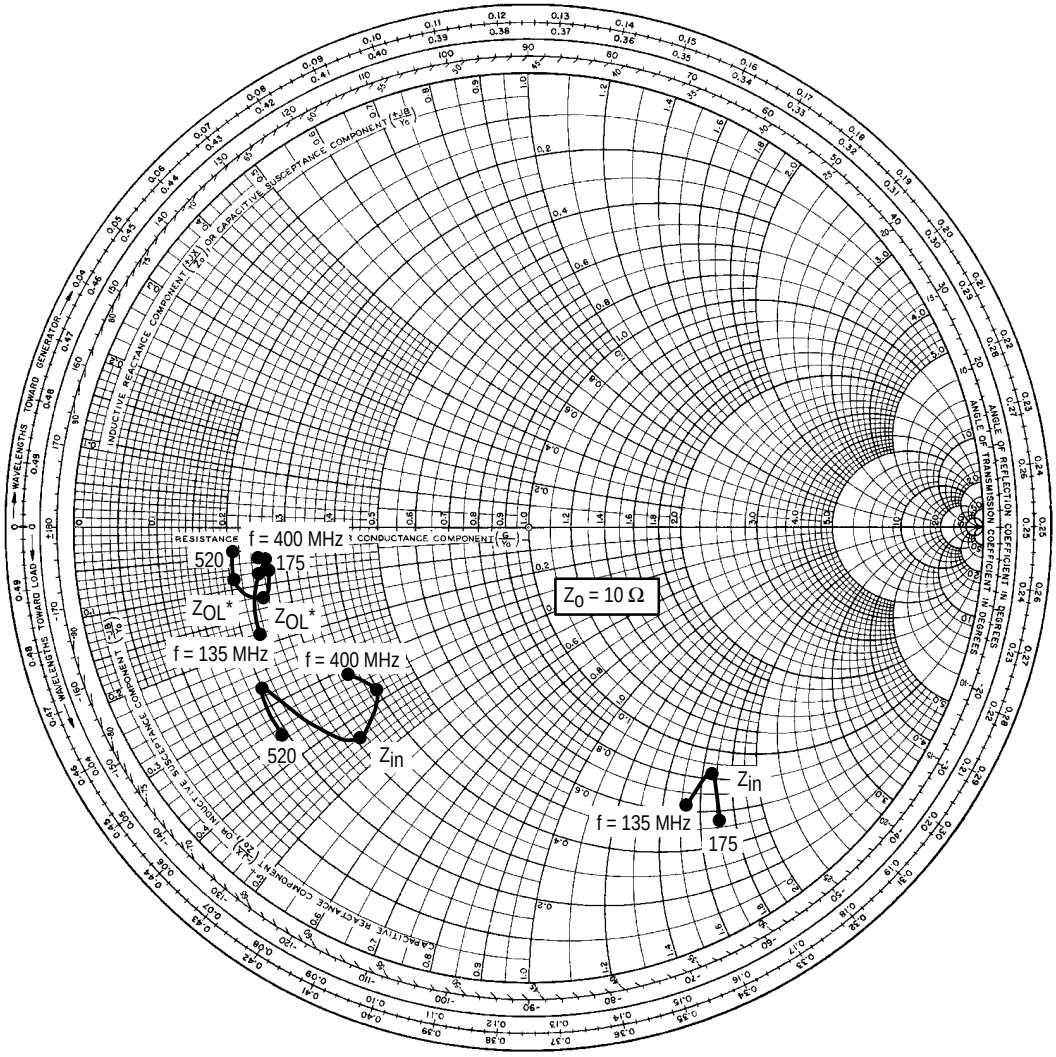


Figure 19. Maximum Rated Forward Biased Safe Operating Area



V_{DD} = 7.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	3.6 – j3.1	2.5 – j0.5
440	4.0 – j3.7	2.7 – j0.6
470	3.1 – j4.4	2.5 – j1.2
500	2.0 – j2.71	2.05 – j0.65
520	1.9 – j3.5	2.1 – j0.4

V_{DD} = 7.5 V, I_{DQ} = 800 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	6.2 – j15.1	2.3 – j1.8
155	8.29 – j16.9	2.5 – j0.8
175	5.33 – j17.0	2.6 – j0.6

Z_{in} = Conjugate of source impedance with parallel 20 Ω resistor and 82 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Z_{in} = Conjugate of source impedance with parallel 10 Ω resistor and 1000 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Table 1. Common Source Scattering Parameters (V_{DS} = 7.5 Vdc)

I_D = 150 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.76	–138	15.18	100	0.04	12	0.71	–141
100	0.77	–155	7.68	84	0.04	–3	0.72	–156
200	0.81	–162	3.53	65	0.03	–18	0.78	–162
300	0.85	–165	2.08	53	0.03	–27	0.83	–164
400	0.89	–167	1.37	44	0.03	–33	0.87	–166
500	0.91	–169	0.96	37	0.02	–36	0.90	–168
700	0.95	–171	0.54	27	0.01	–35	0.94	–170
850	0.96	–173	0.38	22	0.01	–30	0.95	–172
1000	0.97	–174	0.29	19	0.01	–19	0.96	–173
1200	0.98	–175	0.20	16	0.01	3	0.97	–174

I_D = 800 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.82	–152	16.58	98	0.03	9	0.79	–161
100	0.81	–165	8.37	88	0.03	1	0.80	–169
200	0.82	–170	4.08	76	0.02	–8	0.81	–172
300	0.84	–172	2.60	68	0.02	–13	0.83	–173
400	0.85	–172	1.84	61	0.02	–17	0.84	–173
500	0.87	–172	1.38	54	0.02	–20	0.86	–173
700	0.90	–173	0.86	44	0.02	–21	0.89	–174
850	0.91	–174	0.64	38	0.01	–19	0.90	–174
1000	0.92	–175	0.49	33	0.01	–12	0.92	–175
1200	0.94	–176	0.36	29	0.01	2	0.93	–176

I_D = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.83	–156	16.45	97	0.02	9	0.80	–164
100	0.83	–167	8.29	88	0.02	1	0.81	–171
200	0.83	–172	4.06	77	0.02	–6	0.82	–174
300	0.84	–173	2.61	70	0.02	–10	0.83	–174
400	0.86	–173	1.86	63	0.02	–13	0.85	–174
500	0.87	–174	1.41	57	0.02	–15	0.86	–174
700	0.89	–174	0.89	47	0.01	–16	0.88	–175
850	0.91	–175	0.67	41	0.01	–13	0.90	–175
1000	0.92	–175	0.52	36	0.01	–6	0.91	–175
1200	0.93	–176	0.38	31	0.01	8	0.92	–176

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MRF1507 is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of 10^9 Ω — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF1507 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF1507 was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF1507 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package.

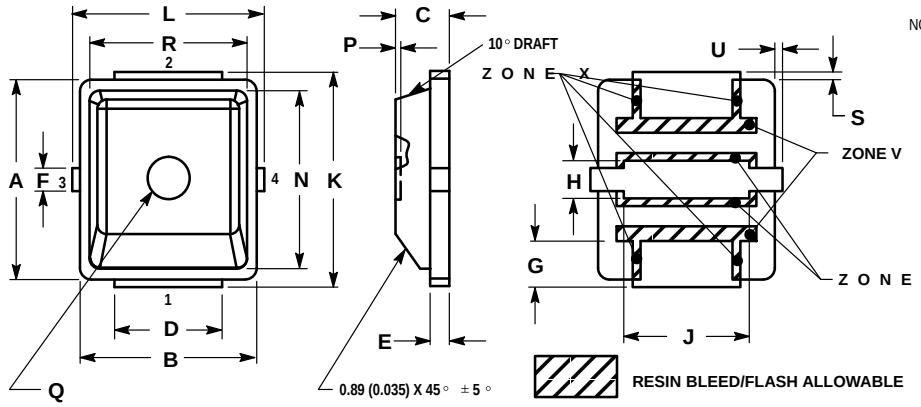
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF1507. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF1507 yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two–port stability analysis with the MRF1507 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters” for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. RESIN BLEED/FLASH ALLOWABLE IN ZONE V, W, AND X.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.255	0.265	6.48	6.73
B	0.225	0.235	5.72	5.97
C	0.065	0.072	1.65	1.83
D	0.130	0.150	3.30	3.81
E	0.021	0.026	0.53	0.66
F	0.026	0.044	0.66	1.12
G	0.050	0.070	1.27	1.78
H	0.045	0.063	1.14	1.60
J	0.160	0.180	4.06	4.57
K	0.273	0.285	6.93	7.24
L	0.245	0.255	6.22	6.48
N	0.230	0.240	5.84	6.10
P	0.000	0.008	0.00	0.20
Q	0.055	0.063	1.40	1.60
R	0.200	0.210	5.08	5.33
S	0.006	0.012	0.15	0.31
U	0.006	0.012	0.15	0.31
ZONE V	0.000	0.021	0.00	0.53
ZONE W	0.000	0.010	0.00	0.25
ZONE X	0.000	0.010	0.00	0.25

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

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