

### 2N5401HR

#### Hi-Rel PNP bipolar transistor 150 V - 0.5 A

#### **Features**

BV <sub>CEO</sub>	150 V
I <sub>C</sub> (max)	0.5 A
H <sub>FE</sub> at 10 V - 150 mA	> 60
Operating temperature range	-65°C to +200°C

- Hi-Rel PNP bipolar transistor
- Linear gain characteristics
- ESCC qualified
- European preferred part list EPPL
- Radiation level: lot specific total dose contact marketing for specified level



The 2N5401HR is a silicon planar epitaxial PNP transistor in TO-18 and LCC-3 packages. It is specifically designed for aerospace Hi-Rel applications and ESCC qualified according to the 5202-014 specification. In case of conflict between this datasheet and ESCC detailed specification, the latter prevails.

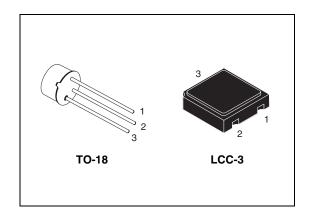


Figure 1. Internal schematic diagram

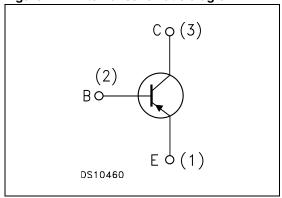


Table 1. Device summary

Order codes	Packages	Lead finish	Marking	Туре	EPPL	Packaging
2N5401HR	TO-18	Gold Solder Dip	520201401 520201402	ESCC Flight		Strip pack
2N5401T1	TO-18	Gold	2N5401T1	Engineering model		Strip pack
SOC5401	LCC-3	Gold	SOC5401	Engineering model		Waffle pack
SOC5401HRB	LCC-3	Gold Solder Dip	520201404 520201405	ESCC Flight	Yes	Waffle pack

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Electrical ratings 2N5401HR

# 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CBO</sub>	Collector-base voltage (I <sub>E</sub> = 0)	-160	V
V <sub>CEO</sub>	Collector-emitter voltage (I <sub>B</sub> = 0)	-150	V
V <sub>EBO</sub>	Emitter-base voltage (I <sub>C</sub> = 0)	-5	V
IC	Collector current for 2N5401HR for SOC5401HRB	-0.6 -0.5	A A
Р <sub>ТОТ</sub>	Total dissipation at $T_{amb} \le 25$ °C for 2N5401HR for SOC5401HRB for SOC5401HRB $^{(1)}$ Total dissipation at $T_c \le 25$ °C for 2N5401HR	0.36 0.36 0.58	W W W
T <sub>STG</sub>	Storage temperature	-65 to 200	°C
TJ	Max. operating junction temperature	200	°C

<sup>1.</sup> When mounted on a 8x10x0.6 mm ceramic substrate.

Table 3. Thermal data for through-hole package

Symbol	Parameter	Value	Unit
R <sub>thJC</sub>	Thermal resistance junction-case max	146	°C/W
$R_{thJA}$	Thermal resistance junction-ambient max	486	°C/W

Table 4. Thermal data for SMD package

Symbol	Parameter	Value	Unit
R <sub>thJA</sub>	Thermal resistance junction-ambient max Thermal resistance junction-ambient (1) max	486 302	°C/W
	Thermal resistance junision ambient	002	0,

<sup>1.</sup> When mounted on a 8x10x0.6 mm ceramic substrate.

## 2 Electrical characteristics

 $T_{case}$  = 25 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>CBO</sub>	Collector-base cut-off current (I <sub>E</sub> = 0)	V <sub>CB</sub> = -120 V V <sub>CB</sub> = -120 V T <sub>C</sub> = 150 °C			-50 -50	nA μA
I <sub>EBO</sub>	Emitter-base cut-off current (I <sub>C</sub> = 0)	V <sub>EB</sub> = -3 V			-50	nA
V <sub>(BR)CBO</sub>	Collector-base breakdown voltage (I <sub>E</sub> = 0)	I <sub>C</sub> = -100 μA	-160			V
V <sub>(BR)CEO</sub> (1)	Collector-emitter breakdown voltage (I <sub>B</sub> = 0)	I <sub>C</sub> = -1 mA	-150			V
V <sub>(BR)EBO</sub>	Emitter-base breakdown voltage (I <sub>C</sub> = 0)	I <sub>E</sub> = -10 μA	-5			V
V <sub>CE(sat)</sub> (1)	Collector-emitter saturation voltage	$I_C = -10 \text{ mA}$ $I_B = -1 \text{ mA}$ $I_C = -50 \text{ mA}$ $I_B = -5 \text{ mA}$			-0.2 -0.5	V V
V <sub>BE(sat)</sub> (1)	Base-emitter saturation voltage	$I_C = -10 \text{ mA}$ $I_B = -1 \text{ mA}$ $I_C = -50 \text{ mA}$ $I_B = -5 \text{ mA}$			-1 -1	V V
h <sub>FE</sub> <sup>(1)</sup>	DC current gain	$\begin{split} & I_{C} = -1 \text{ mA} & V_{CE} = -5 \text{ V} \\ & I_{C} = -10 \text{ mA} & V_{CE} = -5 \text{ V} \\ & I_{C} = -50 \text{ mA} & V_{CE} = -5 \text{ V} \\ & I_{C} = -10 \text{ mA} & V_{CE} = -5 \text{ V} \\ & T_{amb} = -55 \text{ °C} \end{split}$	50 60 60 20		240	
h <sub>fe</sub>	Small signal current gain	$V_{CE} = -10 \text{ V}$ $I_{C} = -10 \text{ mA}$ $f = 10 \text{ kHz}$	5			
C <sub>obo</sub>	Output capacitance (I <sub>E</sub> = 0)	V <sub>CB</sub> = -10 V			6	pF

<sup>1.</sup> Pulsed duration = 300  $\mu$ s, duty cycle  $\leq$  2 %

## 3 Package mechanical data

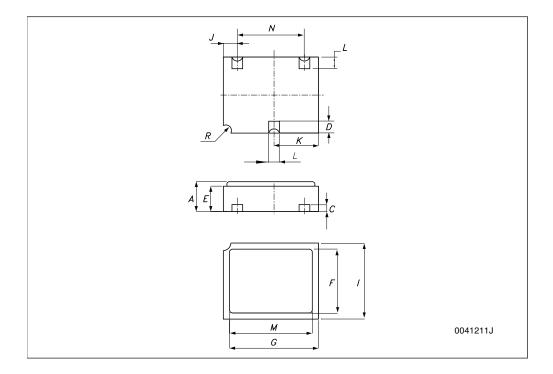
In order to meet environmental requirements, ST offers these devices in different grades of  $\mathsf{ECOPACK}^{\mathbb{B}}$  packages, depending on their level of environmental compliance.  $\mathsf{ECOPACK}^{\mathbb{B}}$  specifications, grade definitions and product status are available at:  $\mathit{www.st.com}$ .  $\mathsf{ECOPACK}^{\mathbb{B}}$  is an ST trademark.

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#### Ceramic Leadless Chip Carrier 3 mechanical data

DIM.		mm.	
DIW.	MIN.	TYP	MAX.
Α	1.16		1.42
С	0.45	0.50	0.56
D		0.76	
E		1	
F	1.90		2.15
G	2.90		3.25
I	2.40		2.74
J	0.40	0.57	0.80
К	1.35	1.52	1.75
L		0.50	
М	2.40		2.65
N		1.90	
R		0.30	

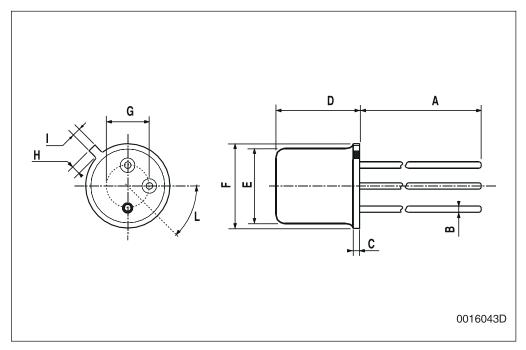


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10-	18	Mec	han	ıcal	data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А		12.7			0.500	
В			0.49			0.019
D			5.3			0.208
E			4.9			0.193
F			5.8			0.228
G	2.54			0.100		
Н			1.2			0.047
I			1.16			0.045
L	45°			45°		





2N5401HR Revision history

# 4 Revision history

Table 6. Document revision history

Date	Revision	Changes
04-Jan-2010	1	Initial release

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