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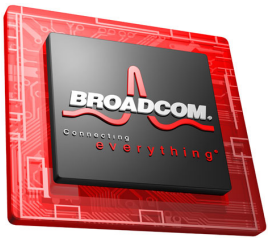
BCM8125
PRODUCT Brief



10 GBPS 1:16 DEMUX WITH CDR AND LIMITING AMPLIFIER

FEATURES

- **Supports 10-Gigabit MSA (Multi-Source Agreement) features**
- **Fully integrated CDR and demultiplexer**
- **Support for multiple rates—OC-192: 9.953 Gbps, OC-192 FEC: 10.664 and 10.709 Gbps, 10G Ethernet: 10.3125 Gbps**
- **1:16 demultiplexer with LVDS parallel data and clock outputs**
- **Lock detect**
- **Loss of signal detect**
- **Integrated limiting amplifier:**
  - Minimum input sensitivity 10 mV single ended
- **Exceeds SONET jitter requirements**
- **Core power supply: 1.8V**
- **I/O power supply: CML, LVDS, LVPECL at 1.8V, CMOS at 1.8V or 3.3V**
- **Power consumption: 900 mW typical @ 1.8V**
- **Standard CMOS fabrication process**
- **11 x 11 mm, 127-pin BGA package**

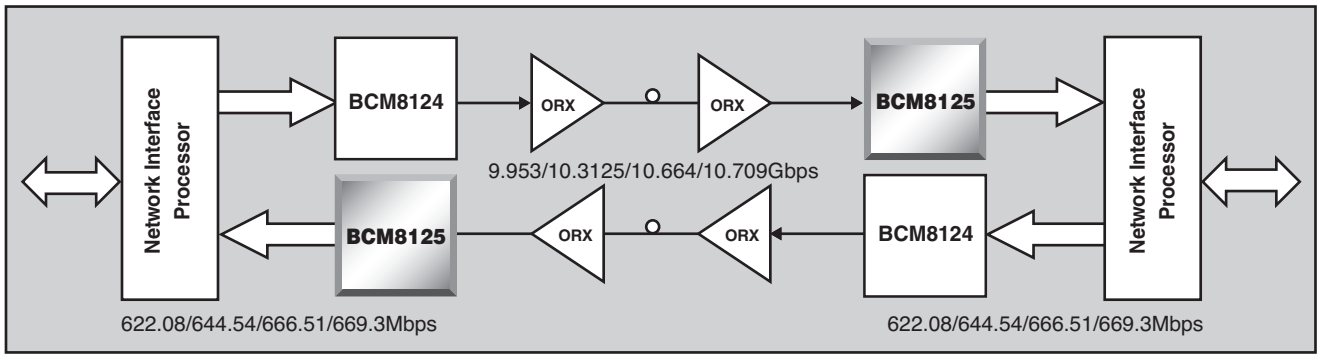
SUMMARY OF BENEFITS

- **Compliant with industry standards such as Optical Internetworking Forum (OIF), Telcordia, ITU-T, and IEEE 802.3ae standards.**
- **Reduces design cycle and time to market.**
- **High level of integration allows for higher port density solutions.**
- **Uses the most effective silicon economy of scale for CMOS-based devices.**
- **Low power consumption eliminates the need for external cooling sources.**

APPLICATIONS

- **OC-192/STM-64/10GE transmission equipment**
- **SONET/SDH optical modules**
- **ADD/DROP multiplexers**
- **Digital cross-connects**
- **ATM switch backbones**
- **SONET test equipment**
- **Terabit routers**
- **Edge routers**

BCM8125 Application Diagram



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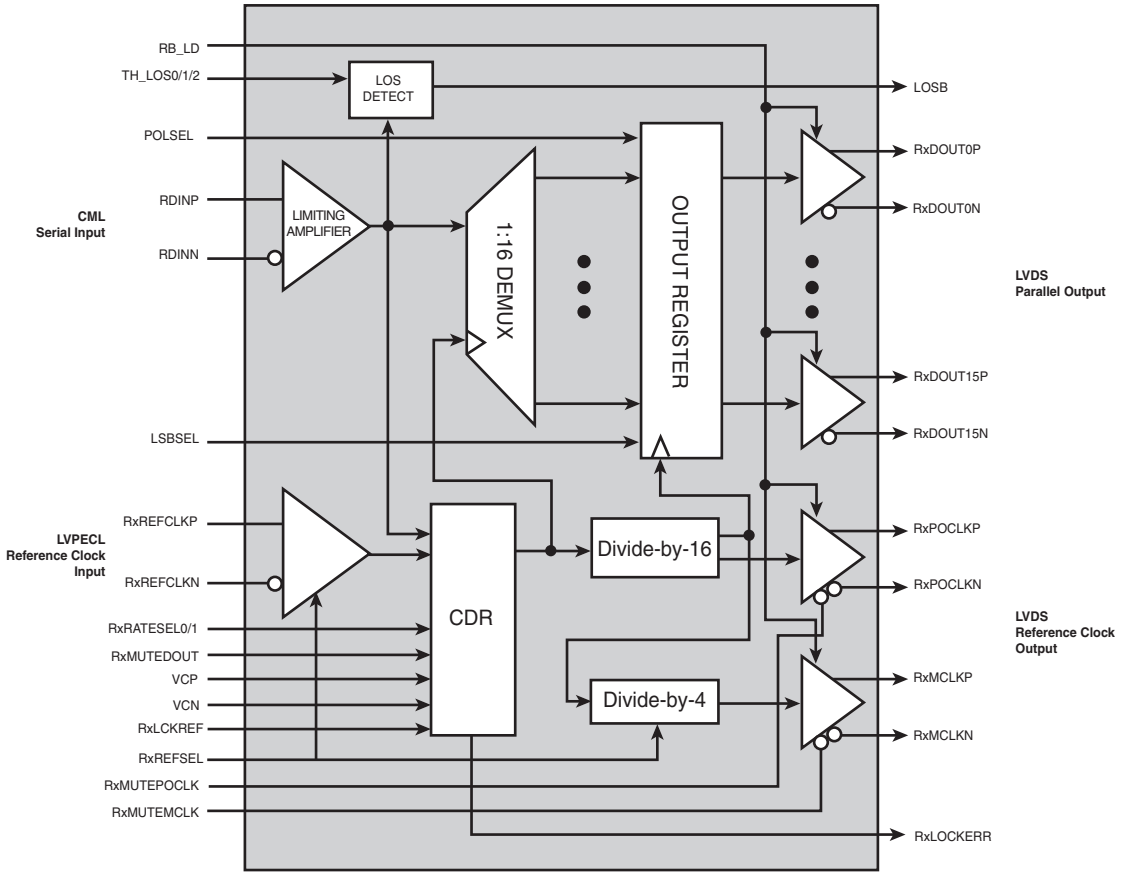
OVERVIEW



The **BCM8125** is a fully integrated MSA-compatible quad-rate SONET/SDH/10GE receiver operating at OC-192/STM-64, 10GE, and two different FEC (Forward Error Correction) data rates (9.953, 10.3125, 10.664, and 10.709 Gbps) with deserializer, clock and data recovery (CDR), and loss-of-signal (LOS) detection circuitry. The **BCM8125** provides high-jitter tolerance and low-jitter generation to comply with Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T standards.

The **BCM8125** reference clock input frequency is user-selectable to the line rate divided by either 16 or 64. The reference clock output and the LVDS receive parallel bus output can be squelched under user control. An integrated limiting amplifier provides the **BCM8125** with input sensitivity down to 10 mV single ended, saving the customer cost and power.

The **BCM8125** can be powered with a single 1.8V supply or dual 1.8/3.3V supply without any special power supply sequencing requirements.

The **BCM8125** comes in an 11 x 11 mm, 127-pin BGA package.

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