

MC74VHC157

Quad 2-Channel Multiplexer

The MC74VHC157 is an advanced high-speed CMOS quad 2-channel multiplexer, fabricated with silicon gate CMOS technology. It achieves high-speed operation similar to equivalent Bipolar-Schottky TTL, while maintaining CMOS low-power dissipation.

It consists of four 2-input digital multiplexers with common select (S) and enable (\bar{E}) inputs. When \bar{E} is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 4.1 \text{ ns}$ (Typ) at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V}$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 82 FETs
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at www.onsemi.com for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

www.DataSheet4U.com

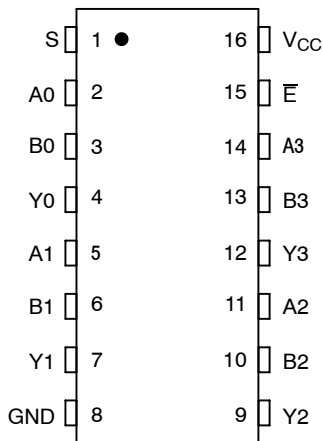


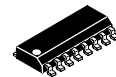
Figure 1. Pin Assignment



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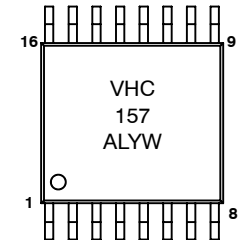
MARKING DIAGRAMS



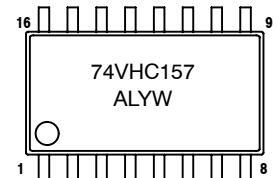
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOIC EIAJ-16
M SUFFIX
CASE 966



- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHC157D	SOIC-16	48 Units/Rail
MC74VHC157DR2	SOIC-16	2500 Units/Reel
MC74VHC157DT	TSSOP-16	96 Units/Rail
MC74VHC157DTR2	TSSOP-16	2500 Units/Reel
MC74VHC157M	SOIC EIAJ-16	50 Units/Rail
MC74VHC157MEL	SOIC EIAJ-16	2000 Units/Reel

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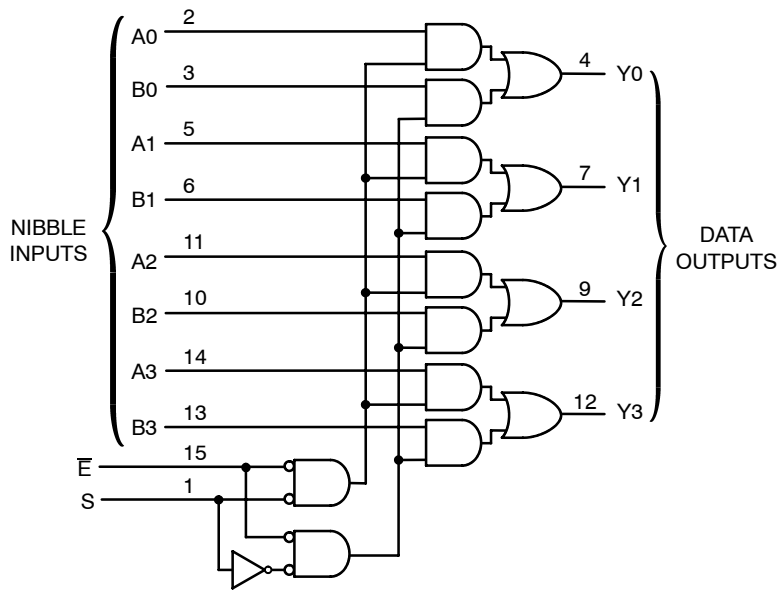


Figure 2. Expanded Logic Diagram

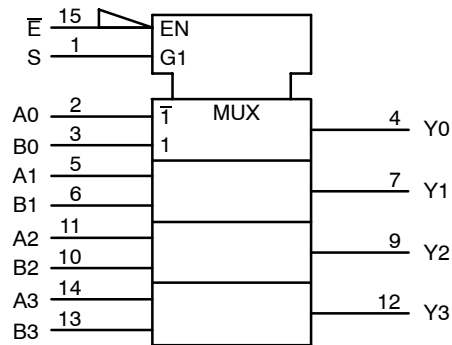


Figure 3. IEC Logic Symbol

FUNCTION TABLE

Inputs		Outputs
\bar{E}	S	Y0 - Y3
H	X	L
L	L	A0-A3
L	H	B0-B3

A0 - A3, B0 - B3 = the levels of the respective Data-Word Inputs.

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	-20	mA
I _{OK}	DC Output Diode Current V _O < GND	±20	mA
I _O	DC Output Sink Current	±25	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+150	°C
θ _{JA}	Thermal Resistance	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% - 35%	UL-94-VO (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 85°C (Note 5)	±500	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage (Note 6)	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	-55	125	°C
t _r , t _f	Input Rise or Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0	100 20	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

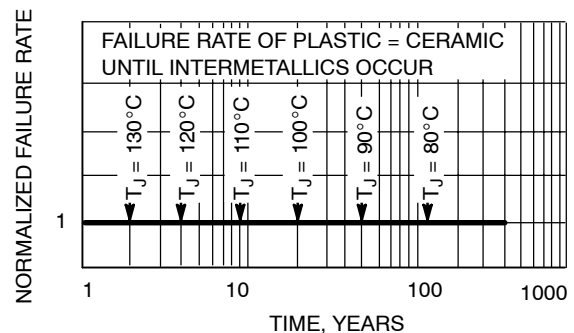


Figure 4. Failure Rate vs. Time Junction Temperature

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0 3.0 to 5.5	1.5 0.7 V _{CC}			1.5 0.7 V _{CC}		1.5 0.7 V _{CC}		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 to 5.5			0.5 0.3 V _{CC}		0.5 0.3 V _{CC}		0.5 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA	3.0 4.5	2.58 3.94			2.48 3.8		2.34 3.66		
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA I _{OH} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			4.0		40.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Characteristic	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Typ	Max	Typ	Max	
t _{PLH} , t _{PHL}	Propagation Delay, A to B to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		6.2 8.7	9.7 13.2	1.0 1.0	11.5 15.0	1.0 1.0	11.5 15.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		4.1 5.6	6.4 8.4	1.0 1.0	7.5 9.5	1.0 1.0	7.5 9.5	
t _{PLH} , t _{PHL}	Propagation Delay, S to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		8.4 10.9	13.2 16.7	1.0 1.0	15.5 19.0	1.0 1.0	15.5 19.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.3 6.8	8.1 10.1	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	
t _{PLH} , t _{PHL}	Propagation Delay, E to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		8.7 11.2	13.6 17.1	1.0 1.0	16.0 19.5	1.0 1.0	16.0 19.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
C _{IN}	Input Capacitance			4	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		20		

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns; $C_L = 50$ pF; $V_{CC} = 5.0$ V)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.3	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

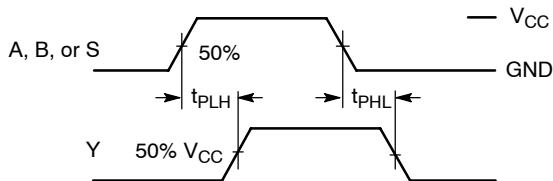


Figure 5. Switching Waveform

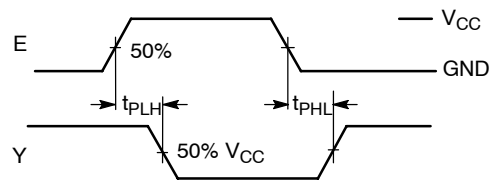
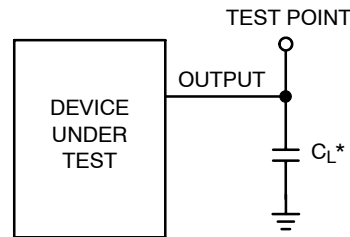


Figure 6. Inverting Switching



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

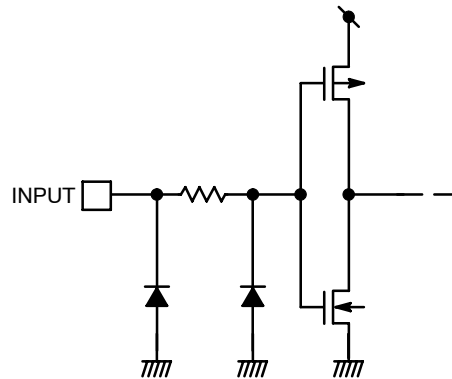
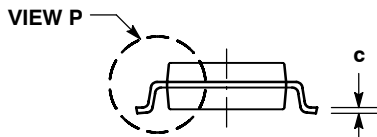
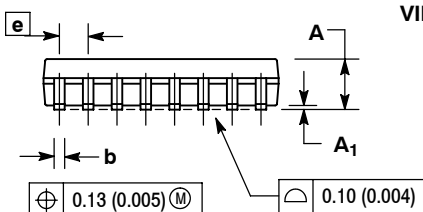
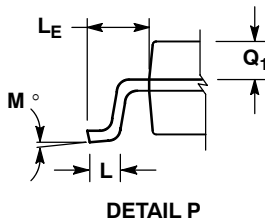
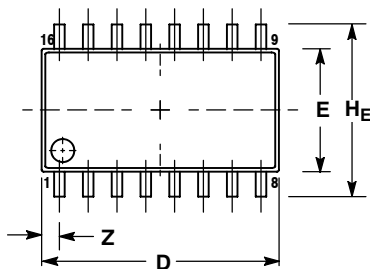


Figure 8. Input Equivalent Circuit

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PACKAGE DIMENSIONS

SOIC EIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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