MC74LCX541

Low-Voltage CMOS Octal Buffer Flow Through Pinout

With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The MC74LCX541 is a high performance, non−inverting octal buffer operating from a 2.3 to 3.6 V supply. This device is similar in function to the MC74LCX244, while providing flow through architecture. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX541 inputs to be safely driven from 5 V devices. The MC74LCX541 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OE1}$. $\overline{OE2}$) inputs, when HIGH, disables the output by placing them in a HIGH Z condition.
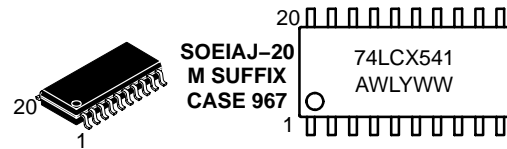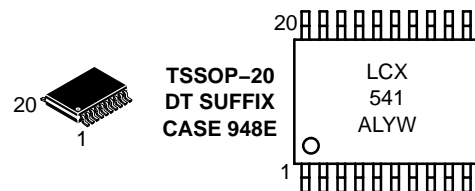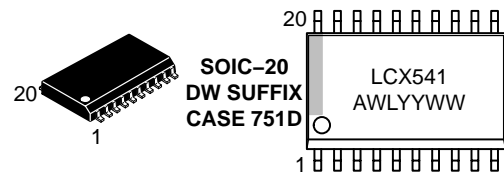
Features

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant − Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V
                        Machine Model >200 V
- Pb−Free Packages are Available*

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MARKING DIAGRAMS

SOIC−20
DW SUFFIX
CASE 751D

LCX541
AWLYYWW

TSSOP−20
DT SUFFIX
CASE 948E

LCX
541
ALYW

SOEIAJ−20
M SUFFIX
CASE 967

74LCX541
AWLYWW

A   = Assembly Location
L, WL   = Wafer Lot
Y, YY   = Year
W, WW   = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
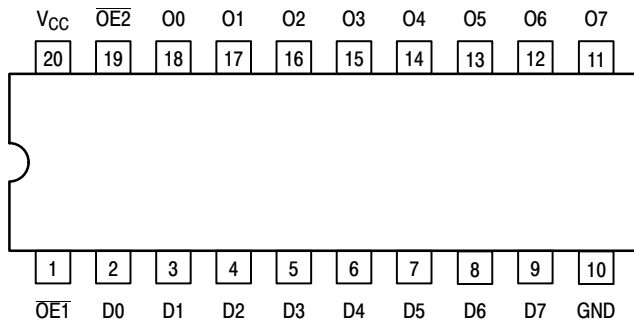
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Figure 1. Pinout: 20–Lead (Top View)

PIN NAMES

Pins	Function
$\overline{OEn}$	Output Enable Inputs
Dn	Data Inputs
On	3–State Outputs
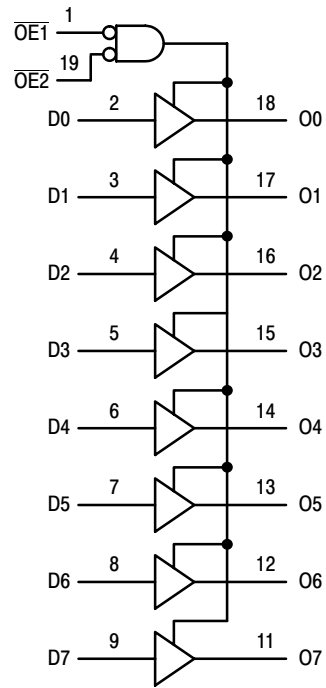
Figure 2. LOGIC DIAGRAM

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	Dn	On
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance
State; X = High or Low Voltage Level and Transitions are Acceptable, for
I_{CC} reasons, DO NOT FLOAT Inputs

MC74LCX541

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3−State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1	V
I_{IK}	DC Input Diode Current	−50	$V_I <$ GND	mA
I_{OK}	DC Output Diode Current	−50	$V_O <$ GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0		V_{CC}	V
		(3−State)	0		5.5	
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0 V − 3.6 V				−24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0 V − 3.6 V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7 V − 3.0 V				−12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7 V − 3.0 V				12	mA
T_A	Operating Free−Air Temperature		−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V		0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74LCX541DW	SOIC−20	38 Units / Rail
MC74LCX541DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC74LCX541DWR2	SOIC−20	1000 Tape & Reel
MC74LCX541DR2G	SOIC−20 (Pb−Free)	1000 Tape & Reel
MC74LCX541DT	TSSOP−20*	75 Units / Rail
MC74LCX541DTR2	TSSOP−20*	2000 Tape & Reel
MC74LCX541MEL	SOEIAJ−20	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2)	2.7 V ≤ V_{CC} ≤ 3.6 V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2)	2.7 V ≤ V_{CC} ≤ 3.6 V		0.8	V
V_{OH}	HIGH Level Output Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = −100 µA	V_{CC} − 0.2		V
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.2		
V_{OL}	LOW Level Output Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 µA		0.2	V
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	2.7 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_I ≤ 5.5 V		±5.0	µA
I_{OZ}	3−State Output Current	2.7 ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_O ≤ 5.5 V; V_I = V_{IH} or V_{IL}		±5.0	µA
I_{OFF}	Power−Off Leakage Current	V_{CC} = 0 V; V_I or V_O = 5.5 V		10	µA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		10	µA
		2.7 ≤ V_{CC} ≤ 3.6 V; 3.6 ≤ V_I or V_O ≤ 5.5 V		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} − 0.6 V		500	µA

2. These values of V_I are used to test DC electrical characteristics only.

AC ELECTRICAL CHARACTERISTICS (t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω)

Symbol	Parameter	Waveform	V_{CC} = 3.0 V to 3.6 V Min	V_{CC} = 3.0 V to 3.6 V Max	V_{CC} = 2.7 V Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	6.5 6.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	8.5 8.5	ns
t_{OSHL} t_{OSLH}	Output−to−Output Skew (Note 3)			1.0 1.0		ns

(Limits / T_A = −40°C to +85°C)

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	Unit
V_{OLP}	Dynamic LOW Peak Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V

4. Number of outputs defined as "n". Measured with "n−1" outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.
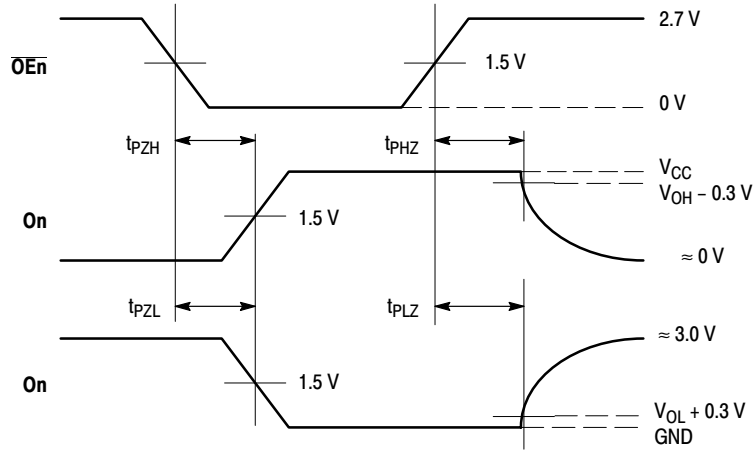
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF

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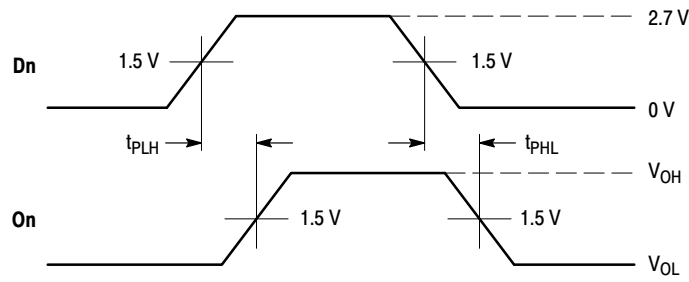
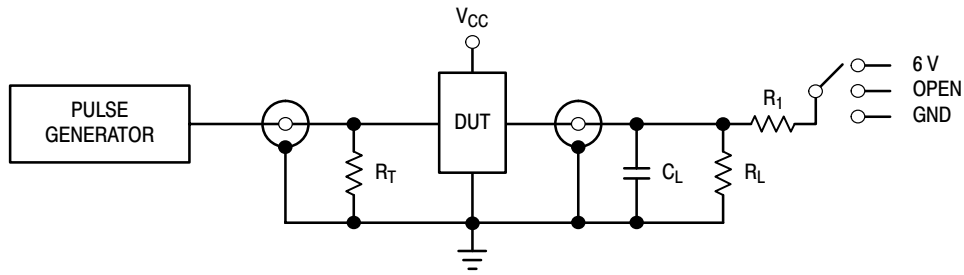**WAVEFORM 1 – PROPAGATION DELAYS**
$t_R = t_F = 2.5$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

Figure 3. AC Waveforms

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH}, t_{PHZ}	GND

$C_L = 50$ pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1 = 500\ \Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

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PACKAGE DIMENSIONS

SOIC–20
DW SUFFIX
CASE 751D–05
ISSUE G
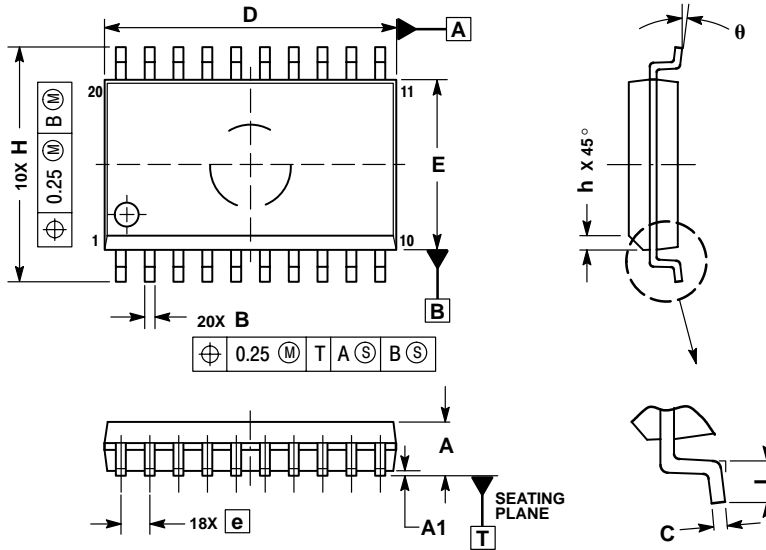
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

TSSOP–20
DT SUFFIX
CASE 948E–02
ISSUE B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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PACKAGE DIMENSIONS

SOEIAJ–20
M SUFFIX
CASE 967–01
ISSUE O
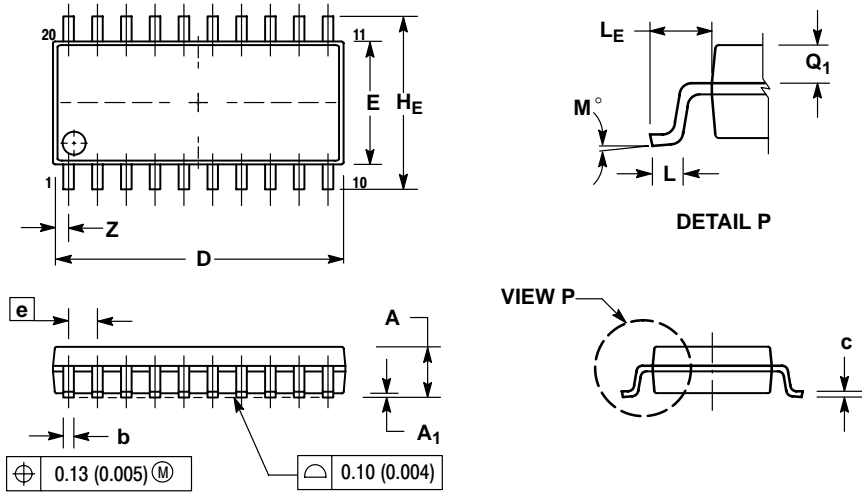
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DETAIL P

VIEW P

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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MC74LCX541/D