

# BCD-to-Seven-Segment Latch/ Decoder/Display Driver

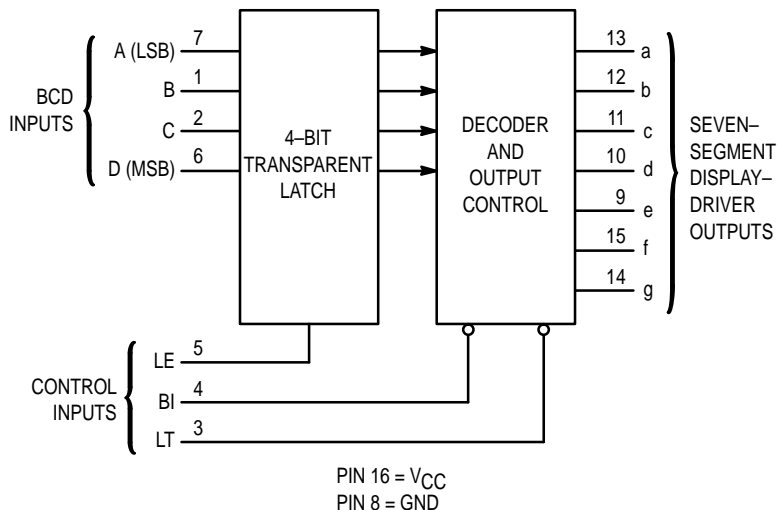
## High-Performance Silicon-Gate CMOS

The MC74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

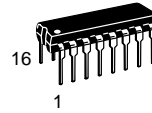
The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates

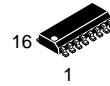
### LOGIC DIAGRAM



# MC74HC4511



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

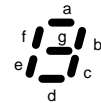
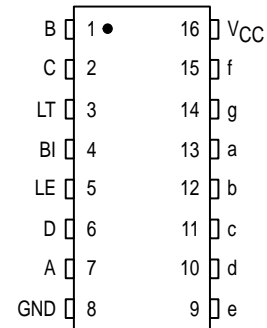


**D SUFFIX**  
SOIC PACKAGE  
CASE 751B-05

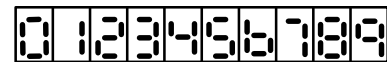
### ORDERING INFORMATION

MC74HCXXXXN Plastic  
MC74HCXXXXD SOIC

### PIN ASSIGNMENT



DISPLAY



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 70	mA
P <sub>D</sub>	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 3)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit				
				- 55 to 25°C	≤ 85°C	≤ 125°C					
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V				
			4.5	0.9	0.9	0.9					
			6.0	1.2	1.2	1.2					
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V				
			4.5	0.1	0.1	0.1					
			6.0	0.1	0.1	0.1					
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA				
			I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0		8	80	160	μA
						6.0		8	80	160	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0	600	750	900	ns
		4.5	120	150	180	
		6.0	102	129	153	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, VCC = 5.0 V		pF
		70		

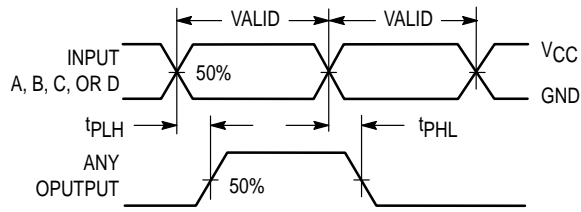
\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** (Input  $t_r = t_f = 6$  ns)

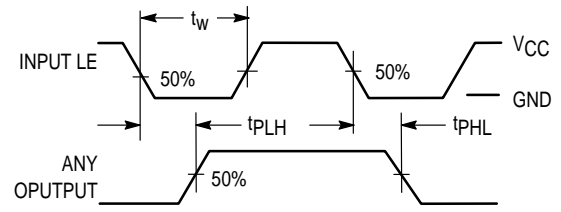
Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>su</sub>	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>h</sub>	Minimum Hold Time, Latch Enable to Input A, B, C, or D (Figure 5)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t <sub>w</sub>	Minimum Pulse Width, Latch Enable (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

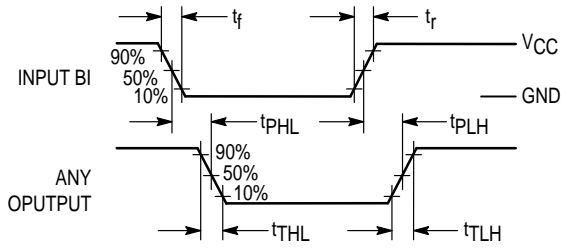
**SWITCHING WAVEFORMS**



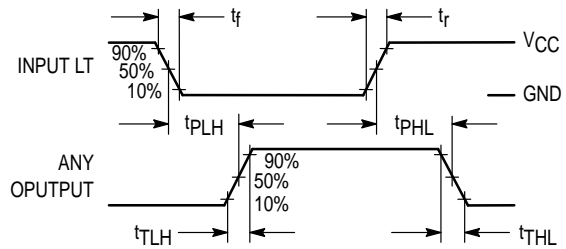
**Figure 1.**



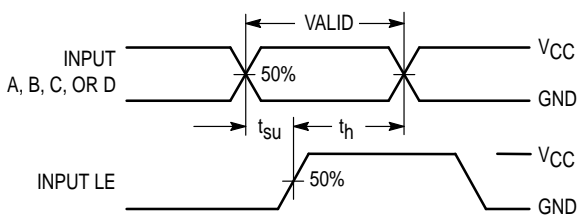
**Figure 2.**



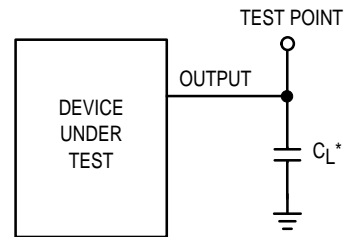
**Figure 3.**



**Figure 4.**



**Figure 5.**



\* Includes all probe and jig capacitance

**Figure 6. Test Circuit**

FUNCTION TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	L	L	H	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	*							*

\* = Depends upon the BCD code previously applied while LE was at a low level.

## PIN DESCRIPTIONS

### INPUTS

#### A, B, C, D (Pins 7, 1, 2, 6)

BCD inputs. A (pin 7) is the least significant bit and D (pin 6) is the most significant bit. Hexadecimal code A–F at these inputs causes the outputs to assume a low level, offering an alternate method of blanking the display.

### OUTPUTS

#### a, b, c, d, e, f, g (Pins 13, 12, 11, 10, 9, 15, 14)

Decoded, buffered seven–segment display–driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

### CONTROL INPUTS

#### BI (Pin 4)

Active–low display blanking input. A low level on this input will cause all outputs to be held low, thereby blanking the display. LT is the only input that overrides the BI input.

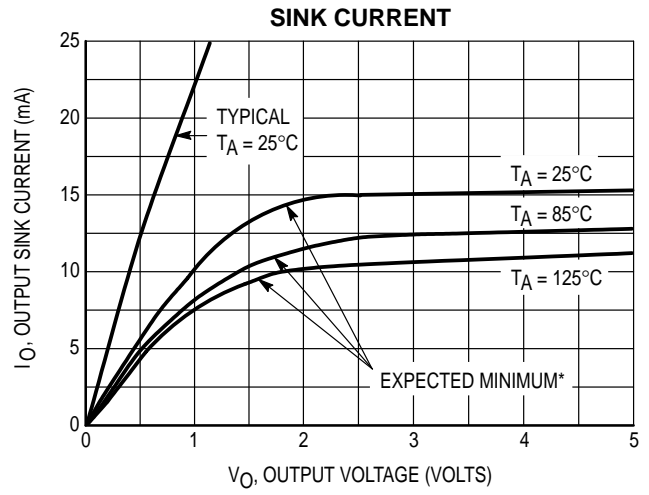
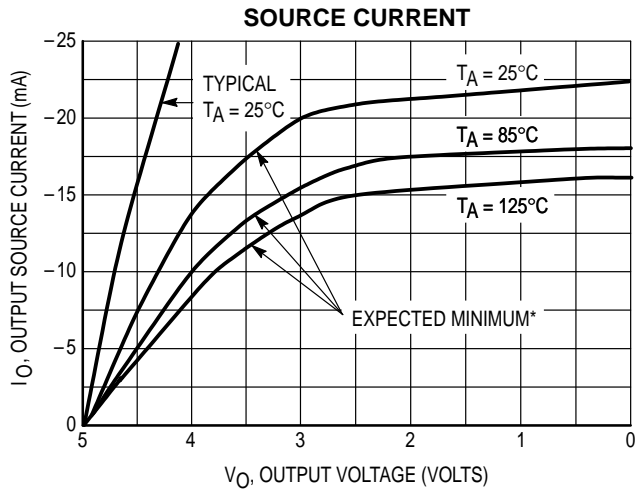
#### LT (Pin 3)

Active–low lamp test. A low level on this input causes all outputs to assume a high level. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

#### LE (Pin 5)

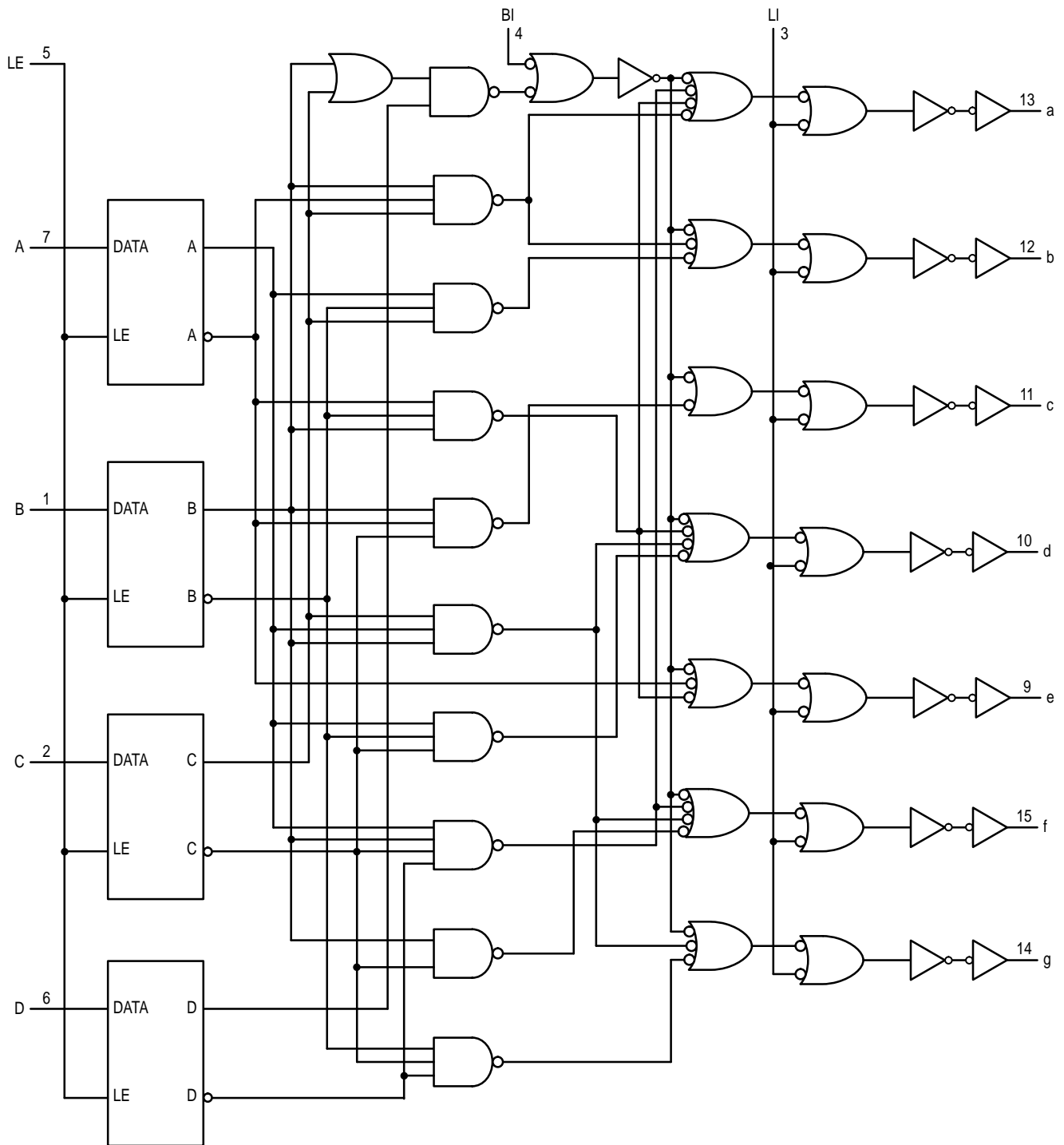
Latch enable input. This input controls the 4–bit transparent latch. A high level on this input latches the code present at the A, B, C and D inputs, a low level allows the code to be transmitted through the latch to the decoder.

OUTPUT CHARACTERISTIC CURVES ( $V_{CC} = 5\text{ V}$ )



\* The expected minimum curves are not guarantees, but are design aids.

EXPANDED LOGIC DIAGRAM



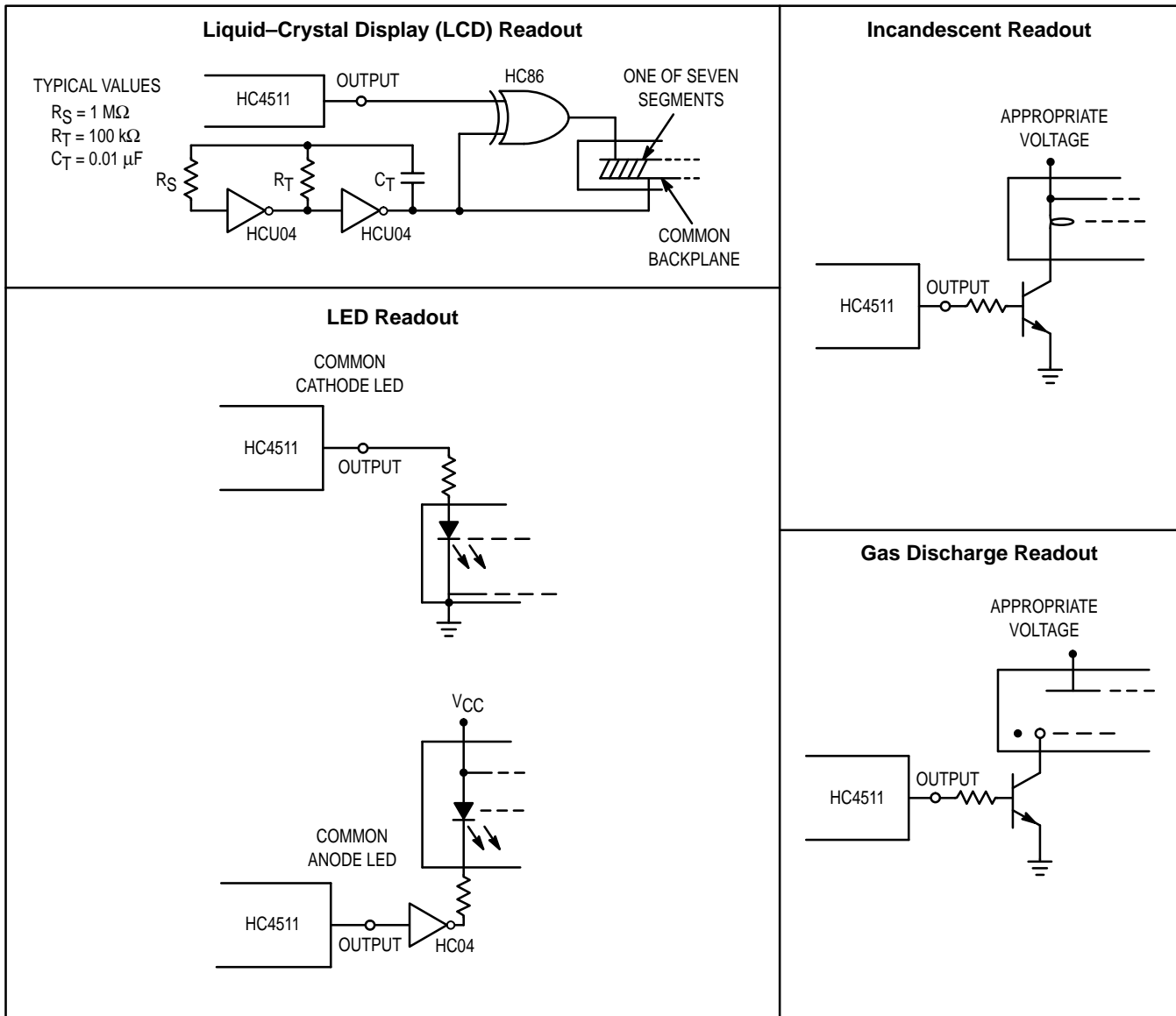
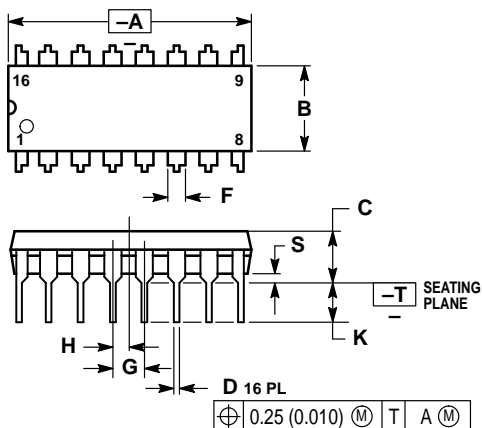


Figure 7. Connections to Various Display Readouts



OUTLINE DIMENSIONS

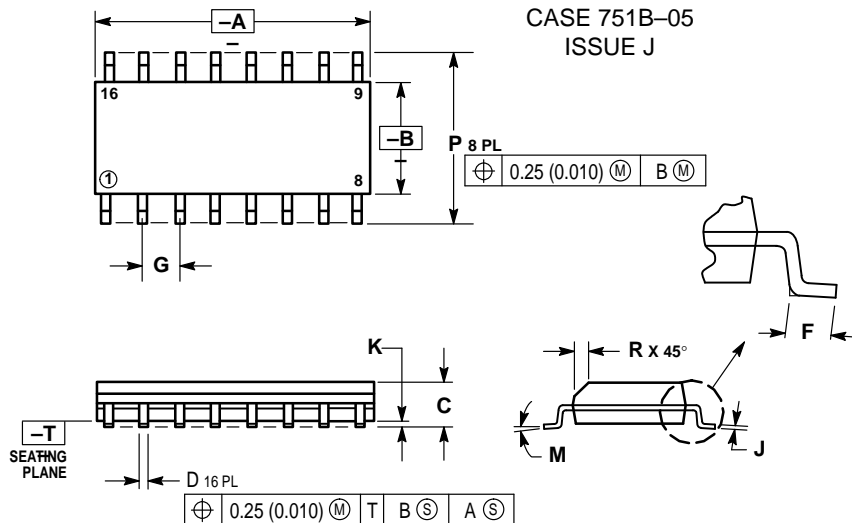
**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751B-05**  
**ISSUE J**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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◇ CODELINE

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