

MC74AC373, MC74ACT373

Octal Transparent Latch with 3-State Outputs

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state.

Features

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT373 Has TTL Compatible Inputs
- Pb-Free Packages are Available

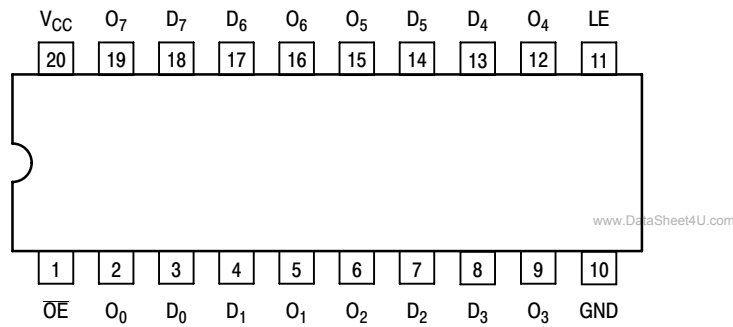


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O ₀ -O ₇	3-State Latch Outputs

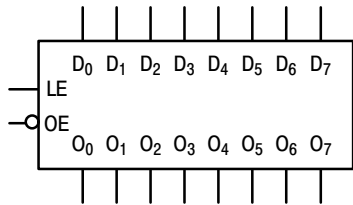
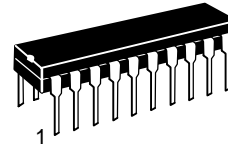


Figure 2. Logic Symbol

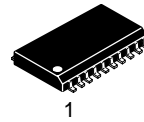


ON Semiconductor®

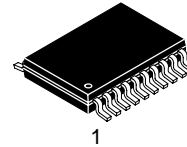
<http://onsemi.com>



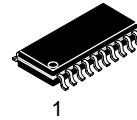
PDIP-20
N SUFFIX
CASE 738



SOIC-20W
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E



SOEIAJ-20
M SUFFIX
CASE 967

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

MC74AC373, MC74ACT373

TRUTH TABLE

Inputs			Outputs
\overline{OE}	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H = HIGH Voltage Level

L = LOW Voltage Level

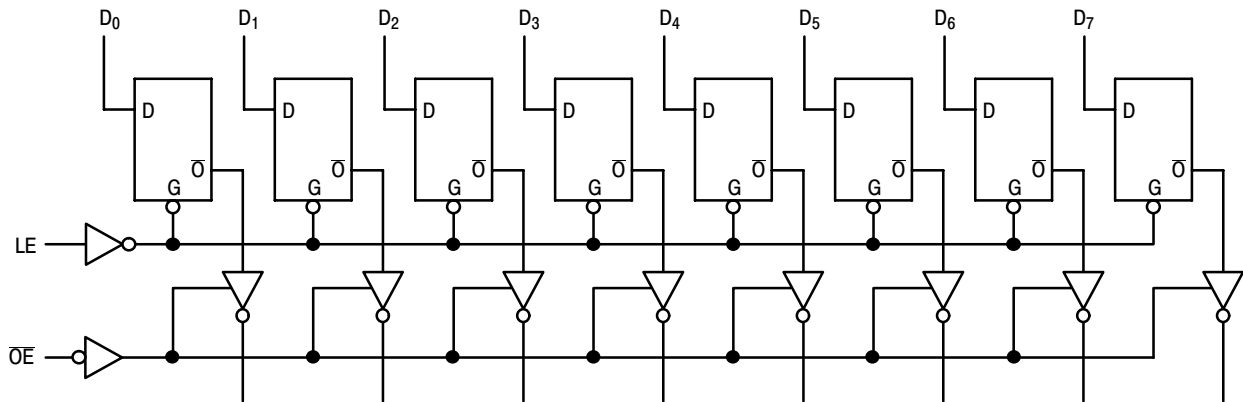
Z = High Impedance

X = Immaterial

O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MC74AC373, MC74ACT373

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V_{CC}	V	
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	-	150	-	ns/V
		V_{CC} @ 4.5 V	-	40	-	
		V_{CC} @ 5.5 V	-	25	-	
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	-	10	-	ns/V
		V_{CC} @ 5.5 V	-	8.0	-	
T_J	Junction Temperature (PDIP)	-	-	140	$^{\circ}\text{C}$	
T_A	Operating Ambient Temperature Range	-40	25	85	$^{\circ}\text{C}$	
I_{OH}	Output Current – High	-	-	-24	mA	
I_{OL}	Output Current – Low	-	-	24	mA	

- V_{IN} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC373, MC74ACT373

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0	-	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA
		4.5	-	3.86	3.76			
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	-	0.36	0.44			
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5	-	±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

MC74AC373, MC74ACT373

AC CHARACTERISTICS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	10 7.0	13.5 9.5	1.5 1.5	15 10.5	ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	9.5 7.0	13 9.5	1.5 1.5	14.5 10.5	ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	10 7.5	13.5 9.5	1.5 1.5	15 10.5	ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	9.5 7.0	12.5 9.5	1.5 1.5	14 10.5	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	9.0 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	8.5 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	10 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0	3.5 2.0	5.5 4.0	6.0 4.5		ns	3-9
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0	-3.0 -1.5	1.0 1.0	1.0 1.0		ns	3-9
t _w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.0	5.5 4.0	6.0 4.5		ns	3-6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC373, MC74ACT373

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76			
5.5	-	4.86	4.76					
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44			
5.5	-	0.36	0.44					
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OZ}	Maximum 3-State Current	5.5	-	±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

MC74AC373, MC74ACT373

AC CHARACTERISTICS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	8.5	10	1.5	11.5	ns	3–5
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3–5
t _{PLH}	Propagation Delay LE to O _n	5.0	2.5	8.5	11	2.0	11.5	ns	3–6
t _{PHL}	Propagation Delay LE to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3–6
t _{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns	3–7
t _{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.5	10.5	ns	3–8
t _{PHZ}	Output Disable Time	5.0	2.5	9.0	11	2.5	12.5	ns	3–7
t _{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.0	10	ns	3–8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS (For Figures and Waveforms – See AND8277/D at www.onsemi.com)

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	3.0	7.0	8.0	ns	3–9	
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0	0	1.0	ns	3–9	
t _w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns	3–6	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V

MC74AC373, MC74ACT373

ORDERING INFORMATION

Device	Package	Shipping†
MC74AC373N	PDIP-20	18 Units / Rail
MC74AC373NG	PDIP-20 (Pb-Free)	
MC74ACT373N	PDIP-20	
MC74ACT373NG	PDIP-20 (Pb-Free)	
MC74AC373DW	SOIC-20	38 Units / Rail
MC74AC373DWG	SOIC-20 (Pb-Free)	
MC74AC373DWR2	SOIC-20	1000 / Tape & Reel
MC74AC373DWR2G	SOIC-20 (Pb-Free)	
MC74ACT373DW	SOIC-20	38 Units / Rail
MC74ACT373DWG	SOIC-20 (Pb-Free)	
MC74ACT373DWR2	SOIC-20	1000 / Tape & Reel
MC74ACT373DWR2G	SOIC-20 (Pb-Free)	
MC74AC373DT	TSSOP-20*	75 Units / Rail
MC74AC373DTG	TSSOP-20*	
MC74AC373DTR2	TSSOP-20*	2500 / Tape & Reel
MC74AC373DTR2G	TSSOP-20*	
MC74ACT373DT	TSSOP-20*	75 Units / Rail
MC74ACT373DTG	TSSOP-20*	
MC74ACT373DTR2	TSSOP-20*	2500 / Tape & Reel
MC74ACT373DTR2G	TSSOP-20*	
MC74AC373MEL	SOEIAJ-20	2000 / Tape & Reel
MC74AC373MELG	SOEIAJ-20 (Pb-Free)	
MC74ACT373MEL	SOEIAJ-20	2000 / Tape & Reel
MC74ACT373MELG	SOEIAJ-20 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*These packages are inherently Pb-Free.

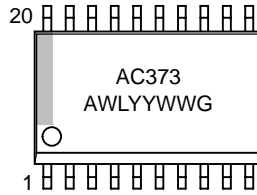
MC74AC373, MC74ACT373

MARKING DIAGRAMS

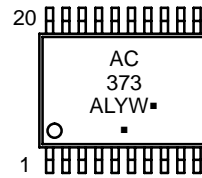
PDIP-20



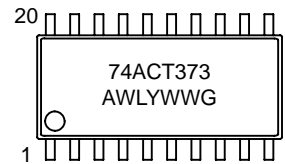
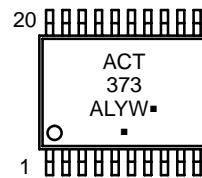
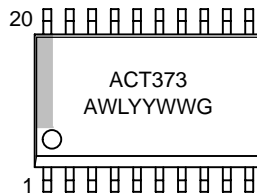
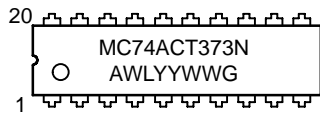
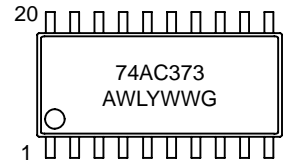
SOIC-20W



TSSOP-20



SOEIAJ-20

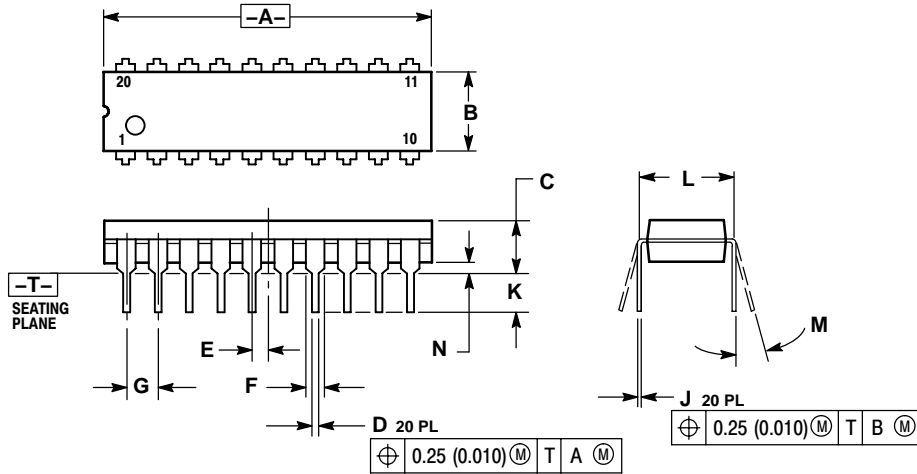


A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ▪ = Pb-Free Package
 (Note: Microdot may be in either location)

MC74AC373, MC74ACT373

PACKAGE DIMENSIONS

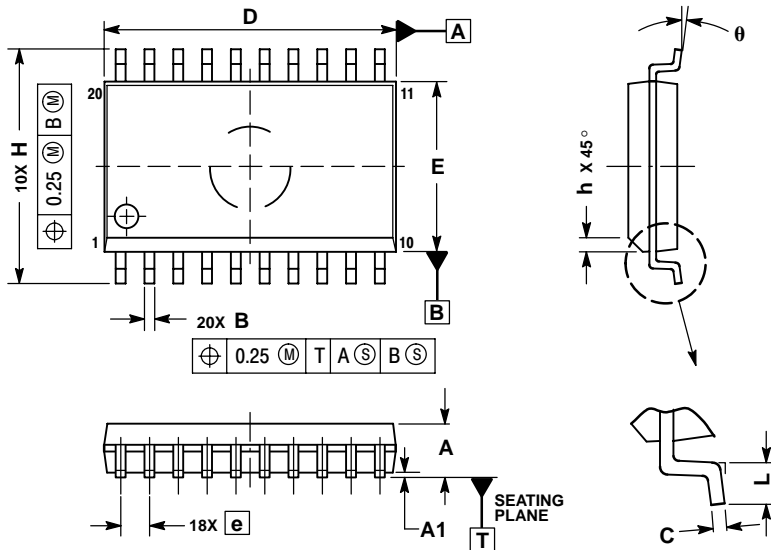
PDIP-20
N SUFFIX
 PLASTIC DIP PACKAGE
 CASE 738-03
 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOIC-20W
DW SUFFIX
 CASE 751D-05
 ISSUE G



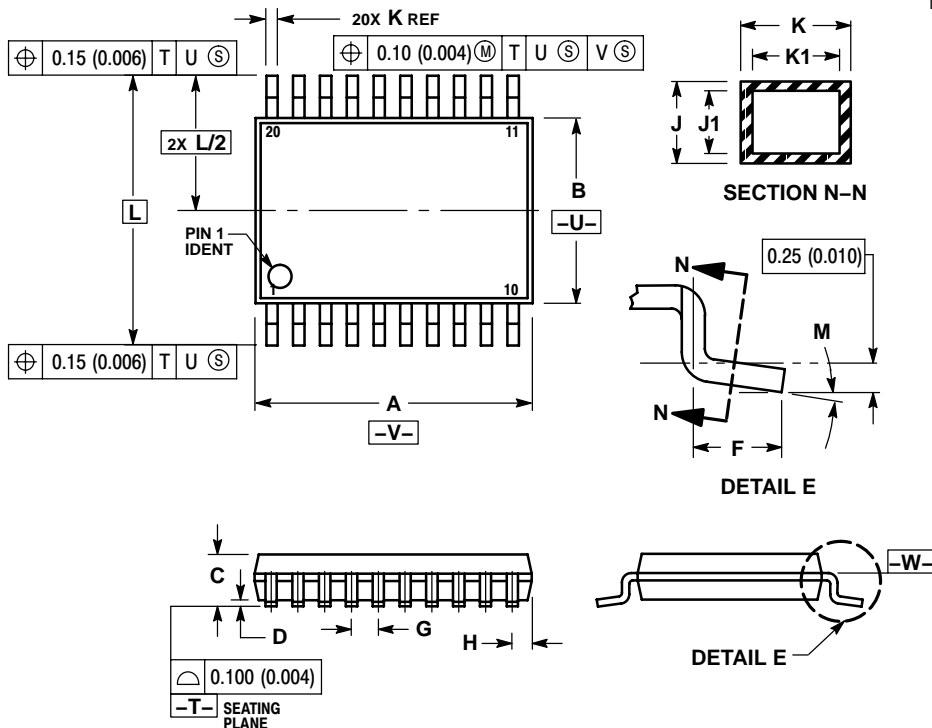
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

MC74AC373, MC74ACT373

PACKAGE DIMENSIONS

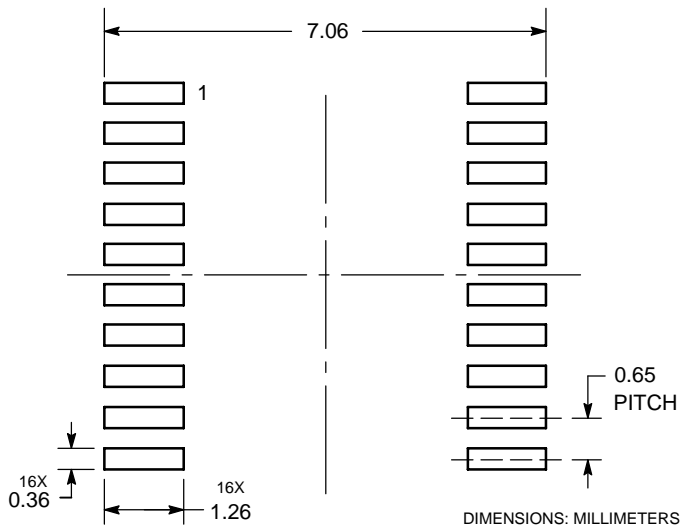
TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*

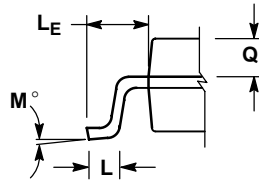
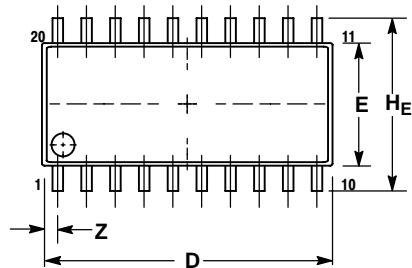


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

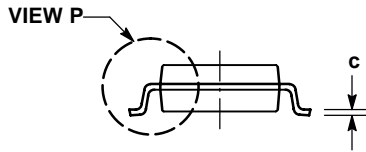
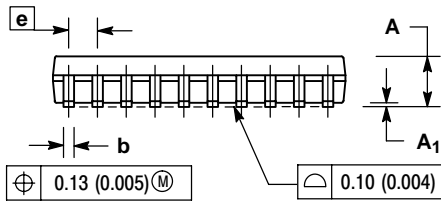
MC74AC373, MC74ACT373

PACKAGE DIMENSIONS

SOEIAJ-20
M SUFFIX
CASE 967-01
ISSUE A



DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0° - 10°		0° - 10°	
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC74AC373/D