

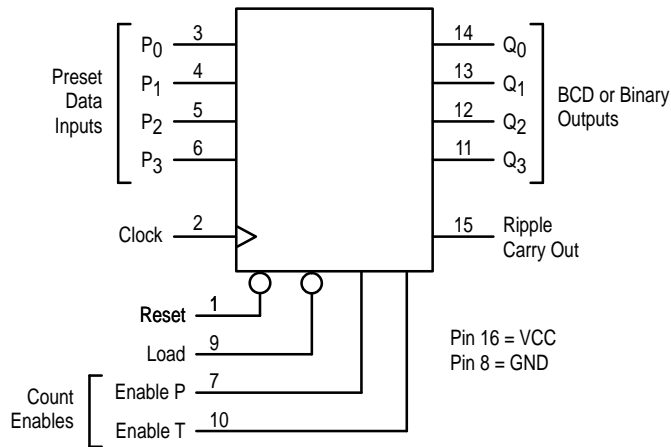
## Presetable Counters High-Performance Silicon-Gate CMOS

The MC54/74HCT161A and HCT163A are identical in pinout to the LS161A and LS163A. These devices may be used as level converters for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT161A and HCT163A are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- TTL, NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 200 FETs or 50 Equivalent Gates

### LOGIC DIAGRAM



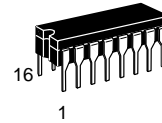
### FUNCTION TABLE

Inputs					Output Q
Clock	Reset*	Load	Enable P	Enable T	
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

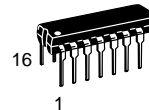
H = High Level; L = Low Level; X = Don't Care

\* = HCT163A only. HCT161A is an "Asynchronous-Reset" device.

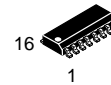
## MC54/74HCT161A MC54/74HCT163A



**J SUFFIX**  
 CERAMIC PACKAGE  
 CASE 620-10



**N SUFFIX**  
 PLASTIC PACKAGE  
 CASE 648-08



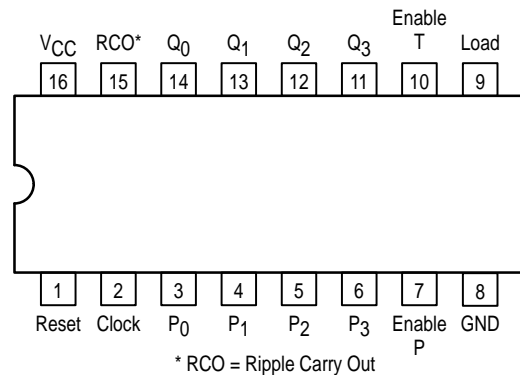
**D SUFFIX**  
 SOIC PACKAGE  
 CASE 751B-05

### ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC

Device	Count Mode	Reset Mode
HCT161A	Binary	Asynchronous
HCT163A	Binary	Synchronous

### Pinout: 16-Lead Package (Top View)



# MC54/74HCT161A MC54/74HCT163A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Positive DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	- 1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature Range	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package Ceramic DIP	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125° C  
Ceramic DIP: - 10 mW/°C from 100° to 125° C  
SOIC Package: - 7 mW/°C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25° C	≤ 85° C	≤ 125° C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> = -1.0V  I <sub>out</sub>   ≤ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5	0.80	0.80	0.80	V
			5.5	0.80	0.80	0.80	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.70	V
			5.5	0.10	0.10	0.10	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	4.5	0.10	0.10	0.10	μA
			5.5	± 0.10	± 1.00	± 1.00	
I <sub>CC</sub>	Maximum Quiescent Supply Current (Per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	4.5	4	40	160	μA
			5.5				
I <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4V, Any One Input V <sub>IN</sub> = V <sub>CC</sub> or GND Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ -55° C	25 to +125° C		mA
				2.9	2.4		

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V} \pm 10\%$ ;  $C_L = 50\text{ pF}$ , Input  $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Fig	Guaranteed Limit			Unit
			- 55 to 25° C	≤85° C	≤125° C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle)*	1,7	30	24	20	MHz
$t_{PLH}$	Maximum Propagation Delay Clock to Q	1,7	20	23	28	ns
$t_{PHL}$		1,7	25	30	32	ns
$t_{PHL}$	Maximum Propagation Delay Reset to Q (HCT161A Only)	2,7	25	29	33	ns
$t_{PLH}$	Maximum Propagation Delay Enable T to Ripple Carry Out	3,7	16	18	20	ns
$t_{PHL}$		3,7	21	24	28	ns
$t_{PLH}$	Maximum Propagation Delay Clock to Ripple Carry Out	1,7	22	25	28	ns
$t_{PHL}$		1,7	28	33	35	ns
$t_{PHL}$	Maximum Propagation Delay Reset to Ripple Carry Out (HCT161A Only)	2,7	24	28	32	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output	2,7	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	1,7	10	10	10	pF

\* Applies to noncascaded/nonsynchronous clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine  $f_{max}$ . However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the  $f_{max}$  in the table above is applicable. See Applications information in this data sheet.

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

$C_{PD}$	Power Dissipation Capacitance (Per Gate)*	Typical @ 25° C, $V_{CC} = 5.0\text{ V}$		pF
		60		

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**TIMING REQUIREMENTS** ( $V_{CC} = 5.0\text{ V} \pm 10\%$ ;  $C_L = 50\text{ pF}$ , Input  $t_r = t_f = 6.0\text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			- 55 to 25° C	≤85° C	≤125° C	
$t_{su}$	Minimum Setup Time, Preset Data Inputs to Clock	5	12	18	20	ns
	Minimum Setup Time, Load to Clock	5	12	18	20	ns
	Minimum Setup Time, Reset to Clock (HCT163A Only)	4	12	18	20	ns
	Minimum Setup Time, Enable T or Enable P to Clock	6	12	18	20	ns
$t_h$	Minimum Hold Time, Clock to Preset Data Inputs	5	3	3	3	ns
	Minimum Hold Time, Clock to Load	5	3	3	3	ns
	Minimum Hold Time, Clock to Reset (HCT163A Only)	4	3	3	3	ns
	Minimum Hold Time, Clock to En T or En P	6	3	3	3	ns
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (HCT161A Only)	2	12	17	23	ns
	Minimum Recovery Time, Load Inactive to Clock	2	12	17	23	ns
$t_w$	Minimum Pulse Width, Clock	1	12	15	18	ns
	Minimum Pulse Width, Reset (HCT161A Only)	1	12	15	18	ns
$t_r, t_f$	Maximum Input Rise and Fall Times		500	500	500	ns

**FUNCTION DESCRIPTION**

The HCT161A/163A are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading and count-enable controls.

The HCT161A and HCT163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

**INPUTS**

**Clock (Pin 2)**

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading occur with the rising edge of the Clock input. In addition, control functions, such as resetting (HCT163A) and loading occur with the rising edge of the Clock Input.

**Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)**

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (Pin 3) is the least-significant bit and P3 (Pin 6) is the most-significant bit.

**OUTPUTS**

**Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)**

These are the counter outputs. Q0 (Pin 14) is the least-significant bit and Q3 (Pin 11) is the most-significant bit.

**Ripple Carry Out (Pin 15)**

When the counter is in its maximum state 1111, this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot \text{Q0} \cdot \text{Q1} \cdot \text{Q2} \cdot \text{Q3}$$

**CONTROL FUNCTIONS**

**Resetting**

A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HCT161A resets asynchronously, and the HCT163A resets with the rising edge of the Clock input (synchronous reset).

**Loading**

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

**Count Enable/Disable**

These devices have two count-enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

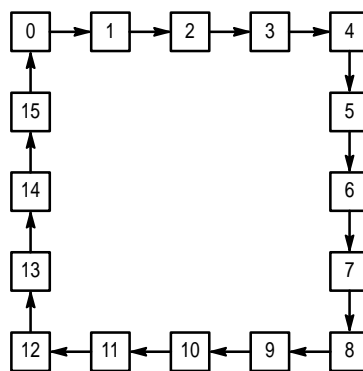
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control: Enable T is both a count-enable and a Ripple-Carry Output control.

**Table 1. Count Enable/Disable**

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0-Q3 are maximum*
X	X	L	No Count	L

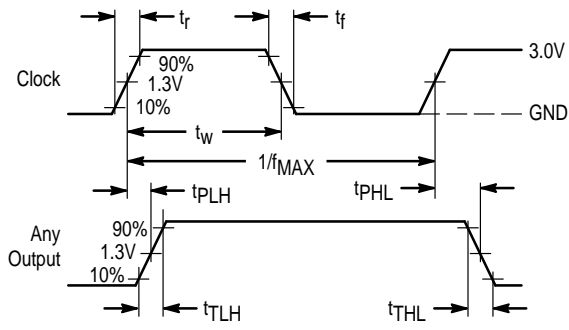
Q0 through Q3 are maximum when Q3 Q2 Q1 Q0 = 1111.

**OUTPUT STATE DIAGRAM**

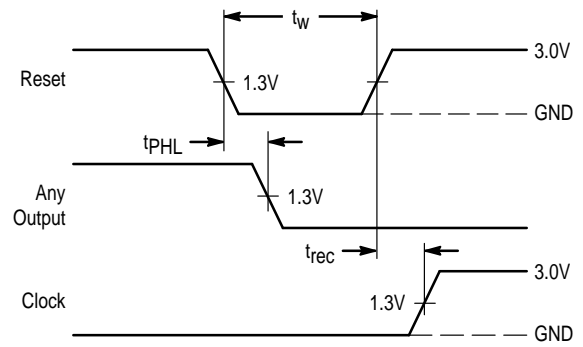


**Binary Counters**

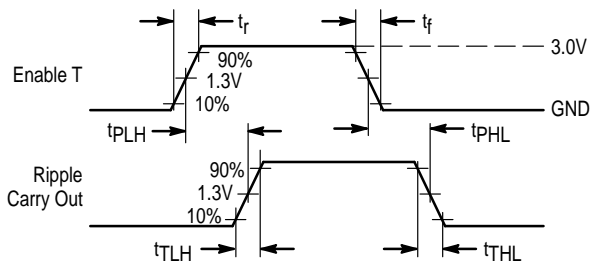
**SWITCHING WAVEFORMS**



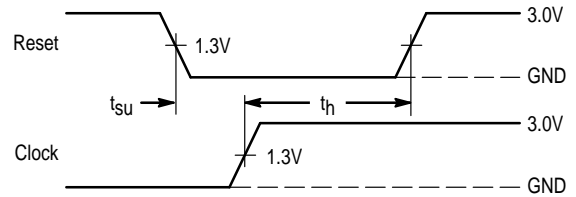
**Figure 1.**



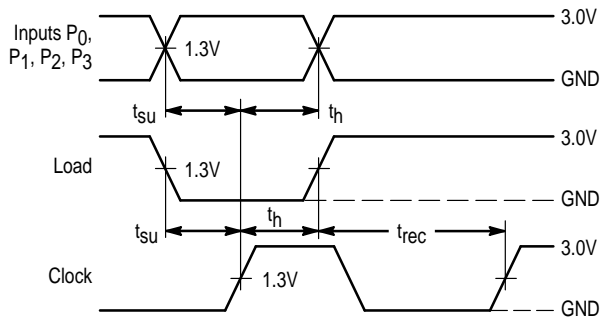
**Figure 2.**



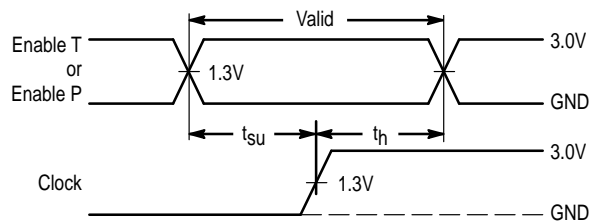
**Figure 3.**



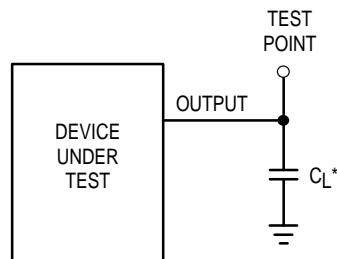
**Figure 4. HCT163A Only**



**Figure 5.**



**Figure 6.**



\*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

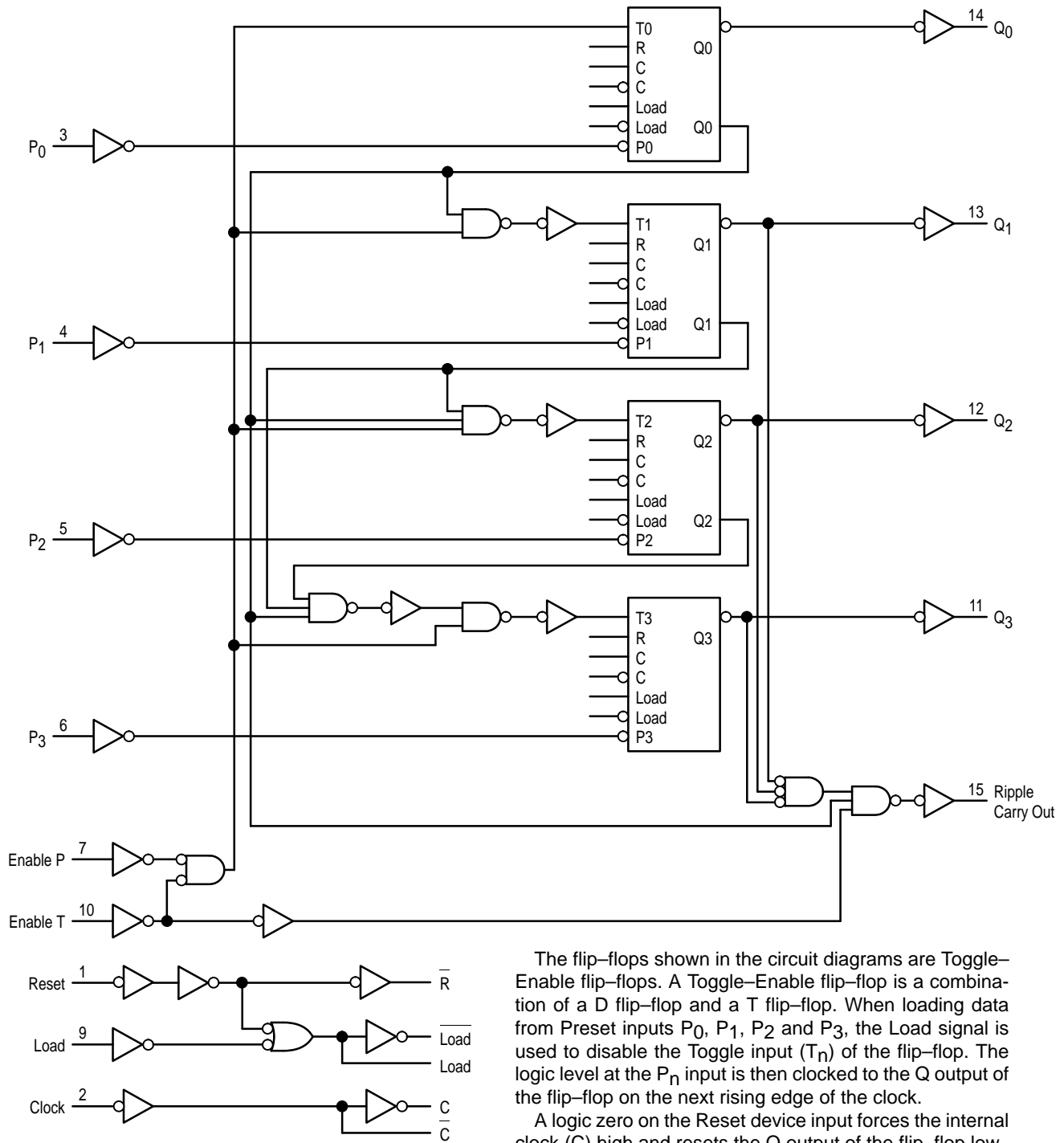


Figure 8. 4-Bit Binary Counter with Asynchronous Reset (MC54/74HCT161A)

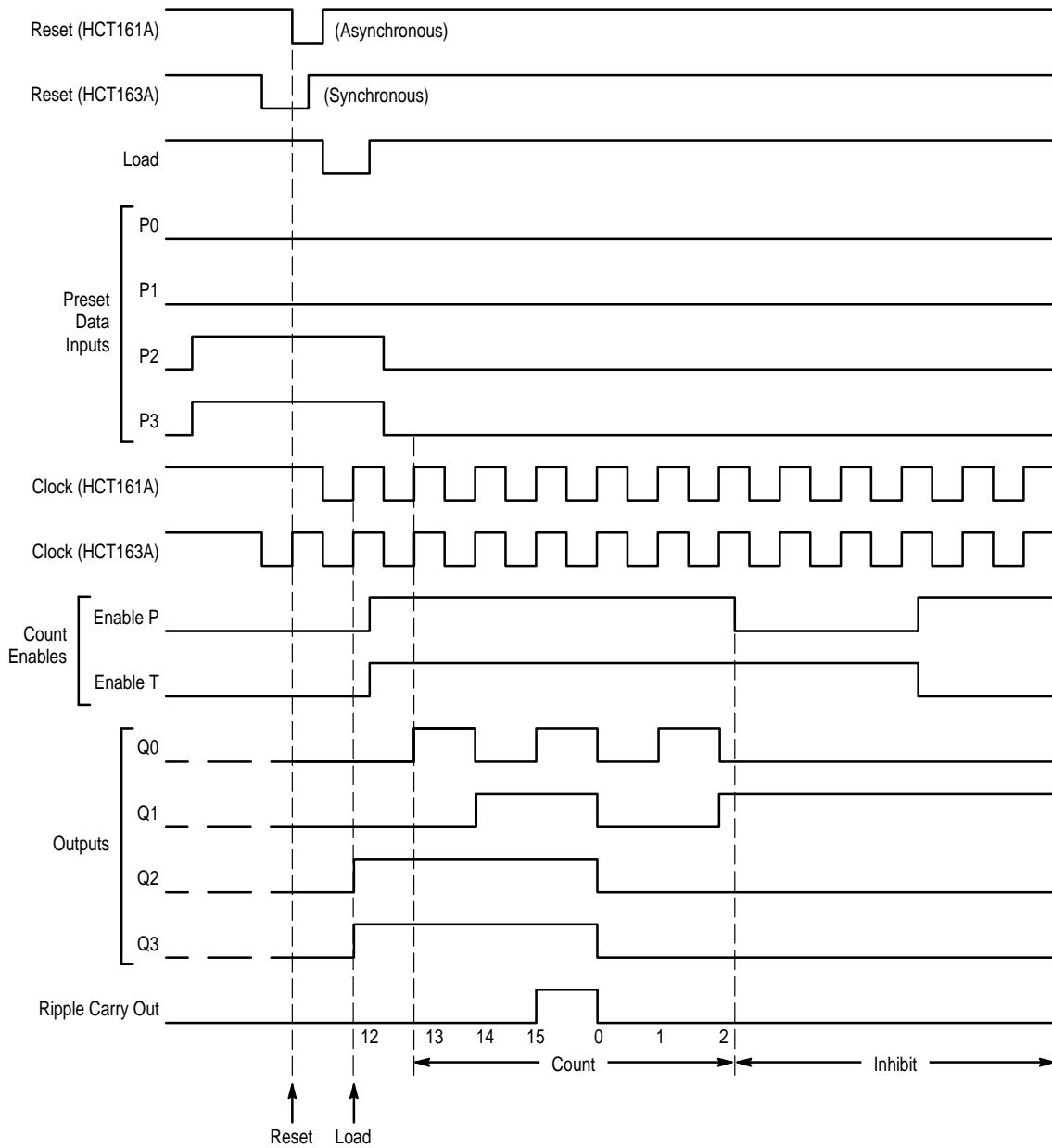


Figure 9. Timing Diagram

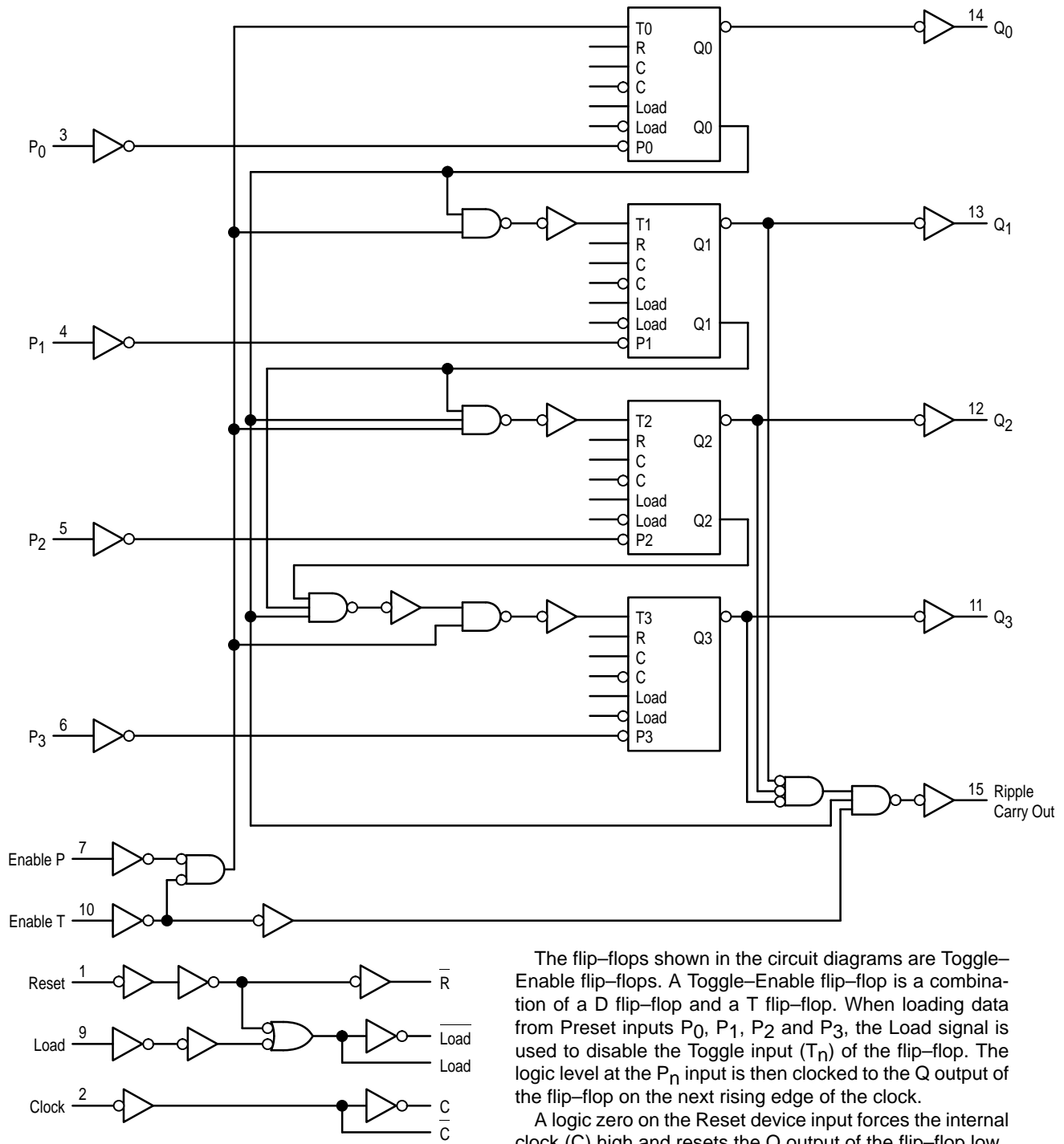
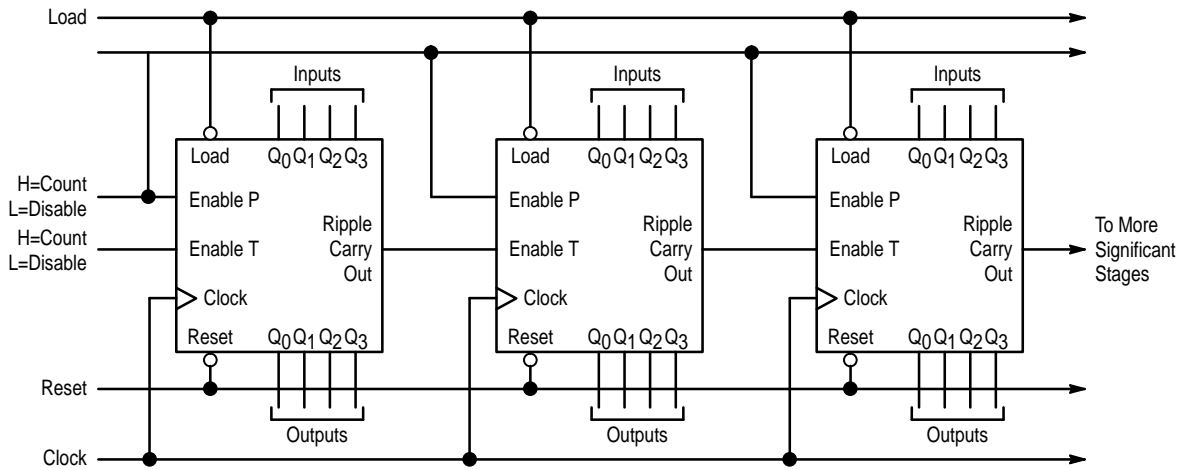


Figure 10. 4-Bit Binary Counter with Synchronous Reset (MC54/74HCT163A)

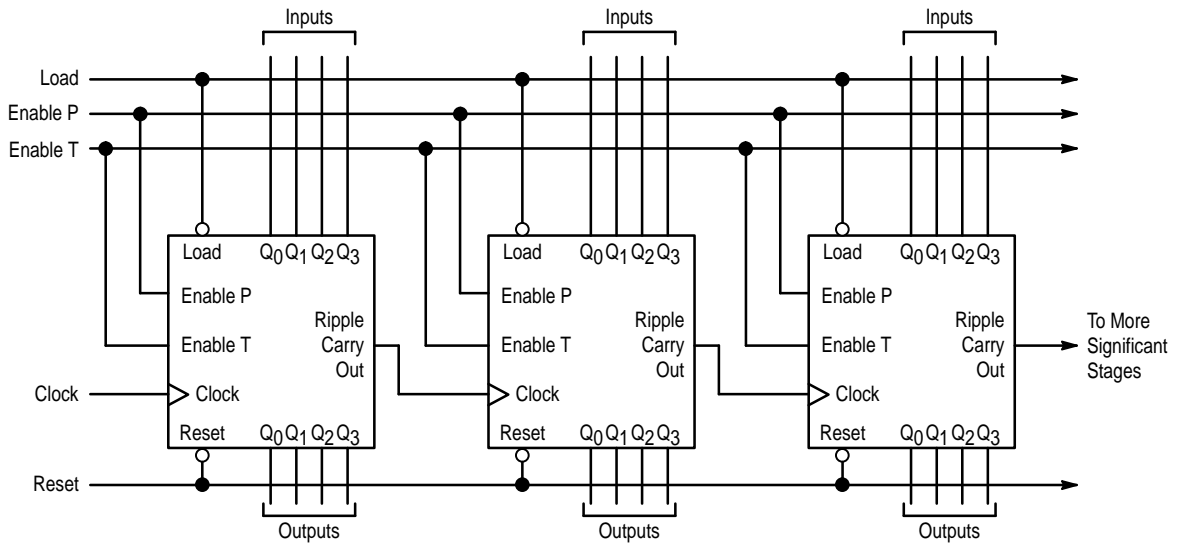


**TYPICAL APPLICATIONS CASCADING**



NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set-up times between Enable (port) and clock.

**Figure 11. N-Bit Synchronous Counters**



**Figure 12. Nibble Ripple Counter**

TYPICAL APPLICATIONS VARYING THE MODULUS

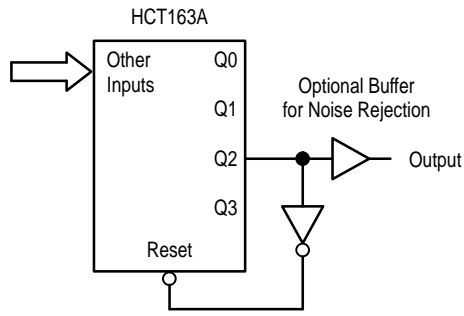


Figure 13. Modulo-5 Counter

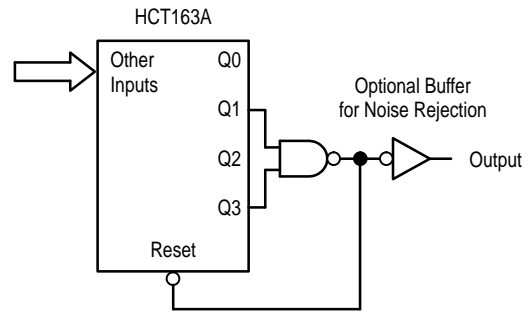
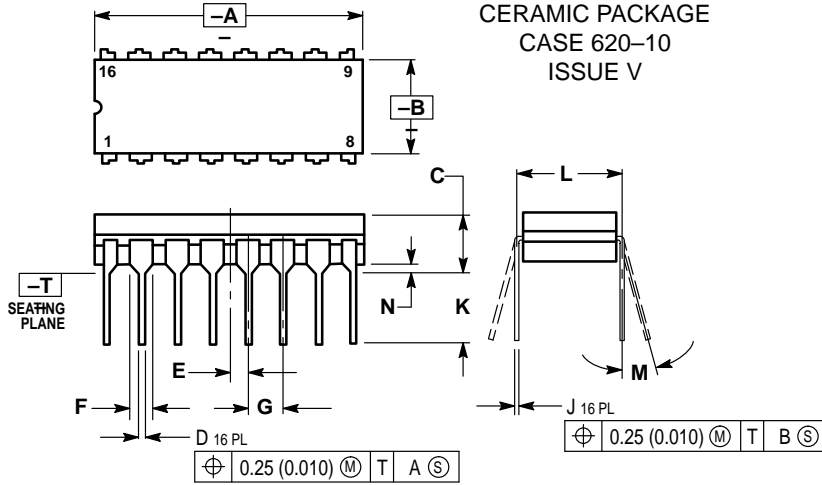


Figure 14. Modulo-11 Counter

The HCT163A facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.

OUTLINE DIMENSIONS

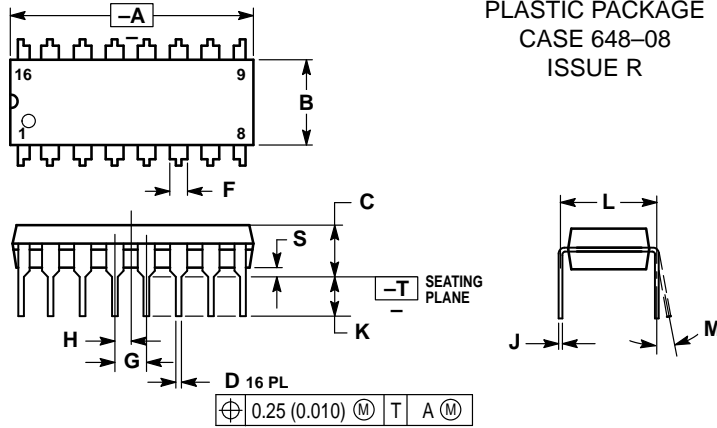
**J SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10  
ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

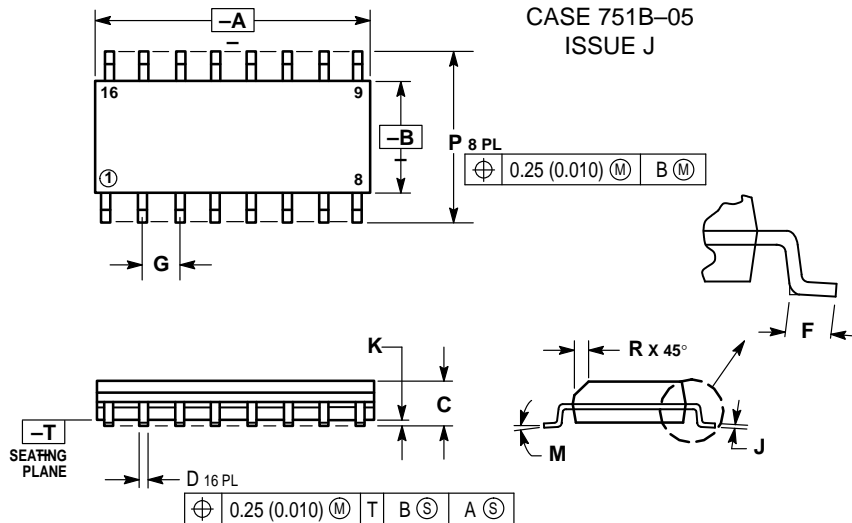
**N SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08  
ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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◇ CODELINE

MC54/74HCT161A/D

